CMOS Realization of the Operational Mirror Amplifier

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Abstract: - The design of a CMOS operational mirrored amplifier (OMA) suitable for high frequency applications is proposed. The CMOS operational mirrored amplifier is developed using class AB operational amplifier and two current mirrors. To obtain a wide bandwidth and high stability, HF feedforward techniques have been used. These techniques made the proposed circuit suitable for continuous – time analog signal processing. Simulation results for the proposed CMOS operational mirror amplifier circuit using PSpice are presented. Also, a performance comparison with pervious realization using BJT is given.

Key-Words: - Operational mirror amplifier, Nullor, Nullator, Darlington pair, CMOS, operational floating amplifier.

1 Introduction

Recently, current-mode analog integrated circuits in CMOS technology have received considerable interest. CMOS current-mode techniques can achieve considerable improvement in amplifier speed, high slew rate, low power consumption accuracy and bandwidth [1].

The controlled current source is an important analog building block in the electronic instrumentation. A monolithic circuit which can be used to construct a VCCS or a CCCS is the Operational Mirrored Amplifier (OMA) [2 - 3]. The OMA is a general purpose current mode building block, which consists of a high gain transconductance scheme with identical output currents.

An alternative important circuit which can also be used to construct a VCCS or a CCCS is the Operational Floating Amplifier (OFA). It consists of a transconductance amplifier featuring high gain and two current outputs I_{o1}=-I_{o2}. The main difference between OMA and OFA is the output currents [3 - 6].

The ideal OFA, whose symbol shown in Fig. 1(a), exhibits these terminal characteristics: $I_+ = I_-$ =0, V_+=V_- and I_{o1} = -I_{o2}. Similarly, the OMA, whose symbol shown in Fig. 1(b), has terminal characteristics as follows: I_+=I_-=0, V_+=V_- and I_{o1}=I_{o2}. The output of the OMA can be expressed by equation (1) where G_m is the open loop transconductance gain of the OMA. When a negative feedback is applied, the voltages at the two input ports are forced to be equal as expressed by equation (2).

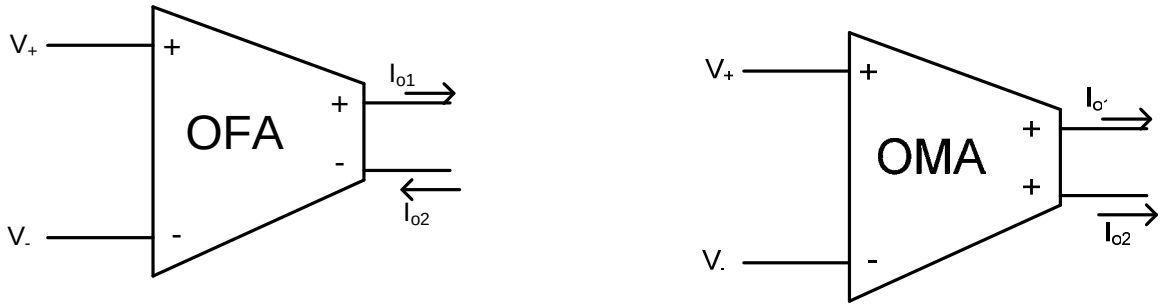
$$I_{o1}=I_{o2}=G_m (V_+ - V_-) \quad (1)$$

$$V_+ = V_- \quad \text{as } G_m \longrightarrow \infty. \quad (2)$$

As the finite open loop gain G_m decreases, the difference between the two voltages increase. Therefore, the open loop transconductance gain is required to be as large as possible in order to improve the performance.

The OMA was first presented in [2], the design was realized using the BJT technology and a supply voltage of ±15V, and thus it can not fulfill the modern integrated circuits design requirements because of its high supply voltage.

In this paper, the CMOS realization of the OMA presented in [2] is introduced with necessary modifications to operate with low supply voltage. The PSpice simulations of the CMOS circuit are also introduced to verify the operation. The paper is organized as follows, in section 2, the original OMA design using BJT in [2] is presented and simulated, then, the proposed CMOS realization of the OMA is presented and also the PSpice simulations demonstrated. Finally, the conclusion is drawn in section 3.



(a) (b)

Fig. 1. (a) Symbol of the OFA, (b) Symbol of the OMA.

2 OMA Design

2.1 BJT realization of the OMA [2]

The simplified circuit diagram of the first proposed OMA [2] is shown in Fig. 2(a). It consists of an input stage and two current mirrors. The first current mirror $T_2 - T_4$ is realized by Wilson current mirror to minimize the error in the current transfer I_4/I_2 where:

$$\frac{I_4}{I_2} = \frac{1}{1+\frac{2}{\beta^2}} \tag{3}$$

The second current mirror consists of two current measuring diodes $D_1 - D_2$ and a regulating amplifier (A) with the transistor T_1. In this case, the absolute error in the current transfer I_1/I_3 is due to the mismatch between the diodes and the non – ideal properties of the regulating amplifier. The output currents are given by:

$$I_{o1} = I_1 - I_2 = I_3 - I_4 = I_{o2} \tag{4}$$

To reduce non – ideal effects and increase β of the input stage, the transistors are connected in parallel as shown in Fig.2 (b). The total β could be obtained as follow:

$$\beta_{tot} = \beta_1 + \beta_2 \tag{5}$$

Also, to increase the OMA bandwidth, the transistor pair shown in Fig 2(c) is used in the output stage. This configuration is called Darlington pair [7] and at frequencies below ω_1 the circuit behaves like a normal Darlington pair with

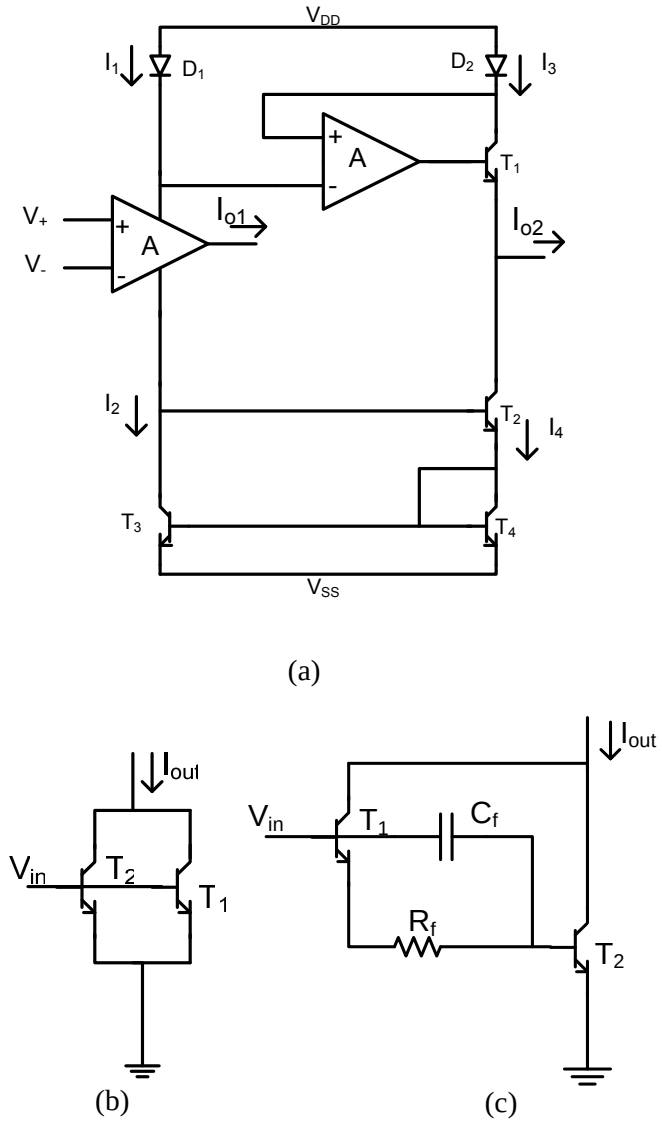


Fig. 2. (a) Simplified circuit diagram of the OMA, (b)Two transistor connected in parallel, (c)Darlington configuration.

current gain of $\beta_{totD,}$ eqns.(6-7), while at frequencies above ω_2, the transistor T_1 is by – passed via

capacitor C_f resulting in a current gain of β_h, eqns.(8-9), where:

$$\omega_1 = \frac{1}{\beta_1 \beta_2 R_f C_f} \quad (6)$$

$$\beta_{totD} = \beta_1 \beta_2 \quad (7)$$

$$\omega_2 = \frac{1}{R_f C_f} \quad (8)$$

$$\beta_h = \beta_2 \quad (9)$$

The BJT realization of the OMA block is shown in Fig 3. A differential pair $T_1 - T_5$ based on the configuration shown in Fig. 2(b) is used in the input stage to convert the input voltage to two output current with very high gain. These currents are applied to a level shifting $T_6 - T_9$ in order to provide proper level shifting and symmetrical operation. The transistors of the level shift stage are by – passed at high frequencies, thus avoiding the poor high frequency response of the transistors.

This is accomplished by using the all-pass networks R_1, C_1 and R_2, C_2.the output stage $T_{10} - T_{22}$ consists of a feed-forward stage based on the Darlington pair to prevent the high frequency peaking with capacitive loads and a current mirror stage to copy the output current to the second terminal. The simulated current mirror consists also of the measuring diodes $D_1 - D_4$.

Finally, the regulated amplifier is represented by the transistors $T_{23} - T_{32}$. As shown its input stage is realized by the configuration shown in Fig. 2(b) to increase the amplifier gain and reduce its non – ideal effects.

The circuit, shown in Fig. (3), has been simulated using PSpice and transistor parameters given in table 1. The supply voltages were ±1.5V, and biasing voltages of $V_{B1} = V_{B3} = 0.5V$, $V_{B2} = V_{B4} = -0.5V$. The open loop transconductance of the BJT based OMA is 19.5 dB referenced to a resistance of 2.4kΩ and a unity gain bandwidth of 5.5 kHz as shown in Fig.4 (a). The output currents of the OMA are shown in Fig. 4(b) and it's shown that the OMA can supply currents up-to 28μA.

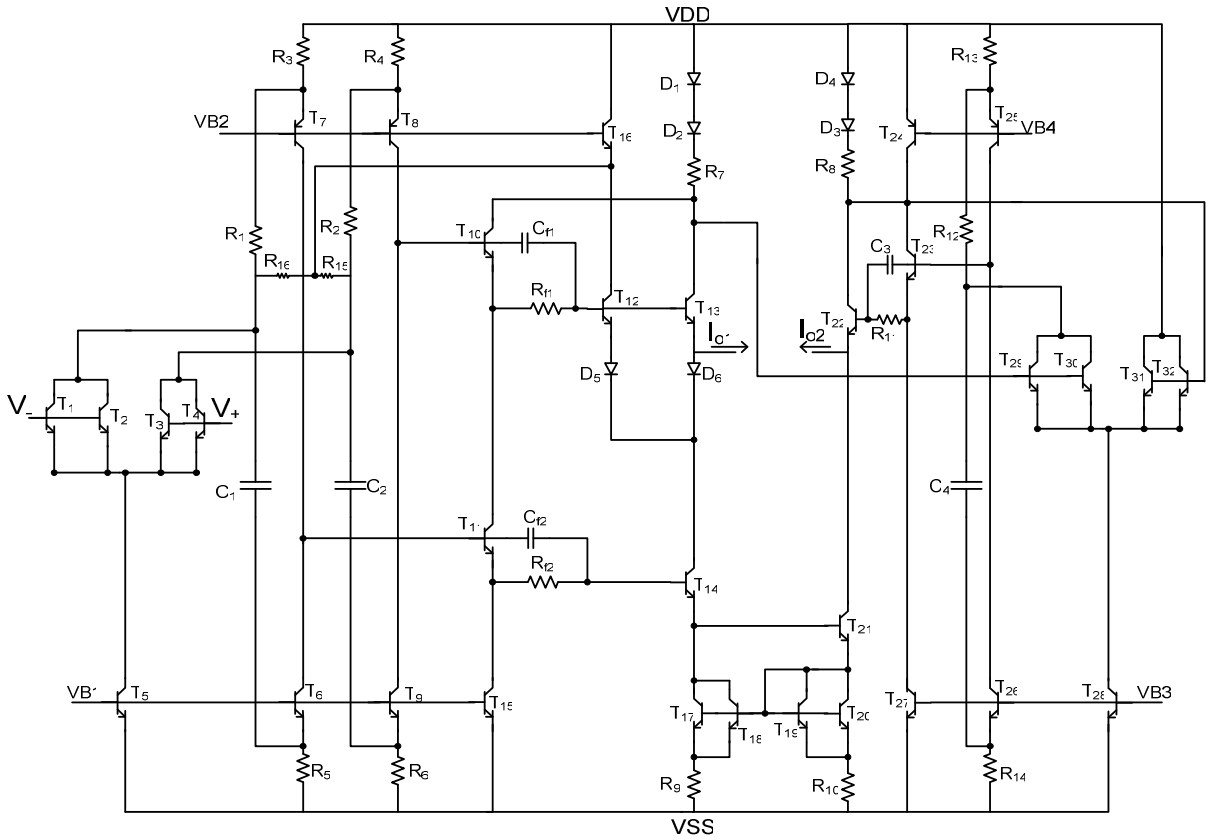
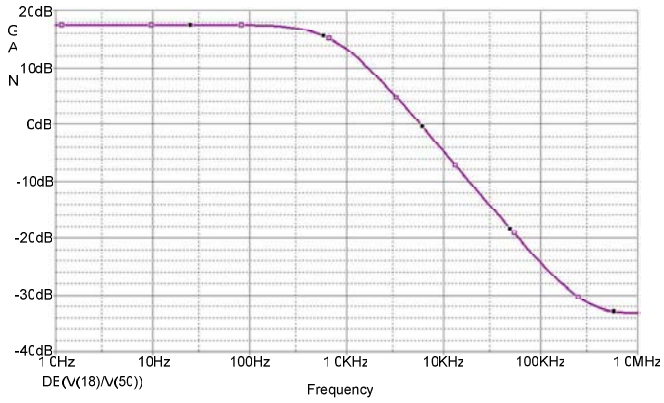
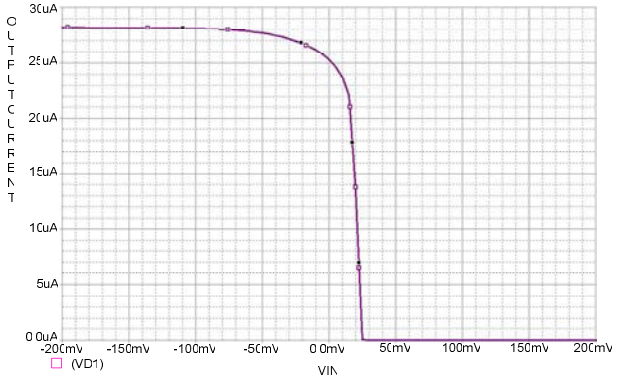


Fig. 3 BJT realization of the OMA [2].



(a)



(b)

Fig. 4 (a)The frequency responce and, (b) The output current of the BJT based OMA

2.2 The CMOS Realization

The CMOS realization of the OMA, shown in Fig. 5, is based on the simplified circuit diagram of Fig. 2(a). An adaptation for the circuit to be realizable in CMOS has been done, which has enabled the low voltage operation and reduced the circuit complexity.

First, the measuring diodes used in the current mirror are replaced with a simple active load for the current mirror, because such a diode configuration can not operate with such a low supply voltage.

Second, the parallel transistors configuration used in the BJT realization are not required here because the output current of the differential pair can be controlled by the transistors aspect ratio. To enable the high frequency operation of the OMA, the allpass networks used with the level shifting network are the same as the BJT technique. Also, an equivalent CMOS Darlington pair [8] is used for the same purpose.

So, the CMOS implementation becomes simpler than the BJT realization, where the current sensing circuits have been removed and the Wilson current source is used with a simple active load. In addition, the CMOS circuit has increased the band width and the maximum output current.

The proposed OMA is simulated using PSpice and level 3 parameters for 0.25μm standard CMOS process provided from MOSIS. The CMOS realization is operated from dual supply voltages ±1.5V, the transistors aspect ratio for the OMA is given in table 2 and the biasing voltages are V_{B1} = V_{B4} = 0.5V and V_{B3} = V_{B2} = -0.5V.

The frequency response of the OMA is shown in Fig.6 (a) showing a voltage gain of 56 dB referenced to a resistance of 2.4kΩ and a unity gain bandwidth of 80MHz. The output currents of the OMA are shown in Fig.6 (b) and it's shown that the OMA can supply currents up-to 250μA. A performance comparison between the BJT realization presented in [2] and the proposed CMOS realization is given in table 3.

3 Conclusion

The design of a CMOS monolithic class AB operational mirrored amplifier was presented. The proposed block is suitable to the realization of controlled current source. Darlington pairs are used to increase the circuit bandwidth and stability. The simulation results of the proposed OMA are also presented. A performance comparison between the BJT based OMA presented in [2] and its CMOS realization was given in table 3. From the comparison table, it is clear that the CMOS realization of the OMA has higher 3-dB bandwidth, unity gain bandwidth, maximum output current and gain than BJT realization. In addition to the CMOS realization is most suitable for modern integrated circuit design requirements.

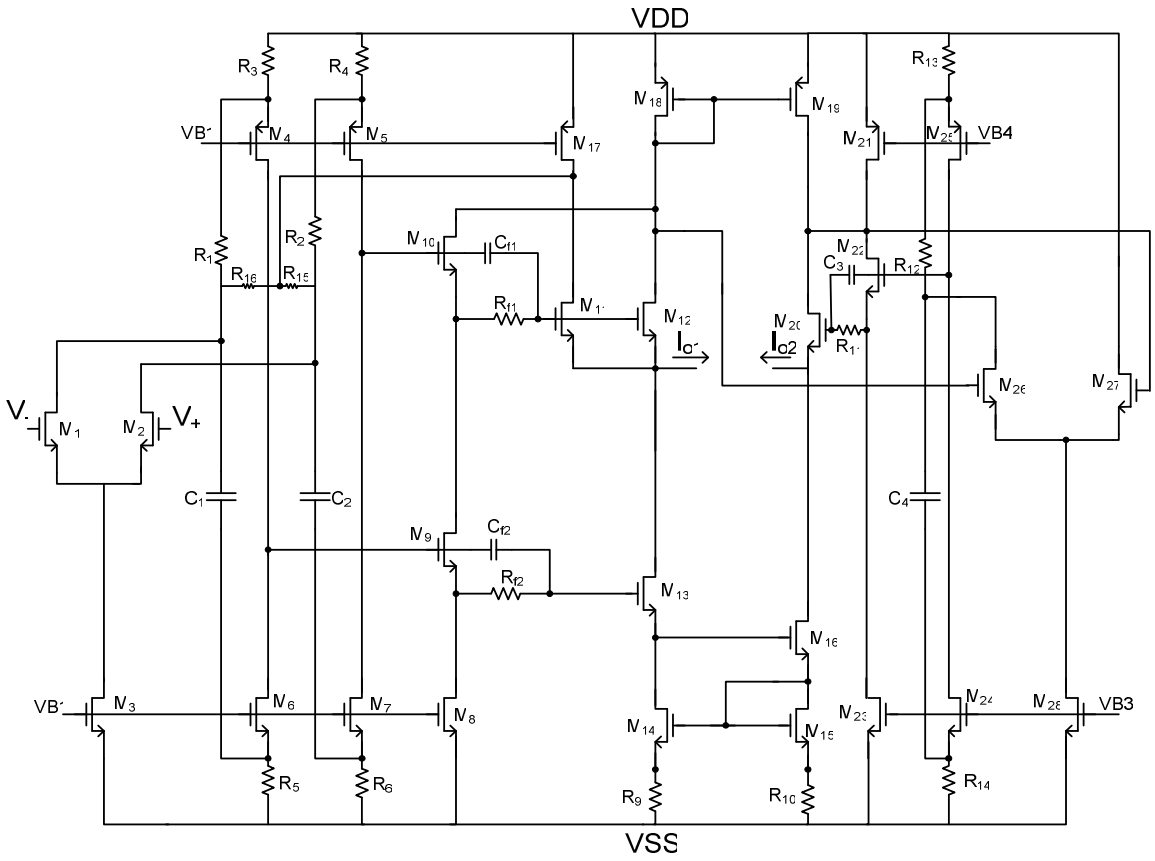
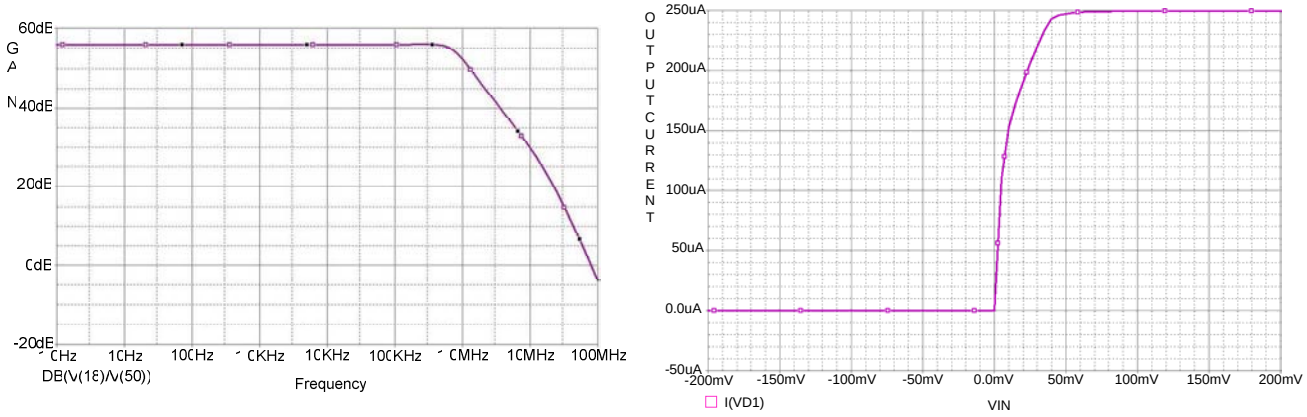


Fig. 5 The CMOS realization of the OMA.



(a) (b)

Fig. 6. (a) The frequency response, and (b) The output current of the CMOS OMA.

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Table 1. The PSPICE parameters of the BJT transistors.

Transistor	Model parameters
NPN transistor	IS =10.0E-15 XTI = 3.000E+00 EG=1.110E+00 VAF=1.00E+02 VAR=1.000E02 BF=466.5E+00 ISE =74.286E-15 NE=1.660E+00 IKF=14.000E-03 XTB=0.000E+00 BR=.1000E00 ISC=10.005E-15NC=2.000E+00 IKR=10.00E-03 RC=10.000E+00 CJC=786.51E-15 MJC=0.333E-00 VJC=0.7500E-00 FC=5.000E-01 CJE=1.28E-12 MJE=.336E-00 VJE=0.750E-00 TR=10.000E-09 TF=490.01E-12 ITF=.270E-0 XTF=5.38E+00 VTF=28.39E+0 PTF=0.000E+0 RE=0.0E+00 RB=0.00E+00 NK=.468
PNP transistor	IS=10.0E-15 XTI=3.000E+00 EG=1.110E+00 VAF=1.00E+02 VAR=1.000E+02 BF=94.5E+00 ISE=976.47E-15 NE=1.990E+00 IKF=1.1100E-03 XTB=0.000E+00 BR=.1000E+00 ISC=10.005E-15 NC=2.000E+00 IKR=10.00E-03 RC=10.000E+00 CJC=3.84E-12 MJC=0.333E-00 VJC=0.7500E-00 FC=5.000E-01 CJE=1.45E-12 MJE=.336E-00 VJE=0.750E-00 TR=10.000E-09 TF=24.3E-9 ITF=1.25E-00 XTF=10.05E+00 VTF=9.79E+00 PTF=0.000E+00 RE=0.0E+00 RB=0.00E+00 NK=.53

Table 2. Transistor aspect ratio for the CMOS OMA circuit.

Transistors	Aspect ratios (W/L)
M_1, M_2, M_{26}, M_{27}	55/0.25
M_3, M_{28}	55/10
M_6, M_7	2.5/32.25
M_8, M_9, M_{14} - M_{16}	80/0.25
M_4 – M_5, M_{24}, M_{25}, M_{28}	2.5/0.25
M_8, M_{11}- M_{13}, M_{18}, M_{19}, M_{20}, M_{22}	100/0.25
M_{17}, M_{21}, M_{23}	60/2.25

Table 3. Performance comparison between the proposed CMOS and BJT [2] realizations.

	BJT [2]	CMOS realization
# of transistors	34	28
Input range(mV)	NA	-0.019 to 32
3-dB bandwidth(kHz)	0.744	871
Unity gain frequency(MHz)	0.0055	80
Gain (dB)	19.5	56
Power dissipation (mW)	0.52	0.823
Maximum output current (μA)	28	250