Research on k-fault diagnosis and testability in analog circuit

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Abstract: - Fault diagnosis is very important for development and maintenance of safe and reliable electronic circuits and systems. Many k-fault diagnosis methods were put forward such as branch method, node method, loop method, mesh method, cut set method. But the tolerance effect as well as non-linear problems exist and are difficult to deal with. A fault diagnosis method for analog circuit is proposed in this paper, including the mathematical model and two improved algorithms about K-node method and K-branch method. The potential of the algorithms is demonstrated by an order active circuit example and the workload of the verification can be reduced. For the testability problems of analog circuit, testability analysis and testability design are researched under prescriptive condition. A testable topological condition which has nothing to do with the circuit parameters is put forward, and the testability analysis and testability design are carried out by a variety of convenient and flexible ways. The method is extended to the testability problems of analog circuit, and result shows that the testability problems of analog circuit can be resolved effectively without any other complex numerical computation.

Key words: - k-fault diagnosis; fault diagnosis; fault verification; analog circuit; K-node method ; K-branch method; testability;

1. Introduction

Diagnosis is a common behaviour in our daily life. Every system may be affected by faults. Whenever we think about why something does not behave as it should, we are starting the process of diagnosis. Generally speaking, a fault is any change in a system that prevents it from operating in the proper manner [1]. Diagnosis is defined as the task of identifying the cause and location of a fault by feasible methods. This is conceptually divided into two main phases: the fault detection phase and the fault isolation phase. In the fault detection phase, the system is characterized as faulty. The faulty elements or regions are identified in the fault isolation phase. By a fault, we mean any change in the value of a circuit element with respect to its nominal value that can cause the failure of the system performance.

The following figure 1 expresses the general structure of a diagnostic system. Signals x(t) and y(t) are input and output of the system, respectively. Faults and disturbances also affect the test of the system. Here denoted as the ‘‘Process’’. The values of these errors are not known. The diagnostic system’ task is to produce a diagnostic statement S, including the information about fault modes that can explain the behavior of the Process. But the diagnostic system is assumed to be passive. In other words, it can not affect the Process itself.

The whole diagnostic system can be divided into

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several parts that are also diagnostic systems named D_i. It is assumed that each of them produces diagnostic statement Si. This decision is to combine all the information and then form the entire diagnostic statement S.

The number of possible faults in a system may be large and can be located everywhere in the system. To diagnose in such conditions one frequently uses hierarchical approach where successive diagnostic statements are generated as the level of description of the system is lowered going down towards the fault itself [2].This allows for smaller sets of faults to be considered at a time for the given hierarchical level. Modern automatic test pattern generator may support such concepts [3].

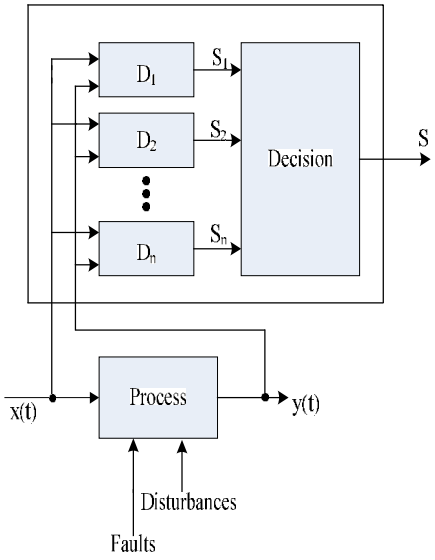

Fig.1 The general structure of a diagnostic system

2. Diagnosis of analog circuits

Fault diagnosis and testing are important for development and maintenance of safe and reliable electronic circuits and systems. According to collected statistics, most part of an electronic system is digital (about 80%), but about 80% of the faults occur in the analog segment [4]. Although the techniques for digital circuits' diagnosis and testing have been mature, while the diagnosis and testing on analog circuits are evolved very slowly.

Fault diagnosis of analog circuit is still an active research topic in pattern recognition and computer-aided testing area [5] [6] .The advent of modern, complex integrated circuits and systems creates and enhances many research works in these areas.

In general, faults are categorized into two classes, catastrophic faults or hard faults are the opens or shorts of faulty elements, and deviation faults or soft faults are often referred to the parameter deviation [7]. Large deviation faults are due to the deviation of about 50% of the faulty element(s) from their nominal value(s). Hard faults are relatively easy to detect because they often produce totally unwanted results.

Fault diagnosis of analog circuits is a difficult problem. This difficulty is due to several reasons such as:

1. There are nonlinearity problem and feedback loop in analog circuits, it sharply increases the difficulty of the diagnosis.
2. The inaccuracy in circuit measurements besides the inability of measuring current without breaking the circuit connections.
3. The parameters of analog elements are usually continuous, which can change from zero to infinitude, it is impossible to define any unified fault model for them.
4. The limited accessibility to circuit nodes especially in modern integrated circuits.
5. The lack of good fault models since analog circuits have a continuum of possible faults.

Since the 1970s, analog circuit fault detection has become an active research area, and significant research results have been achieved.

Starting with the basic research reported in [8] and [9] several ideas were reported. In [10] the fault location phase is considered as an optimization problem where the parameter value is searched for in order to minimize the difference among the actual and simulated response. Linear circuits in the frequency domain are considered being characterized by symbolic functions [11].

In Ref. [12], a dictionary method based on the principle of branch screening is introduced, branch set screening currents are obtained as fault features. Although the fault features are hard to get by simulation, the proposed fault diagnosis method can be used to diagnose soft fault of nonlinear analog circuits. In order to diagnose multiple soft faults in the same type of circuits the Woodbury formula was applied to the modified nodal equation to construct the so called fault equation in [13].

A new fault dictionary approach for linear analog circuit is presented in Ref [14] .

Based on the ingenious idea of Ref [14], Ref [15] firstly developed the method for diagnosis soft faults of tolerance analog circuits and nonlinear circuits; while Ref [16]. constructed a new dictionary method based on a theorem named conservation of node voltage sensitivity weight sequence.

In one approach, small parameter changes were allowed in nonlinear circuits [17].

A decomposition method was proposed in [18] aiming to cope with circuit complexity.

Reference [19] presented a fault diagnosis method based on wavelet-neural network, whose fault features are extracted by circuit simulation, after data processed by wavelet-neural network.

Reference [10] tried to diagnose the faults of linear analog circuits based on transferring *pi*-loci from a plane to three-dimensional (3-D) or four-dimensional (4-D) spaces, the fault feature is the relation of input and output (transfer function), which is often nonlinear and hard to obtain but can be used for double-fault diagnosis.

A low-noise amplifier was diagnosed in [20] by using digital signatures suitable for built-in self test design concepts. Hard and soft faults were diagnosed the former modelled as resistors having convenient values

In [21] method based on fault trajectory concept for fault diagnosis of analog linear continuous time networks, which relies on evolutionary techniques, where a genetic algorithm (GA) was coded to optimize test vector generation, was reported.

3. k-fault diagnosis

k-fault diagnosis has great significance in the development of analog circuit fault diagnosis process. The appearance of k-fault diagnosis made the fault diagnosis for analog circuit from the early fault dictionary method and parameter identification method to verification method.

The method changes the parameters of fault element into fault current, while the numbers of the faults in the network are limited among k. Therefore, the parameter to be verified is fault current. If the fault current is 0 that means no fault, or there is a fault. The method makes use of the changes of the parameters of fault elements, and the relationship of voltage and current changes in the amount of the nodes detectable. It realizes the location by verifying the compatibility of the fault diagnosis equation.

There are a important hypothesis in k-fault diagnose that the effects of the faults can't be offset each other. The parameters of fault elements are usually continuous, so the probability of offset is very small. In other words, the hypothesis is feasible.

Many k-fault diagnosis methods were put forward such as branch method, node method, loop method, mesh method, cut set method [22]. These methods diagnose the circuits directly by the equation of k-fault diagnosis under a single model. In order to conduct further studies on the k-fault diagnosis theory, it is necessary to carry out unified mathematical model of k-fault diagnosis theory, and use them to deal with the tolerance effect as well as non-linear and design-for-test issues

In the k-fault diagnosis, the content which should be verified such as [23]:

1) The number of the fault elements is not more than k;
2) If the number of the fault elements is not more than k, the fault elements should be determined.

If the above mentioned can be verified in the network N, then we can say the network N can be k-fault detected.

3.1 fault current model

Set of fault current sources in a branch circuit can be showed by vectors as follows:

$$I_{sf}=\begin{bmatrix}\Delta Y_1(V_1+V_{f1})\\ \Delta Y_2(V_2+V_{f2})\\ \mathrm{M}\\ \Delta Y_b(V_b+V_{fb})\end{bmatrix} \quad (1)$$

To any branch k in circuit, $I_{sfk}=\Delta Y_k(V_k+V_{fk})$. Where k is an integer, and $1\le k\le b$.b is the number of branches in circuit. I_{sfk} means the fault current value of K-th branch. ΔY_k means the admittance increment of K-th branch. V_k means the normal voltage. V_{fk} means the voltage increment when faults exist. The following figure 2 expresses the current model of active and passive branches.

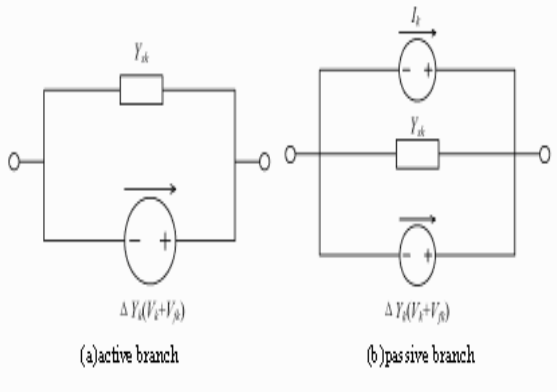

Fig. 2 form of fault current source

If the fault current source of one branch is 0, then no fault exist in this branch. If the fault current source of one branch is not 0, then one fault or many faults exist in this branch and the branch will be called fault branch [24].

In the circuit network, nodes are produced because of some branches. The cut sets are produced by a number of collections of some branches which are cut Therefore, in circuit the sufficient and necessary condition for any node (cut set) without fault is the branch fault current related to the node (cut set)is 0. If the fault current of a node (cut set) is not 0, it means that at least one of the branches related to the node (cut set) has one fault or many faults. The node (cut set) is called fault node (cut set).

3.2 Mathematical model of k-fault diagnosis theory [25]

More generally speaking, we can get the mathematical model [26] :

$$\mathbf{AX=B} \tag{2}$$

Where $\mathbf{A} \in \mathbf{C}^{m\times d}$ and **A** means coefficient matrix of various diagnosis equation. In other words, it's the transfer admittance and transfer impedance in circuit. $\mathbf{B} \in \mathbf{C}^{m}$ and **B** means current (voltage) increment matrix which can be obtained by measuring after faults appear in the network N. $\mathbf{X} \in \mathbf{C}^{d}$ and **X** means various fault model of excitation source. **X** is unknown and non-zero vector in **X** means the location of circuit fault occurs.

In the equation, d numbers are unknown but m equations exist. So normally it should have infinitely solutions. But the main purpose of fault diagnosis is to determine the fault location, so in order to determine whether there is any fault in circuit only needs to see whether the fault excitation source is zero. Consequently, the question of fault location will convert to the question of non-zero which is verified in the component about fault excitation source. The equations have infinitely non-zero solution, so fault component can not be confirmed. But if the number of fault in the network is limited to k, a special solution of the equations can be got [27].

4 An improving k-fault diagnosis method and application example

4.1 K-node fault diagnosis

In the k-node fault diagnosis, node whose fault current is not 0 must be verified firstly, and then make sure of the fault node. At last by using node fault current to determine the fault branch (or component) [28]

4.1.1 An improving algorithm of the K-node method

As shown in Figure 3, a linear network N has b branches and n nodes (with the exception of public nodes). M nodes are accessible.

Because of the principle of network analysis we can get

$$\mathbf{Y_n V_n=I_n} \tag{3}$$

Where $\mathbf{Y}_n$ is the admittance matrix of a network named **N**. $\mathbf{V_n}$ and $\mathbf{I_n}$ are node potential vector and node exciting current vector.

If the network **N** breaks down into **N+ΔN** and its admittance changes into a matrix Yn+ΔYn, we can get

$$(\mathbf{Y_n}+\Delta\mathbf{Y_n})\ (\mathbf{V_n}+\Delta\mathbf{V_n}) = \mathbf{I_n} \tag{4}$$

Where $\Delta\mathbf{V_n}$ is a node potential increment vector.

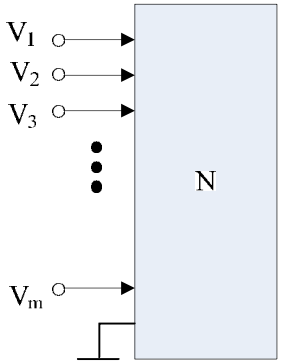

Fig.3 Linear network N

After simplifying we can get

$$\Delta\mathbf{V_n=J_n} \tag{5}$$

In the equation,

$$Z_n=Y_n^{-1}$$

$$J_n=-\Delta Y_n(V_n+\Delta V_n) \tag{6}$$

As the network N only has m ports，so we only can impose current and measuring voltage into these m ports. So

$$I_n = \begin{bmatrix} I_m \\ 0 \end{bmatrix} \tag{7}$$

$$\Delta\mathbf{V_m=Z_{mn}J_n} \tag{8}$$

Where $\mathbf{Z_{mn}}$ is an impedance matrix which is composed of row vector related to accessible ports from Z_n.

The formula is called as K-node (k <m) fault diagnosis equation. In these equations there are several unknown numbers (n), but m (m <n) equations exist, so the equations have infinite solutions.

4.1.2 K-node fault diagnosis steps

This is done using k-node fault diagnosis method as in the following steps:

1. Accessible Nodes of the detectable network **N** are determined. Undirected test graph G_t is drawn. The value of k in the network is affirmed under the condition of accessible nodes.
2. Admittance matrix $\mathbf{Y_n}$ and node impedance matrix $\mathbf{Z_n}$ in the network N are calculated under the condition of the parameters. and in accordance with the n test points to determine $\mathbf{Z_{mn}}$.
   Steps 1–2 are completed before testing.
3. **M** vectors are exerted to stimulate the testing point. **M** voltage response $\mathbf{V_{mm}}+\Delta\mathbf{V_{mm}}$ of the accessible ports are tested. Increment $\Delta\mathbf{V_{mm}}$ is calculated.
4. Whether the numbers of the fault nodes are more than k is searched and verified, or corresponding $\mathbf{T_j}$ is searched to calculate the $\mathbf{Z_{mk}}$ so that the corresponding $\mathbf{Z_{mk}}$ is obtained. Then $\mathbf{J'_k}$ is calculated.
5. Current excitation I_{mn} and fault current J_{nm} are used to calculate node voltage $V_{nm}+\Delta V_{nm}$ in network $\mathbf{N}+\Delta\mathbf{N}$. A suitable column matrix is chosen to calculate $\Delta\mathbf{Y_nS}$.
6. The incidence matrix **A** and $\Delta\mathbf{Y_nS}$ of the network **N** are used to calculate $\Delta\mathbf{Y_b}$. And then the fault components and their parameters are confirmed.

In the above steps Step 4 requires a lot of calculations, and it is also carried out after the test. So it is a defect of the k-fault diagnosis.

4.2 K-branch fault diagnosis

In the k-branch fault diagnosis, branch whose fault current is not 0 must be verified, and then make sure of the location about the fault branch and components [29][30].

When the K-branch comes into being a complete loop or a incomplete loop, more excitations need to impose so that fault branch and components can be confirmed.

4.2.1 An improving algorithm of the K-branch method

K-branch fault diagnosis equation can be calculated from the K-node fault diagnosis equation (8).

$$\Delta\mathbf{V_m}=\mathbf{Z_{mn}}(\mathbf{A}J_b)=(\mathbf{Z_{mn}A})\ J_b=\mathbf{Z_{mb}}\ J_b \quad (9)$$

In the formula (7),

$$J_b=-\Delta Y_b A^T(V_n+\Delta V_n)=-\Delta Y_b(V_b+\Delta V_b) \quad (10)$$

$$\mathbf{Z_{mb}}=\mathbf{Z_{mn}A} \quad (11)$$

The formula is called as K- branch fault diagnosis equation. J_b is the branch fault current vector.

4.2.2 K- branch fault diagnosis steps

This is done using k-node fault diagnosis method as in the following steps:

1. Node impedance matrix $\mathbf{Z_{mn}}$ of the network **N** is calculated, and then the transfer impedance matrix $\mathbf{Z_{mb}}$ is get.
2. The global column rank of the $\mathbf{Z_{mb}}$ is verified to determine the value k. Or at first the value of k in the K-node fault diagnosis is made sure, and then it is approximated to the value k in the K-branch fault diagnosis. More similar approach is to make k = m-1, but this method may lead much error.
   Steps 1–2 are completed before testing.

In fact, value k in K-fault diagnosis is generally small. Usually 2~3 is preferable.

3. 2 excitation vectors are exerted to stimulate the testing ports. IF only one fault needs to be test then only one vector should be imposed. M response $\mathbf{V_{m2}}+\Delta\mathbf{V_{m2}}$ of the accessible ports is tested. Increment $\Delta V_{m2}(\Delta V_{m2}\in R^{m\times 2})$ is calculated.
4. Arbitrary column vector is get from $\mathbf{V_{m2}}$. Whether T_j exists is searched and verified so that the corresponding $\mathbf{Z_{mk}}$ is obtained. Then J'_k is calculated. If the $k \geqq 2$ and the fault branch comes into being a loop，there may be several T_j make r（T_j）=k. At this time one of the groups $\mathbf{Z_{mk}}$ is get to calculated.
5. Whether the branches which correspond to nonzero elements in J'_k may be a loop is checked. If it's impossible, the fault branch can be affirmed at once. If some or all of these branches comes into being a loop, then the branches require more researches.
6. Two column vectors of $\Delta\mathbf{V_{m2}}$ are got by double-excitation method. The actual faults can be affirmed by multi-excitation K- branch fault diagnosis method.

4.3 Application example

Here, an example is demonstrated to show the application of the presented diagnosis method above. The experimental circuit is shown in Fig.4.

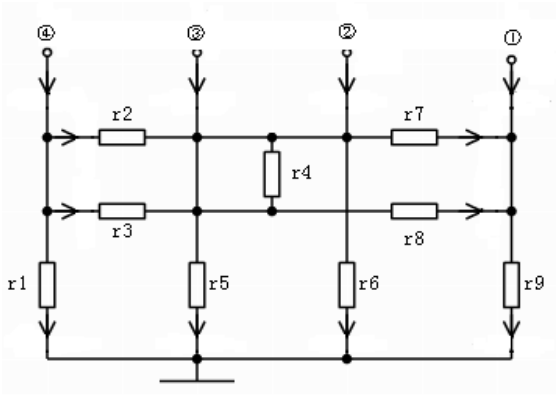

Fig. 4 A practical example

In the above figure, r_i=1Ω(i=1~9). If excitation is imposed on the node 1, node 2, and node 4 which are accessible such as

$$I_{mm}=\begin{bmatrix} I_1 \\ I_2 \\ I_4 \end{bmatrix}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix},$$

Then test increment is

$$\Delta V_{mm}=\begin{bmatrix} \Delta V_{m1} \\ \Delta V_{m2} \\ \Delta V_{m4} \end{bmatrix}=\frac{1}{286}\begin{bmatrix} 6 & 7 & 6 \\ 7 & 1 & 7 \\ 6 & 7 & 6 \end{bmatrix}.$$

If excitation is imposed on the node 1~ node 4 such as

$$I_{mm}=\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}=\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix},$$

Then test increment is

$$\Delta V_{mm}=\frac{1}{47\times 60}\begin{bmatrix} -15 & 76 & -63 & 5 \\ 76 & -175 & 115 & -17 \\ -64 & 115 & -17 & 15 \\ 4 & -19 & 15 & 1 \end{bmatrix}.$$

Here, the fault nodes or components are affirmed by k-fault diagnosis method as follows.

1. By the new k-node method

① Because m=3, k is estimated at 2.

Then

$$Z_{mb}=\frac{1}{15}\begin{bmatrix} 7 & 4 & 4 & 0 & 3 & 3 & 1 & 1 & 2 \\ 3 & -2 & 0 & 2 & 2 & 6 & 2 & 0 & 3 \\ 2 & -1 & -1 & 0 & 3 & 3 & -3 & -3 & 7 \end{bmatrix}$$

② After row transformation the expansive matrix $\begin{bmatrix} \Delta V_{mm} & I \end{bmatrix}$ (where $I \in R^{m\times m}$ is a unit matrix) changes as follows:

$$\frac{1}{285}\begin{bmatrix} 7 & 8 & 7 & 1 & 0 & 0 \\ 0 & -\frac{57}{7} & 0 & -\frac{9}{7} & 1 & 0 \\ 0 & 0 & 0 & -1 & 0 & 1 \end{bmatrix}$$

That is,

$$Q=\begin{bmatrix} 1 & 0 & 0 \\ -\frac{9}{7} & 1 & 0 \\ -1 & 0 & 1 \end{bmatrix}$$

So r ($\Delta \mathbf{V_{mm}}$) =2.Then we can see that there are two independent faults in the network **N.**

③ Then

$$QZ_{mb}=\frac{1}{106}\begin{bmatrix} 49 & 28 & 28 & 0 & 27 & 27 & 7 & 7 & 14 \\ -35 & -53 & -31 & 21 & -3 & 32 & 13 & -7 & 5 \\ -35 & -35 & -35 & 0 & 0 & 0 & -35 & -35 & 35 \end{bmatrix}$$

④ In the third row of $\mathbf{QZ_{mb}}$ we search $\mathbf{W_b}$ so that the fault branches are branch 4, branch 5, and branch 6.

⑤ Because branch 4, branch 5, and branch 6 can come into being a loop, so it needs further researches to affirm actual fault branches by multi-excitation method.

After more calculations we can see the actual fault branches are branch 4 and branch 5.

2. By the new k-branch method

① After verifications we get k=3.

② $Z_{mn} = Z_n = \frac{1}{16}\begin{bmatrix} 6 & 3 & 3 & 2 \\ 3 & 6 & 2 & 2 \\ 3 & 3 & 6 & 5 \\ 2 & 3 & 3 & 7 \end{bmatrix}$

③ After row transformation the expansive matrix $\begin{bmatrix} \Delta V_{mm} & I \end{bmatrix}$ (where $I \in R^{m \times m}$ is a unit matrix) changes as follows:

$$\frac{1}{47 \times 60}\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & -188 & 188 & 0 \\ 4 & -17 & 16 & -1 \end{bmatrix} Q$$

Where

$$Q = \begin{bmatrix} 1 & 0 & 0 & 4 \\ 0 & 1 & 1 & -5 \\ 0 & 0 & 1 & 16 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

④ That is,

$$QZ_{mn} = \frac{1}{15}\begin{bmatrix} 15 & 15 & 15 & 30 \\ 0 & 0 & 0 & -15 \\ 36 & 50 & 53 & 115 \\ 2 & 7 & 7 & 3 \end{bmatrix}$$

⑤ In the first row and second row of QZ_{mb} we search W_n. Because the first column, the second column, and the third column are the same, so the node 1, node 2, and node 3 are fault nodes.

Now the actual fault branches are branch 1, branch 2 and branch 3.

4.4 Testability in analog circuit

Testability is a very useful concept in the field of circuit testing and fault diagnosis， and it includes testability analysis and testability design. In the testability analysis, the testability of the system is tested while the topological structure and accessible nodes of system are known. In the testability design, the topological structure and accessible nodes of system are chosen to make sure that faults of the system are testable [31]. Testability analysis is a specific method and the premise of fault diagnosis. While the method satisfies testable condition the method would be effective.

4.4.1 Requirement of parameters [32][33]

The fault detection rate for a system, is defined as

$$r_{FD} = N_D / N_T$$

Where N_T is all faults occurring in prescriptive time and N_D is the faults detected exactly by prescriptive way under prescriptive condition [34].

Prescriptive time is defined as the time of all faults that are discovered and detected. Prescriptive way includes BIT （built-in test）, ATE （automatic test equipment）, special apparatus, all-purpose apparatus, manual-work detection and the detection together some way. Prescriptive condition is defined as the state, class of maintenance, level of personnel, etc.

The fault isolation rate for the tested object is defined as

$$r_{FI} = N_L / N_D$$

Where N_D is the number of faults which are detected exactly by prescriptive way under prescriptive condition and N_L is the number of faults which are isolated exactly by prescriptive way under prescriptive condition.

Fault detection time, t_{FD}, is defined as the time from fault taking place to fault detected. Fault isolation time, t_{FI}, is defined as the time from fault detected to fault isolated for prescriptive unit.

The false alarm rate is defined as

$$r_{FA} = N_{FA} /(N_F + N_{FA})$$

Where N_{FA} is the time of false alarm and N_F is the sum of real faults.

4.4.2 Testability analysis

A circuit is k-fault testable means that any component k has fault in circuit, we can get the location and the value by the exciters, parameters and voltage of accessible nodes.

The testability analysis is the premise of fault diagnosis. It is also the foundation of the testability design. If the testability analysis doesn't go along effectively, the effective design is impossible.

Topological condition is put forward firstly. G means topological graph of the circuit N discussed. Then a new graph G_o which plays an important role is introduced [35][36] .

Definition. All branches in G between the accessible nodes are deleted, and all accessible nodes are linked together to be a new node o. After that it is named as graph G_o .

l(G) means the number of branches in the smallest loop(including the branches at least) of G,m+1 means the number of accessible nodes. One

branch connectivity of a graph means the minimum of branches need to be removed that let the graph change to be a disconnected graph or trivial graph, and $\lambda(G_o)$ means the branch connectivity of G_o .

Then the algorithm of the testability analysis can be got, and the flow Chart is show as Fig.5 [37].

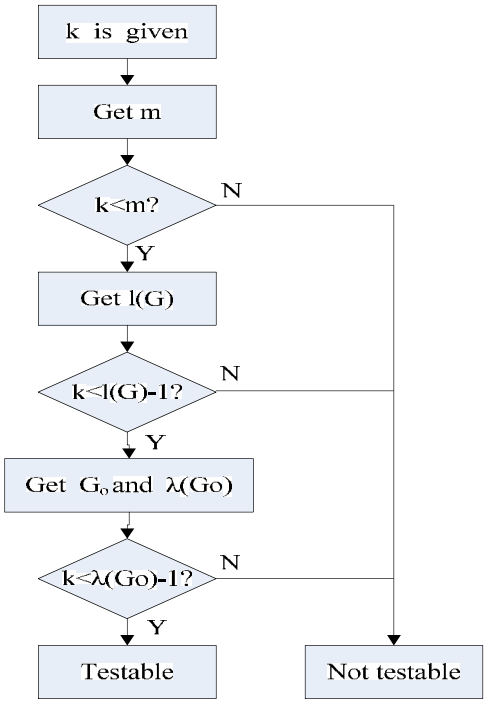

Fig.5 The algorithm of the testability analysis

Obviously, the work of the algorithm lies mainly in l(G) and $\lambda(G_o)$. All the loops need to be found and the smallest one can be found. While the search is finished, the l(G) can be identified.

4.4.3 Testability design[38]

In the K- branch fault diagnosis steps not only single-excitation method but also multi-excitation method would be used under different condition [39].

1) Testability under single-excitation

The value of k is known, in order to design a k fault circuit we just need to satisfy that $m \geqq k+1$, $l(G) \geqq k+2$ and $\lambda(G_o) \geqq k+2$.While value of k is not specified, the circuit designed is hoped to fault testable at most. Therefore, accessible nodes need to be the most in possible. At the same time l(G) and $\lambda(G_o)$ should be large. The value of l(G) has nothing to do with the number and location of the accessible nodes. While the circuit structure is determined, then l(G) is determined.

In the actual design, the number and location of the accessible nodes will be subject to the restrictions of specific issue. At this time an effective method to change $\lambda(G_o)$ is supposing that some nodes have open branches. The approach would work well because open branches have no any effect with the original performance about the circuit. Of course, the setting of open branches should not only be conducive to increasing $\lambda(G_o)$ but also consider that l(G) doesn't become smaller.

In testability analysis, if open branches exist between some accessible nodes, then it's possible to enhance $\lambda(G_o)$ and improve the testability of the circuit.

In the process of testability design, topological structure and the accessible nodes should be close coordination .It may need to adjust repeatedly and then achieve the objective.

2) Testability under multi-excitation

In multi-excitation method, the necessary and almost sufficient condition about k-fault testable is $m \geqq k+1$, $l(G) \geqq k+1$, and $\lambda(G_o) \geqq k+1$. The testability analysis is the same as 4.4.2. Only some conditions change. The design of topological structure and accessible nodes is similar to single-excitation case.

But for a value of k given, the smallest loop branches of G and branch connectivity may be permitted to reduce. Or let $k_m = \min(m-1, l(G)-1, \lambda(G_o)-1)$. So multi-excitation makes restrictions relax, and the testability of the circuit can be improved. At last, the testability design is easier [40].

5 Conclusions

Fault diagnosis is an important part of the analog circuit design. In this paper an improving algorithm is presented. Consequently, in the examples we can see the workload of the verification can reduce.

On the other hand, for the testability problems of analog circuit, testability analysis and testability design are researched under prescriptive condition. Result shows that the testability problems of analog circuit can be resolved effectively without any other complex numerical computation.

The methods the testability problems of analog circuit can be used for diagnosis of electronic circuits in conventional testing systems and neural networks. They may be also useful in parameter identification measurements of other multi-parameter objects modelled by electrical circuits.

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