Variable Lateral Silicon Controlled Rectifier as an ESD Protection

PETR BETAK, VLADISLAV MUSIL
Department of Microelectronics, FEEC
Brno University of Technology
Údolní 53
CZECH REPUBLIC
petr.betak@phd.feec.vutbr.cz

Abstract: - The Variable lateral Silicon Controlled Rectifier (VLSCR) is a SCR based structure with the possibility to tune I-V snapback characteristics. This effect is important for an ESD (electrostatic discharge) protection design. The ESD protection structures act as a protection of integrated circuits against parasitic electrostatic discharge. Among often used structures belong structures having snapback type of I-V characteristic. Typical is a gate-grounded NMOS transistor [3] or a SCR [3]. This text is dealing with the VLSCR structure which enables I-V snapback characteristics tuning according to the application demand. Simulated technology was 0.5µm CMOS very high voltage (VHV Integrated Circuits). Measurement was done in 1.5 µm BiCMOS process.

Key-Words: - ESD, SCR, LVTSCR, VLSCR

1 Introduction

Fig.1 illustrates a principal connection of some ESD protection cells and required I-V behaviour. A random ESD stress goes through the ESD clamps to ground and a core circuit is not endangered. The protections must be active only during the ESD event.

The typical snapback I-V characteristic is shown in Fig.2. The required snapback protection device should fulfil subsequent conditions: the value of a leakage current is low, the ESD current in the area of the snapback is high, robustness of the ESD cell is sufficient. An important feature of the ESD structure is trigger voltage adjustability and holding voltage adjustability. For the ESD protections design the holding voltage adjustability and the trigger voltage adjustability is the key to form required I-V characteristic. The voltage triggered ESD clamps are based mainly on diodes and they are often used as power clamps [3]. The power clamps need to have a voltage reference upon $V_{DD}$ level otherwise a power supply could short out.

Fig.2 Snap-back I-V characteristic of common ESD device.

Nevertheless, the diode string for the supply clamps has several disadvantages like high resistances and slow performance. The ideal ESD protection structure is a Silicon Controlled Rectifier (SCR) for the sake of its quick performance, but the problem is in the high trigger condition (approximately 40-50V) and low holding voltage (~1V)[2]. This limits the application of SCR as a power supply protection. However, there is a way to design the SCR having better triggering and higher holding voltage. The first approach was introduced as a Modified Lateral SCR [2]. The trigger voltage is determined by N-well to a P-substrate breakdown. In MLSCR is inserted the $N^+$ diffusion in $N$-well to
decrease the trigger voltage. But the holding voltage in the MLSCR is still too low. The first power–supply–adjustable–SCR-based structure was introduced by Chatterjee [1]. The structure was termed as “Low Voltage Triggering SCR (LVTSCR)”.

2 Conventional LVTSCR (low voltage-trigger Silicon Controlled Rectifier)

The LVTSCR structure uses a MOS transistor in parallel with a SCR. Therefore, the triggering condition is set on the MOS breakdown level (in the submicron CMOS process approximately 10-15V) and the holding voltage level is given by $X$ and $L$ dimension.

The dimension $L$ (Fig.3) represents a length of $NPN$ base region in the SCR structure. By changing $L$, the current gain of the parasitic bipolar transistors is changed. This yields different $I$-$V$ characteristics. The dimension $L$-$X$ represents a size of $N^+$ diffusion. This diffusion changes the concentration in $N$-well region. Usually the higher is $X+L$, the higher is holding voltage. Formula (1) determines a latch-up condition [2].

$$\beta_{npn} \cdot \beta_{pnp} \geq 1 \quad (1)$$

$\beta_{npn}$ and $\beta_{pnp}$ are the current gains of the $NPN$ and $PNP$ transistors. However, the collector of one is the base of the other. Therefore, it is not possible to use the discrete $\beta$ when computing Equation (1). The illustration in Fig.5 introduces a typical behaviour of LVTSCR as the function of sizes $L$ and $X$. It is evident that the higher is size $L$, the higher are holding voltage and “ON” resistance. The trigger voltage is almost constant. The 0.5µm CMOS technology provides a trigger condition at 14.9V.

The LVTSCR was simulated in a TCAD device simulator to verify declared performance [2, 4].

The Fig.3 shows the LVTSCR structure of a conventional primary ESD protection. Fig.4 illustrates a circuit scheme of the structure.

![Cross section of the LVTSCR structure](image)

**Fig. 3: Cross section of the LVTSCR structure.**

![Circuit scheme and connection of the LVTSCR structure](image)

**Fig. 4: Circuit scheme and connection of the LVTSCR structure.**

The Fig.5 shows the LVTSCR structure of a conventional primary ESD protection. Fig.4 illustrates a circuit scheme of the structure.
LVTSCR structure is not adjustable for higher holding voltages (for example to protect 10V, 15V, 30V as a supply clamp). The reason is the grounded MOS gate which sets the trigger and the holding voltage level close to the MOS breakdown.

![Thermal-voltage dependence for N-type LVTSCR](image)

**Fig. 6:** Simulated thermal-voltage dependence of the LVTSCR structure.

But according to the Fig.6 is possible to say that the LVTSCR structure has big robustness against second destructive breakdown. The Fig.6 shows simulation results of the thermal-voltage dependence. We can see that the thermal breakdown starts at 850 K. This can be also seen in Fig.7 and in Fig.8. The figures show the simulation results from the HBM test and there is a comparison of the LVTSCR structure with conventional lateral SCR.

![HBM test for LVTSCR](image)

**Fig. 7:** The simulated HBM test at the LVTSCR structure.

It is evident that the LVTSCR structure is more effective than LSCR especially when using in advanced CMOS processes. However, due to its higher voltage limitation and trigger voltage adjustability limitation the new structure called Variable lateral Silicon Controlled Rectifier was developed to improve these features.

### 3 Variable lateral Silicon Controlled Rectifier

The Variable lateral Silicon Controlled Rectifier is a structure that enables tuning of its performance according to the requirements. First of all focusing on the semiconductor physics is needed. The conductivity of a semiconductor \( \sigma \) is given by:

\[
\sigma = nq\mu_n + pq\mu_p
\]  

(2)

where \( \mu_n \) and \( \mu_p \) are the electron and hole mobilities and \( n \) and \( p \) are the electron and hole concentrations, respectively. \( q = 1.602 \times 10^{-19} \), \( C \) is the electronic charge, \( n \) and \( p \) are given by the equations:

\[
n = n_i \exp \left( \frac{q(\psi - \Phi)}{kT} \right)
\]

(3)

\[
p = n_i \exp \left( \frac{q(\phi - \psi)}{kT} \right)
\]

(4)

\( \psi \) and \( \Phi \) are the potentials corresponding to the Fermi energy, \( E_F \) and the Fermi energy for the intrinsic semiconductor, \( E_i \), respectively.
Hence, $\Phi = -E_F/q$ and $\psi = -E_i/qn_i$ is the intrinsic carrier concentration given by:

$$n_i = \sqrt{N_C N_V} \exp \left( \frac{-E_i}{2kT} \right) \quad (5)$$

where $N_C$ and $N_V$ are the effective density of states in the conduction and valence bands, respectively.

For silicon, we get:

$$n_i = 1.69 \times 10^{19} \left( \frac{T}{300} \right)^{3/2} \exp \left( \frac{-E_i}{2kT} \right) \quad (6)$$

In $N$-type resistors at low injection current levels, the current density is given by:

$$J = J_n = N_B q\mu_E E = N_B qv_d \quad (7)$$

As the hole current is negligible, $N_B$ is the background doping concentration and $E$ is the electric field, $v_d = \mu E$ is the drift velocity of carriers. As the voltage is increased $E$ increases and so does $J$ and the resistor is ohmic, that is, it shows a linear dependence between current and voltage. As the voltage is raised further the field increases and so does $J$ in accordance with Equation (7) until at $E = 10^4 \text{ Vcm}^{-1}$ the electron drift velocity saturates at $v_{es} = 10^7 \text{ cm s}^{-1}$. Further increasing the voltage serves only to increase the electric field with no increase in $J$ and

$$J = J_{sat} = N_B qv_{es} \quad (8)$$

$J_{sat}$ is a function of the doping concentration and will not be observed for either low $N_B(<10^{14}\text{cm}^3)$ or very high doping levels when $N_B \sim 10^{20}\text{cm}^3$. N-well resistors with $N_B \sim 10^{17}\text{cm}^3$ will have $J_{sat} \sim 10^5 \text{ Acm}^{-2}$, which translates to a current of about 10 mA in a 20 $\mu$m wide resistor.

The high current $I-V$ curve for a 20 $\mu$m wide $N$-well resistor is shown in Fig.9. As the voltage is increased even further in the saturation region, the $E$-field eventually reaches the impact ionization threshold and holes are generated. When the generated hole current becomes large enough to contribute to the total current the voltage decreases and a negative resistance or $snapback$ characteristic is observed as shown in Fig.9. A rough calculation of the maximum voltage across the resistor may be done by assuming that impact ionization begins at $\sim 150 \text{ kV cm}^{-1}$. Then the maximum voltage for a length of 2 $\mu$m is 30 V. The amount of impact ionization required to cause $snapback$ depends on $N_B$, which would influence the maximum voltage across the resistor before $snapback$ occurs.

**Snapback** in the resistor could also occur due to the heating in the saturation region. For more highly doped resistors, self-heating is more likely to result in $snapback$ than avalanche breakdown. Analytical studies and simulations have also shown that current constrictions in the resistor may occur in the negative resistance region.

It is obvious that the more concentrated is $N$ or $P$ region the faster $snapback$ occurs. The feature is important for designing structures based on SCR.

Consider the reverse-biased $PN$ junction. The current through the junction can be calculated:

$$I_B = \frac{qADN_e N_v}{L_e N_B} \exp \left( \frac{-E_i}{kT} \right) + \frac{qW}{\tau_e} \sqrt{N_e N_v} \exp \left( \frac{-E_i}{2kT} \right) \quad (9)$$
Fig. 10: Current in a reverse-biased junction, $I_R$, as a function of temperature. The diffusion dominated region where $ln(I_R)$ is proportional to $1/kT$ is observed at higher temperatures, and the generation-dominated region where $ln(I_R)$ is proportional to $1/2kT$ is observed at lower temperatures [2].

Fig.10 shows a plot of $ln(I_R)$ as a function of $1/kT$. At low temperatures $I_R$ will dominated by the thermal generation, and shows a slope of $\frac{1}{2}$. At higher temperatures, the diffusion current dominates and $I_R$ has a slope of 1. As the reverse voltage is increased and the electric field across the junction approaches $10^5$ V/cm$^1$, the carriers in the depletion region can impart enough energy in a collision with the lattice to generate electron-hole pairs, which become free carriers. These new carriers in turn are accelerated, collide with the lattice and create more carriers. The process is known as avalanche multiplication. The hole and electron currents, $I_{p0}$ and $I_{n0}$, flowing into a high field region are multiplied so that the currents exiting the region are:

$$I_p = I_{p0} + \alpha_p I_{p0} + \alpha_n I_{n0}$$ (10)

$$I_n = I_{n0} + \alpha_p I_{p0} + \alpha_n I_{n0}$$ (11)

$\alpha_{n,p}$ are the electron and hole impact ionization coefficients and are temperature dependent. Empirical equation for the impact ionization coefficients for electrons and holes can be written as follows:

$$\alpha_{n,p} = A_\lambda \exp\left(\frac{-B_\lambda}{E}\right)$$ (13)

where $B_\lambda = E_r/q\lambda$ and $\lambda$ is the mean free path of the carrier.

$$\lambda = \lambda_0 \tanh\left(\frac{E_{r0}}{2kT}\right)$$ (14)

$\lambda_0 = 50A$ and $E_{r0} = 50meV$ are $\lambda$ and the optical phonon energy, $E_r$, at $T = 0$ K. A reasonable fit to experimental results has been obtained by using:

$$\alpha_{n,p} = A_i \exp\left(\frac{-B_i(T)}{E}\right)$$ (15)

Where the coefficient $A_i$ remains constant as a function of temperature and the major variation with temperature is assumed to occur in the exponent $B_i(T)$. The multiplication factor for holes and electrons, $M_{n,p}$, is an important parameter in applying impact ionization models to device behavior.

$$M_{n,p} = \frac{I_{n,p}(\text{out})}{I_{n,p}(\text{in})}$$ (16)

$I_{n,p}(\text{out})$ and $I_{n,p}(\text{in})$ define the currents at the edges of the depletion region. For $\alpha_n \sim \alpha_p - \alpha$, $M_{n,p}$ can be written as

$$M_{n,p} = \frac{1}{1 - \int_0^\alpha \alpha dx}$$ (17)

Avalanche breakdown occurs at the voltage when $M_{n,p}$ approaches infinity, that is:

$$\int_0^\alpha \alpha dx = 1$$ (18)

Empirically, the relationship between $M$ and the voltage across the junction $V_j$ has been described in the form:

$$M = \frac{1}{1 - \left(\frac{V_j}{V_{av}}\right)^n}$$ (19)
where $V_{av}$ is the avalanche breakdown voltage and $n$ is a fitting parameter ranging from 2 to 6 depending on the type of junction being considered. The increase in $M$ with applied voltage is very sharp as $V_j$ approaches $V_{av}$. Another approach is to substitute for $\alpha$ from Equation (15) in Equation (17), to give:

$$M = \frac{1}{1 - A_i \exp\left(-\frac{B_i}{V_j}\right)}$$

(20)

The fitting parameters $A_i \sim A_{x_d}$ and $B_i \sim B_{x_d}$ provide better empirical matching over a range of $V_j$ compared to Equation (19), especially when comparing graded and abrupt junctions. As $V_j$ approaches $V_{av}$, $M$ approaches $\infty$, and Equation (20) can be written as:

$$V_{av} = \frac{B_i}{\ln(A_i)}$$

(21)

This equation can be used to $A_i$ and $B_i$ if $V_{av}$ is already known. The only limiting factor is the resistance of the neutral regions outside the depletion region. The temperature dependence of $\alpha$ is such that as $T$ increases, the impact ionization decreases and $M$ goes down, which means that the avalanche breakdown voltage increases with temperature.

To achieve a better holding and also trigger voltage adjustability a variable lateral SCR (VLSCR) was formed in $N$-well. This structure utilizes $N^{++}$ diffusion between anode and cathode to change the $N$-region concentration for the trigger voltage tuning as was discussed at the beginning in the MLSCR [2]. To change the holding voltage we must manipulate with the $P$-region and the anode-to-cathode spacing as it is shown in Fig. 11.

The Cross section of VLSCR is described by the dimensions $X$, $Y$ and $L$, where $L$ represents the anode-to-cathode spacing and it affects the base length of $PNP$ transistor. The size $Y$ is the $P$+ region extension and it changes the base length of $NPN$ transistor. Finally, $X$ is the size of $N^{++}$ diffusion to change the trigger voltage. The principal circuit scheme of this structure is presented in Fig. 12. The dimensions of the diffusion regions also influence a value of the $P$-region and the $N$-region resistances which are illustrated in the scheme.

Fig. 12: Circuit scheme of SCR-based structure termed as VLSCR

Manipulating with the sizes $X,Y$ the current gains of the $NPN$ and $PNP$ transistor are changed in the way that was discussed earlier and it corresponds with the avalanche conditions according to the equation (21). The Fig 13 presents the simulated $I$-$V$ characteristics of the structure.

According to the graph, the holding voltage adjustability is 17 V-31 V and the trigger voltage
adjustability is 25 V - 57 V. This behaviour is applicable for the high voltage supply clamps. But the behaviour depends on the $P+$ anode resistance. If we use a different $P+$ anode concentration, we get different $I-V$ characteristics. The same VLSCR structure but with a different $P+$ anode concentration is illustrated in Fig. 14.

![Fig. 14: Cross section of VLSCR with $P+$ anode](image)

This structure setting yields different voltage levels in $I-V$ characteristics as seen in Fig.15. In this case, the used voltage at VLSCR or LVTSCR structures is similar. Therefore, the convenient $P+$ anode concentration has to be chosen.

![Fig.15: Simulated $I-V$ characteristics in 0.5µm CMOS process (TCAD device simulation).](image)

Fig.15: Simulated $I-V$ characteristics in 0.5µm CMOS process (TCAD device simulation).

Fig.16 shows measurement results of a VLSCR structure which was manufactured in 1.5µm BiCMOS technology. It is shown that the holding voltage adjustability is approximately from 20 V to 42 V. Trigger voltage changes from 40 V to 60 V.

![Fig.16: Measurement results of VLSCR manufactured in BiCMOS 1.5 µm process.](image)

A cross section of a VLSCR structure manufactured in BiCMOS is shown in Fig.17. To improve adjustability of the holding and trigger voltage, it would be convenient not to use constant $X$ and $L$ setting. BiCMOS technology provides a low doped epitaxial layer and therefore the voltage levels of $I-V$ characteristics are relatively high. In a common CMOS process, the voltage levels are relatively low and the “ON” resistance is better. Fig.18 illustrates a voltage variability of the VLSCR in the 0.5µm CMOS process from the TCAD device simulator.

![Fig.17: Cross section of VLSCR structure manufactured in BiCMOS](image)

![Fig.18: Comparison of different P+ anode concentration, TCAD simulation results](image)

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Also the thermal-voltage dependence was simulated and the results are shown in Fig.19. We can see the simulated performance is similar like at the LVTSCR structure. This means the performance is quite effective. The thermal breakdown starts at 850 K depending on the voltage level. The lower is voltage the higher temperatures can VLSCR withstand.

Fig. 19: The simulated thermal-voltage dependence at the low doped VLSCR structure.

The same dependence but for the structure with more concentrated VLSCR anode is shown in Fig.20. Here, we can see again very similar results like at LVTSCR structure, but the VLSCR results have better performance. Heating of this structure is not as progressive as at the LVTSCR structure.

Fig. 20: The simulated thermal-voltage dependence at the high doped VLSCR structure.

Very important are the results from HBM test. (Fig.21, Fig.22, Fig.23) Here, we have comparison of the both VLSCR structures with the conventional lateral SCR. The significant advantage of the VLSCR is that the temperature during HBM test does not reach as high as at the LSCR structure. Also the falling progress of the maximum temperature at the VLSCR is reasonable. The conventional lateral SCR embodies worse maximum temperature falling progress.

Fig. 21: The simulation results of the HBM test for conventional lateral SCR structure.

Fig. 22: The simulation results of the HBM test for the low doped VLSCR structure.

Fig. 23: The simulation results of the HBM test for the high doped VLSCR structure.
4 Conclusion

The Variable lateral Silicon Controlled Rectifier seems to be useful in the high voltage integrated circuits but even in low voltage applications. The significant advantages of this structure are holding voltage adjustability and trigger voltage adjustability. That means the designer can set the layout dimensions exactly according to the required ESD protection performance. The new VLSCR structure can be formed in CMOS process as was simulated or even in BiCMOS processes as was manufactured and measured.

We can see the performances are very similar even we used different technology. Also other verifications were done and are commented above in the text. The thermal-voltage dependence embodies sufficient behaviour. And the results from the simulated HBM tests proclaim good robustness and efficiency of the new VLSCR structure. The VLSCR structure is convenient for low voltage applications in CMOS process but even for higher holding voltages in BiCMOS process. In the ESD protection design the VLSCR can form a supply clamp or a primary ESD protection. The layout example of the VLSCR

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**Fig. 24:** Simulated $I$-$V$ characteristics in 0.5µm CMOS process (TCAD device simulation).

The Fig. 24 shows adjustability of the holding and trigger voltages simulated in CMOS process. The Fig. 25 shows the adjustability of the same structure manufactured in BiCMOS.

**Fig. 25:** Measurement results of VLSCR manufactured in BiCMOS 1.5 µm process.

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**Fig. 26:** Layout example of the VLSCR structure in CMOS process.

Positive features and good performance of the VLSCR structure enable to use this kind of ESD protection commercially.
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