Methodical Self Checking and Test Infrastructure Design for Fault Tolerance in Digital Circuits

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Abstract: - During the process of development of any system, system reliability is of utmost importance .Specially when designing a processor, it is desired that a processor function correctly even in the presence of faults .This concept is commonly referred to as fault tolerance. The fault tolerant microprocessor systems used in safety critical applications need to be thoroughly validated during the design stages. As feature size reduces in future, there is an increased probability of transient and intermittent faults. Transient faults can only detected by online detection or concurrent checking and not by testing . Because of continuously shrinking dimensions and voltage levels in near future transient faults will be a major source of errors. Therefore concurrent checking is becoming all the more important and necessary. Now these systems on chip integrated circuits contain both digital and analog cores. Test cost for such mixed signal SOC is much higher than the digital SOC that allows the analog and digital cores to be tested. The analog cores are wrapped such that the test can performed using a digital test access mechanism .In our method , an analog test infrastructure is used which consists of test wrappers and test access mechanism. Test wrappers isolate various modules from their surrounding circuitry during test .So the focus is on optimisation of a unified test access architecture that is used for digital and analogue cores. We wrap each analog core by a pair of digital to analog converter and analog to digital converter .They convert analog core to virtual digital core which allow the use of digital testers to test the analog cores. This reduces the need for expensive mixed signal tester so that there is a reduction in the overall cost. The work demonstrates an implementation of a design methodology for embedding fault tolerant capabilities into high level digital system design.

Key-Words: Fault, Multiplier, Adder, wrapper, carry, ADC , Synthesis, Sampling

1. Introduction

Fault tolerant computing means computing correctly despite the existence of errors in a system. Basically, any system containing redundant components or functions has some of the properties of fault tolerance. A desktop computer and a notebook loaded with the same software and with files on floppy disks is an example of a redundant system. Since either computer can be used, the pair is tolerant of most hardware and some software failures. We propose a methodology which involves methodical testing and developing a test circuit which tests analogue circuit along with the digital circuit. The method starts with a standardised behavioural level system description and systematically transforms it into an implementation level circuit design with fault tolerant parts built in. The transformation process aims to keep the changes made in the model transparent from the viewpoint of the designer, in order to maintain capability between the original system models and to minimise the manual interaction needed to implement fault tolerance. The method is intended to be easily incorporated into existing digital system design environments; therefore it applies the de facto industry standard VHDL language both as input and output format.

After synthesis, we focus on detecting the transient faults. We are aware that with the rapidly shrinking dimensions and the diminishing voltage levels, VLSI circuits are becoming increasingly sensitive to temporary or transient faults. These faults are caused for instance by cross talk, power supply, noise, alpha particles and other reasons. Transient faults can be only detected by online detection or concurrent checking and not by testing [1] .If a transient fault occurs in a node of a combinational circuit, an error occurs if, due to this fault, an erroneous value is captured in a latch [2]. A new self checking array or Wallace tree

multiplier for which in accordance with the described situation and tendencies the combinational part and also the output registers of the multiplier are constantly monitored is proposed.

Now many systems contain analogue and digital core. We demonstrate the feasibility of using analogue wrapper by presenting transistor level simulations for an analogue wrapper and a representative core.

2. Synthesis Description

This work demonstrates an implementation of a design methodology for embedding fault tolerance capabilities into high level digital system models. The method starts with a standardised behavioural level system description and systematically transforms into an implementation level circuit design with fault tolerant parts built in., the method is intended to be easily incorporated into existing digital system environment. The implantation of the fault tolerant capabilities is performed by replacing common VHDL data types with alternate, self checking capable versions. This way the initial high level needs only a minimal modification, and maintains comp ability with high level simulation and verification tools.

2.1 Error Detection at Behavioral Level

On the behavioural level of system modelling, the most common data types are numbers. Both the correctness of the result produced by the system and the control flow of the algorithms themselves depend severely on the integrity of the numeric values. However, numbers are transformed to multi bit data lines at lower level of abstraction, so usual physical level faults (stuck at, ridging etc.) are represented as corrupted values at the behavioural level. Therefore the numeric values of the high level model need to be protected under intentional value changes.There are numerous methods for this purpose. The application of residue codes has attractive advantages: relatively low calculation requirements resulting in low hardware time and / or time overhead in the final implementation . In our experimental system, the simple mod 3 residue code involves the extension of all integer values by a separate residue value that contains its remainder modulo. Additionally, the consistency between the numeric value and the residue must be held during the operations on the integers. This task can be solved in an elegant way in VHDL, due to a certain syntactic properties of the language . As all the VHDL operators are treated basically as functions , a feature called operator overloading is provided. The working of the standard VHDL operators can be redefined by the use , simply by writing the appropriate functions that take the operands as arguments and return the result of the operation.

This feature is demonstrated:

```
Package integer_rescode is
    Subtype res_code is integer range 0 to 3 ;
  Type integer_rc is record
 Value : integer
Rescode : res_caode;
End record;
Function "+" (1, r: integer_rc) return integer_rc;
Function : "_" (1,r: integer_rc) return integer_rc;
R : integer_rc ) return integer_rc;
End integer_res_code;
Package body integer_rescode is
Function rescode (arg :integer ) return res code is variable result : res_code;
Begin
Result := arg mod 3; return result;
End res_code;
Function " +" (1, r: integer_rc) return integer_rc is variable result : integer_rc;
Begin
```

Result.value :=1.value+r.value; if (rescode(1):=invalid_rc;

Else

Result result; end "+";

End integer_rescode;.

2.2 Transformation to Register Transfer Level The embedded fault tolerant features of the behavioural models must be transformed. As high level synthesis systems transform behavioural level operations into predefined low level functional units, this transformation necessitates the reimplementation or modification of FU representing the overloaded operators. So their modification is just as simple as the modification of the behavioural model. The register transfer level equivalent of the integer_recode package was implemented as a straightforward modification of IEEE_1164 std_logic numeric operation package.

2.3 Simulation and Result: Attempts were made to generate a gate level VHDL circuit description from the RT level description According to the targeted implementation architecture, a XILINX FPGA development tool was used to convert the RT level into Xilinx FPGA wiring. The overhead in the number of equivalent gate inputs was 48% with 32 bit wide integers. These values are significantly higher than the expected values according to the literature [5]. The actual overhead value, however, is severely affected by the following factors:

1. The sub optimal implementation of the residue code checker.value c
2. The sample circuit was mostly data dominant, with a very simple control sequence. The FPGA synthesis tool generated the checker as a combinational circuit b, optimised for speed .A slightly slower, sequential implementation would have resulted in a smaller hardware overhead.

3. Self Checking Multi plier

Transient faults can only be detected b y online detection or concurrent checking but not by testing. Also many not modelled permanent faults which are not targeted for stuck at faults are detected. If a transient fault occurs in a node of a combinational circuit, an error occurs .The effect of transient faults in the combinational circuit is limited by the following conditions [2]

To capture an error in a latch there must be a sensitised path from the location of the fault to the latch. There must be a significant duration and amplitude of the faulty signal.
The timing of the transient fault must be such that the erroneous value arrives at the input of the latch.

From these conditions it is clear that the memory part of the circuit is more susceptible to soft errors than the combinational circuit. If a circuit is concurrently checked them it is therefore it is very desirable not only to monitor the combinational part but also the contents of the latches of the circuit.

Because of the continuously shrinking dimensions and diminishing voltage levels in the near future transient faults will be the major source of errors. Therefore concurrent checking is becoming more and more important as well for the combinational part for the latches which are also continuously to be monitored for soft errors. We are interested in concurrent checking for multipliers. Since multipliers form a major part of the chip with many outputs the duplication and comparison is not a good option for concurrent checking of these circuits and more sophisticated solutions have to be developed.

Testing of multipliers and the design of easily testable multipliers are a well investigated area of research. But till now only a few results are known for

the design of multipliers which are concurrently checked.

We propose a new self checking array multiplier for which in accordance with the described situation and also the registers of the multiplier are constantly monitored.

In an array multiplier with input operands a= ($a_{0,}$ $a_{1,}$.....$a_{n-1)}$ and b= ($b_{0,}b_{1,}$.....$b_{n-1)}$ the components a_i and b_j of a and b are processed by an AND matrix. These partial products are added by an array or a tree of carry save adder cells into two operands A and B which are finally added by a conventional adder with carry propagation into the result of the multiplication.

The general ideas for a parity checked multiplier design were developed in [8,9,10]. According to these ideas both the carry save adder and the final adder of the multiplier are partially checked. But even errors in the output registers due to soft errors cannot be detected by this method.

We implement the adder cells of the carry save adder as carry dependent sum adders with a single carry out signal only. The consecutive bits of the input operands of the multiplier are exclusive ORed . The AND matrix determines the n^2 partial product .The partial product are added according to their corresponding bit positions by a parity checked carry save adder into two operands A and B which are finally added by a code disjoint self checking sum bit duplicated adder into the final result P= ab and into the inverted sum NP= NOT (ab). The parity checked carry save adder is implemented either as an array or a tree with full and half adder cells.

The parities p_a and p_b of the input operands of the multiplier a and b are connected by an AND matrix. The parity p_c of the carry out signals of all the adder cells of the carry save adder is determined by the XOR tree of the corresponding carry out signals. The operands A and B are input operands of the final code disjoint self checking sum bit duplicated adder.

By comparing the input parity of the adder and the XOR ed sum of the propagate signals of the final adder as well as the propagate signals of the disjoint sum bit duplicated adder are checked. Therefore sum bits and the inverted sum bits of the adder cells of the final adder can be implemented under the assumption that the corresponding propagate signals are already checked.

3.1Test Optimisation

Once the chip has been subjected to formal verification , the test requirements are imposed on digitisation of the analogue signals to maintain certain test accuracy for the analogue core. We focus onathe optimisation of a unified test access architecture that is used for both analog and digital cores. We formulate a global test resource optimisation problem for the entire SOC, instead of treating the digital and analog portions separately.

We wrap each analog core by a pair of digital to analog convertor (DAC) and analog to digital convertor (ADC) data convertors and digital test configuration circuit. Analog test wrapper reduce test cost in two ways:

1. They convert analog cores into virtual digital cores which allows the use of digital testers to test the analog cores. This reduces the need for expensive mixed signal testers therby resulting in significant test cost reduction.

They allow a unified modular test methodology that results in a substantial reduction inthe test application time.
3.They convert analog cores into virtual digital cores , which allows the use of digital testers to test the analog cores..This reduces the need for expensive mixed signal testers thereby resulting in significant test cost reduction.
They allow a unified modular test methodology that results in a substantial reduction to the problem of test infrastructure design in the given test application time.
We present the problem of test infrastructure design for the modular test for digital circuits.
An analog test wrapper can translate the sampled analog test stimuli into continuous analog test signals for the analog core [13, 15]. Similarly, the analog test responses can translated into digital responses by the wrapper to be analysed by the digital ATE. The test information for a wrapper analog core includes only digital test patterns. Thus, the wrapper converts the analog core into virtual digital core with strictly sequential test patterns which are digitised analog signals. In the normal mode of operation, the analog test wrapper is transparent .The primary I/O pins of the analog core are directly accessible in this mode. In contrast, in the test mode, the primaries I/O are connected to the data converters. The ATW has two In order to utilise test resources efficiently, the analog wrapper needs to provide sufficient flexibility in terms of required resources with respect to all the test needs of the analog core. One way to achieve this uniform test access scheme for analog cores is to provide an on chip ADC-DAC pair that can serve as an interface between each analog core and its digital surroundings.

Analog tests are provided by the core vendor to the system integrator. In case of analog testers, these signals are digitised at the high precision ADC-DAC of the tester. In case of on chip digitisation, the analog wrapper needs to include the lowest cost data converters that can still provide the required frequency and accuracy for applying the core tests. Thus on chip conversion of each analog test to digital patterns imposes requirements on the frequency and resolution of the data converters of the analog wrapper. Thus, the on chip implementation of data converters can be used for a wide range of low frequency audio applications [10, 11, 12]. These converters need to be designed to accommodate all test requirements of the analog core.

Fig 2 shows the block diagram of the proposed analog wrapper that can accommodate for each test all the mentioned requirements. The control and clock signals generated by the test control circuit are highlighted. The registers at each end of the data converters are written and read in a semi serial fashion depending on the frequency requirement of each test. The digital test control circuit selects the configuration for each test. This configuration includes the divide ratio of the digital TAM clock, the serial to parallel conversion rate of the input and output registers of the data converters and the test modes.

Analog test wrapper modes: test modes: a self test mode and core test mode. Before the ATW is configured in the core test mode, the wrapper data converters have to be characterised for their conversion parameters, such as the non linearity and the offset voltage in the self test mode. The self test mode is enabled through the analog multiplexer at the input of the wrapper ADC. The parameters of the ADC and DAC pair are determined in this mode and are used to calibrate the measurement results. Once the self test of the test wrapper is complete, core test can be enabled by turning off the self test bits. In the test modes, multiple tests can be applied to the core. Each test may have a different frequency and TAM width requirements .For each analog tests, the encoder is set to the corresponding serial to parallel conversion ratio where it shifts the data from the corresponding TAM inputs into the register of the ADC. Similarly, the decoder shifts data out of the DAC register .The update frequency of the input and output registers is fupdate=fs*cr where fs is he sampling frequency. The serial to parallel ratio cr is chosen such that fupdate is always less than the TAM clock rate. For example, if the test TAM width requirement is 2 bits and the resolution of the data converters is 12 bits, cr= 1/6 i.e. the input

and output registers of the data converters are clocked at a rate 6 times less than the clock of the encoder, and the input data is shifted into the encoder and the decoder at a 2 bits /cycle rate. The complexity of the encoder and the decoder depends on the number of distinct bandwidth and TAM assignments. In order to limit the complexity of the encoder decoder pair, the numbers of such distinct assignments have to be limited.

3.2 Design of Test Converters:

The design methodology includes a parameter translation method that maps the analog core's test specifications to the data converter parameters such as resolution, differential nonlinearity, integral nonlinearity, signal to noise ratio and harmonic distortion. Test requirements are imposed on the digitisation of the analog tests to maintain certain test accuracy for the analog core. In order to utilise ab ADC – DAC pair as an interface mechanism for the analog core, its operational frequency must be within the Nyquist frequency of the data converters. In addition, the data converters must provide adequate resolution to apply and observe the weakest signal given by the core providers. Data converters of 10 bit resolution that can work at several hundred mega hertz are available in the CMOS technology today. An analog test can be represented in terms of a sampling frequency and a number of samples to be taken. The sampling frequency has to be adjusted to meet the Nyquist criterion for the sampling frequency signal components. The numbers of samples are chosen such that atleast several full periods of the lowest frequency signal component are sampled. The numbers of samples are chosen that atleast several full periods of the lowest frequency signal component are sampled. If an contains frequency analog test contains frequencies ranging f_{min} to f_{max} , the sampling frequency f_s is set higher than $2f_{max}$.The test time ha to be long enough to cover at least full periods of the lowest signal, thus , it is to set higher than $2/f_{min}$.obtained from the wrapped analog core.

3.4 Analog Tests:

Test requirements are imposed on the digitisation of the analog tests to a certain test accuracy for the analog core. In order to utilise ADC – DAC pair as an interface mechanism for the analog core, its operational frequency must be within the Nyquist frequency of the data convertors. In addition, the data convertors must provide adequate resolution to apply and observe the weakest signal given by the core providers. Data convertors of 10 bit resolution that can work at several hundred mega hertz are available in the CMOS technology today. Thus the conditions on the frequency and the resolution of the data convertors preclude only RF applications.

An analog test can be represented in terms of a sampling frequency and the number of samples to be taken. The sampling frequency has to be adjusted to meet the Nyquist criterion for the sampling frequency signal components. The number of samples are chosen such that atleast several full samples of the lowest signal component are Sampled.The number of samples are chosen that atleast several full periods of the lowest frequency signal component are sampled.

If an analog test contains frequencies ranging f_{min} to f_{max} , the sampling frequency f_s is set higher than $2f_{max}$. The test time has to be long enough to cover atleast full periods of the lowest signal , thus , it is to be set higher than $2/f_{min.}$.In order to prevent any signal distortion, the analog core requires sampled at uniform intervals. As a result, the analog aignal is sampled at uniform intervals.

3.5 Analog wrapper optimisation: The ADC – DAC pair together with the encoder –decoder pair forms a predominant part of the ATW. The encoder and decoder allow the wrapper to be reconfigured for an asset of different tests. We exploit this feature of reconfigurability to optimise the resource allocation and reduce the overall wrapper area. We propose that an analog wrapper can be designed such that it can support testing of more than one analog core multiplexed in time from one test to another. In the proposed approach, we use the reconfigurability of the analog wrappers to allow the test of multiple analog cores

using a single wrapper. Thus there is overall reduction in the area significantly.

3.6 Case Study: We present implementation details of the analog test wrapper and demonstrate its functionality by applying a test to a wrapped analog core. We design the wrapper using an 8 bit DAC-ADC pair. To demonstrate the accuracy of using digital test patterns to wrapped analog cores, we apply a cut-off frequency test f_c to analog core A .The core is tested for cut off frequency by applying a multi tone signal. The frequency spectrum of the resulting signal is used to extrapolate the cut off frequency of the filter. We compare the frequency spectrum obtained without using a wrapper and doing a direct analog test to that of the test responses obtained from the wrapped analog core.

3.6 Test Cost Optimisation: We define the test cost minimisation problem for a given TAM width W. The objective is to minimise the test cost in terms of test application time and area overhead. We use a previously developed TAM optimisation technique to obtain the test application time. The test cost for a given SOC level TAM width W can be minimised as follows:

The total test cost is expressed as C (W) = wt. Ct (w) +wa.ca, Where wt is the cost weighting factor for the area overhead cost ca.The weighting factors are defined such that wt + wa = 1. The cost of test application time is expressed as ct(w) = 100* T(w)/ Tm(W), where Tm (w) is the test time of the SOC when all the analog cores share a single analog wrapper.

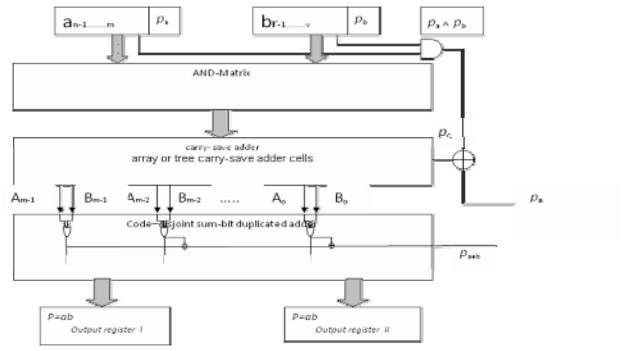

Fig.1 Multiplier circuit

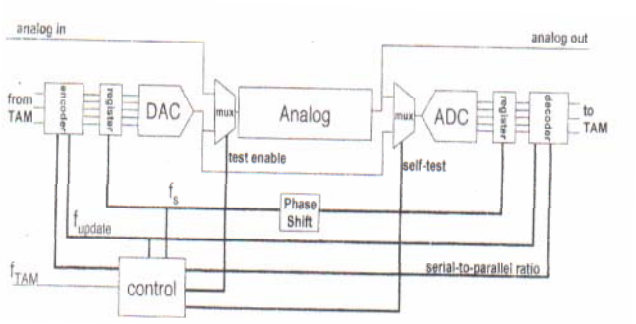

Fig.2 Analog Test Wrapper

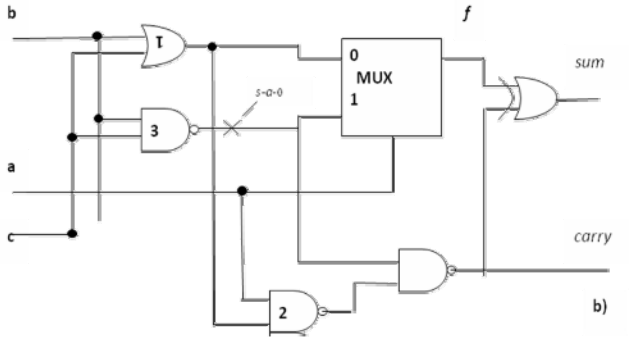

Fig.3 Adder Circuit

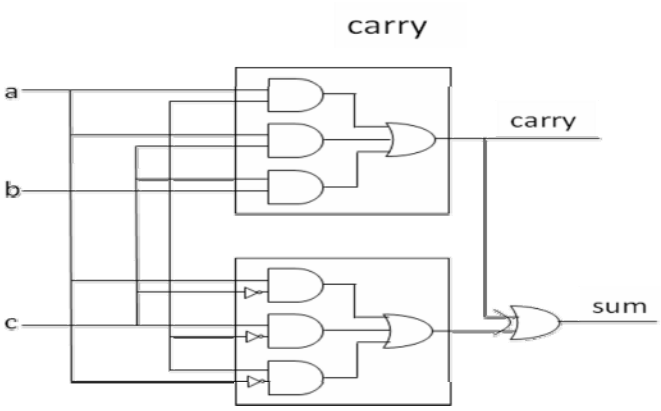

Fig.4 Code Disjoint Duplicated Adder Circuit

Comparison of test time (in clock cycles) in using Analog versus digital bus.

TAM width	SOC p22810m	SOC p34392m	SOC p93791m
24	571823	876014	1438121
32	636113	636113	1032276
40	636113	636113	805659
48	636113	636113	658215
56	636113	636113	636113
64	636113	636113	636113

The results indicate that the use of two analog test busses and a mixed signal tester results in a low.

T(W)

# of wrappers	Wrapper sharing	W=32	W=48	W=64
4	{A,C}	98.3		86.3
	{C,D}	99.1		85.0
	{C,E}	99.1		87.6
	{A,B}	97.5		82.8
	{A,D}	99.1		85.8
	{A,E}	99.1		86.1
	{D,E}	99.1		85.4
3	{A,B,C}	99.8	92.9	90.1
	{A,C,D}	98.3	92.8	87.2
	{A,C,E}	98.3	92.7	86.3
	{A,B,D}	99.1	97.2	85.4
	{C,D,E}	99.1	92.8	85.4
	{A,B,E}	97.9	92.8	82.8
	{A,D,E}	99.1	92.9	85.5
2	{A,B,C,D}	99.4	96.4	98.7
	{A,B,C,E}	99.8	98.5	91.1
	{A,C,D,E}	98.3	92.9	87.2
	{A,B,D,E}	98.3	97.2	85.4
2	{A,B,C}	99.8	94.9	90.1
	{D,E}	98.3	92.8	87.2
	{A,C,D}	98.3	92.9	87.8
	{B,E}	98.3	92.6	86.8
	{A,D,E}	97.9	92.8	86.8
	{B,C}	98.3	92.8	87.8
	{C,D,E}	99.1	97.2	85.4
	{A,B}			
	{A,B,E}			
	{C,D}			
	{A,C,E}			
	{B,D}			
	{A,B,D}			
	{C,sE}			
1	{A,B,C,D,E}	100	100	100

4. Conclusion: We have proposed a new approach for reducing the testing time and test cost for mixed signal digital circuits containing both analog and digital cores. The intermittent faults are eradicated .The proposed approach is based on the use of novel test wrapper for analog cores. We have developed a TAM optimisation and test scheduling approach that can handle analog and digital cores in a unified manner. In addition to reducing testing time, the proposed wrapper obviates the use need for expensive mixed signal testers.

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