# A high-frequency voltage-follower with global feedback

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*Abstract:* - A popular form for a voltage-follower (VF) with global feedback is a voltage operational amplifier (Op-Amp) with 100% negative feedback. Nevertheless, with currently available Op-Amps it is unable to meet high frequency specifications. This paper presents a high frequency voltage-follower based on an overall feedback technique. Despite the global feedback loop, the design presented small-signal bandwidth higher than 3GHz and gain flatness to within 0.1dB up to 170MHz. Due to this feedback loop, the circuits exhibits very high input and very low output impedance. In addition, the output voltage swing achieved is some ±3V, with an input offset current of around 130nA and an offset voltage in the range of 200uV. The proposed circuit is very stable, due to the stability technique used, maintaining low distortion. The total harmonic distortion (THD) of the circuit is better than -65dB and the intermodulation distortion (IMD) is some -70dB, for capacitive loads up to 10pF. The analysis of the novel circuit has been carried out for operating temperatures from -20$^{o}$C to +100$^{o}$C, using Analog Devices' extra fast complementary transistors. The power dissipation is some 52mW on a ±5V power supply, although it can be reduced to ±3.3V, without affecting significantly the performance, depending on the application.

*Key-Words:* - Voltage-follower, buffer, low distortion, high frequency, global feedback

## 1 Introduction

The overall system performance is very much dependent on the high frequency front-end component characteristics[1]. On the other hand, high frequency applications keep growing exponentially and more advanced circuit design methodologies are necessary to follow the market trends.

Typical applications such as TFT-LCD panels, video switches and instrumentation require VFs to provide a combination of isolation and bandwidth [2-3]. In addition, the VF is an important sub-circuit in several high frequency front-ends too, thus extra care should be taken on the design of such circuitry, to avoid limitations in the performance of the entire system. Using active loaded stages offers high voltage gain in feedback systems but at the expense of the significantly high dynamic output impedance. That causes low frequency poles in the system, especially when driving capacitive loads [4]. Using the VF either as an input or output stage provides isolation and current gain, producing a replica of the input signal, irrespectively of the operating conditions and the output load [5]. Ideally, a VF should present infinite input and zero output impedance, unity voltage gain and no distortion of the input signal. Practically, no such ideal unit exists but it is the object of design to approximate ideal performance as closely as possible.

The novel VF presented in this paper, although it has been designed and investigated for relatively large power supply voltages (±5V), can deliver very good THD and IMD performance for frequencies up to 1GHz. Besides, it exhibits very high input impedance, some 50KΩ at 250MHz and very low output impedance, less than 1Ω, at the above operating frequency, figures that can be further improved, at the expense of an increase in the power dissipation. The output voltage swing is some ±3V, mainly due to the increased number of base-emitter voltage drops of the biasing circuitry. This can be increased as well, by using alternative circuitry for

the current source and sink, depending on the applications. Apart from that, the offset voltage achieved is only 228uV at room temperature while the input offset current is some 130nA. The operation of the proposed design is specified from -20°C to +100°C and the power dissipation is some 52mW.

## 2 Circuit Description

The starting point of the proposed voltage-follower is shown in Fig.1. A single stage, long-tailed pair amplifier is followed by an emitter-follower which provides the required feedback [6-7]. Relevant voltages and currents are labeled for the DC analysis.

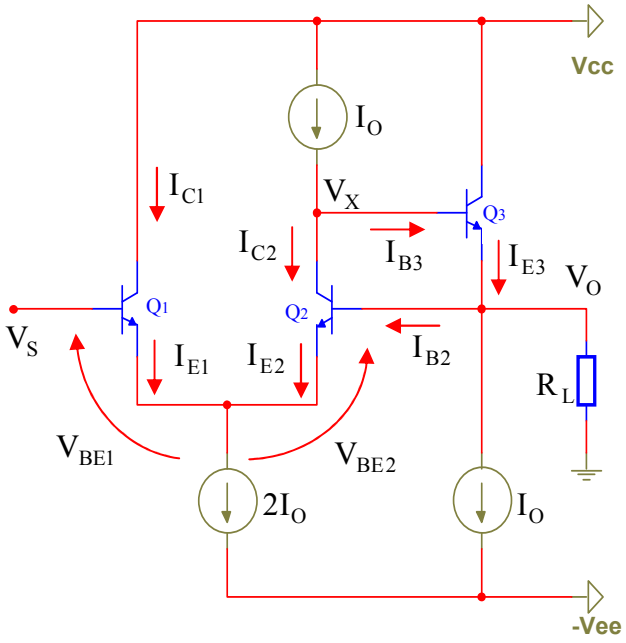


Fig.1 Core circuit of the proposed follower, labeled for a DC analysis

$I_{E2}$ can not exceed $2I_O$ because that would mean that Q1 is cut off. Hence, the current in the base of Q2 will be,

$$I_{B2} < \frac{2I_O}{(1+\beta)} \tag{1}$$

But,

$$I_{E3} = I_{B2} + I_O + \frac{V_O}{R_L} \tag{2}$$

Hence,

$$I_{B3} < \frac{2I_O}{(1+\beta)^2} + \frac{I_O}{(1+\beta)} + \frac{V_O}{(1+\beta)R_L} \approx \frac{I_O}{(1+\beta)} \tag{3}$$

Assuming that $V_O$ is very small and ignoring the first term in (3) compared with the second term,

$$I_{B3} \approx \frac{I_O}{(1+\beta)} \tag{4}$$

Consequently,

$$I_{C2} = I_O - \frac{I_O}{(1+\beta)} = \alpha I_O \tag{5}$$

and,

$$I_{E2} = \frac{1}{\alpha}(\alpha I_O) = I_O \tag{6}$$

Thus,

$$I_{E1} = I_O \quad \text{and} \quad I_{C1} = \alpha I_O$$

On the basis of the approximations made,

$$I_{C1} = I_{C2}$$

However,

$$V_{OS} = V_{BE1} - V_{BE2} = V_T \log_e \frac{I_{C1}}{I_{C2}} \tag{7}$$

Hence,

$$V_{OS} = 0$$

Fig.2 shows the equivalent impedance seen at the input of the circuit.

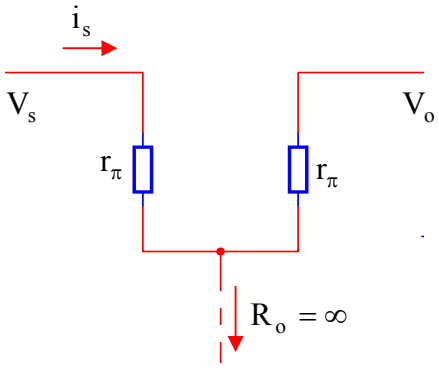


Fig.2 Input impedance of the long-tailed pair

By inspection,

$$i_s = \frac{V_s - V_o}{2r_\pi} = \frac{V_s\left(1 - \frac{V_o}{V_s}\right)}{2r_\pi} \tag{8}$$

Thus, the input impedance is,

$$Rin = \frac{V_s}{i_s} = \frac{V_s \cdot 2r_\pi}{V_s\left(1-\frac{V_o}{V_s}\right)} = \frac{2r_\pi}{\left(1-\frac{V_o}{V_s}\right)} = \frac{2r_\pi}{(1-G)} \quad (9)$$

For Op-Amp as a VF [8],

$$G = \frac{A}{(1+A)} \quad (10)$$

Thus,

$$(1-G) = \left[1-\frac{A}{(1+A)}\right] = \frac{1}{(1+A)} \quad (11)$$

Consequently, the input impedance is,

$$Rin = (1+A)\cdot 2r_\pi \approx A \cdot 2r_\pi \quad (12)$$

Fig.3 shows the equivalent output impedance, using the equivalent circuit of the output transistor Q3.

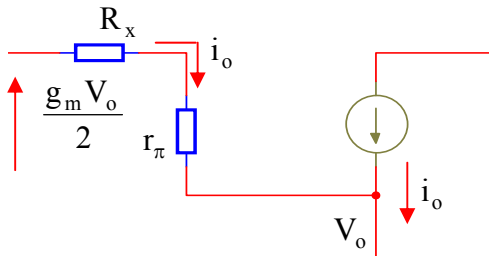


Fig.3 Equivalent circuit for the calculation of $Z_O$

If the output voltage decreases by $V_o$, then the voltage at the collector of Q2 increases by,

$$V_o \frac{g_m}{2} R_x \quad (13)$$

The base current of Q3 is,

$$i_b = \frac{\left(\frac{g_m}{2}R_x + 1\right)V_o}{(R_x + r_\pi)} \quad (14)$$

Thus,

$$i_o = \frac{(\beta_n + 1)\left(\frac{g_m}{2}R_x + 1\right)V_o}{(R_x + r_\pi)} \quad (15)$$

Hence, the output resistance is,

$$r_o = \frac{V_o}{i_o} = \frac{(R_x + r_\pi)}{(\beta_n+1)\left(\frac{g_m}{2}R_x + 1\right)} \approx \frac{\left[r_e + \frac{R_x}{(\beta_n+1)}\right]}{\left(\frac{g_m}{2}R_x + 1\right)} \quad 16)$$

$$r_o \approx \frac{\left[r_e + \frac{R_x}{(\beta_n+1)}\right]}{(A+1)} \quad (17)$$

The circuit of Fig.1 is not, as it stands, suitable for handling fast negative-going pulse edges, similarly to a simple emitter-follower. This limitation is overcome in the proposed circuit.

## 3 The proposed configuration

The complete circuit of the proposed design is shown in Fig.4. The biasing scheme for both source and sink is the "6-pack", used in several recent designs [9-11], and is presented in section 4. Comparing Fig.1 with Fig.4, Q6 and Q9 are added to provide suitable biasing for the complementary output stage. With $V_S = 0$ negative feedback ensures that $V_O \approx 0$, provided the transistors operate in the forward-active mode, with the DC current distribution shown. Now if $V_O = 0$, then the base of Q5 is $2V_{BE}$ above earth potential. The inclusion of the diode-strapped transistor Q3 and Q4 ensures that the collector voltage of Q2 is zero. Connecting the collector of Q1 to the output terminal makes the collector voltage of Q1 zero, too. Q7 and Q8 are connected in parallel so that their base-emitter voltage is the same as the other transistors and each has a collector current of 1mA. The connections, indicated, provide bootstrapping for the collector of both Q1 and Q2, with the intention of providing increased input impedance.

The proposed circuit was simulated with $V_S = 0$ to check the DC conditions. However the output revealed the presence of sustained sinusoidal oscillations occurring at a frequency of approximately 4.2GHz. Thus, the loop-gain magnitude and the loop-gain phase investigated. The result is shown in Fig.5. It is clear that $|L.G| = 2.77\text{dB}$ (i.e., $> 0\text{dB}$) when $\angle L.G = 0^o$, at $f = 4.46\text{GHz}$.

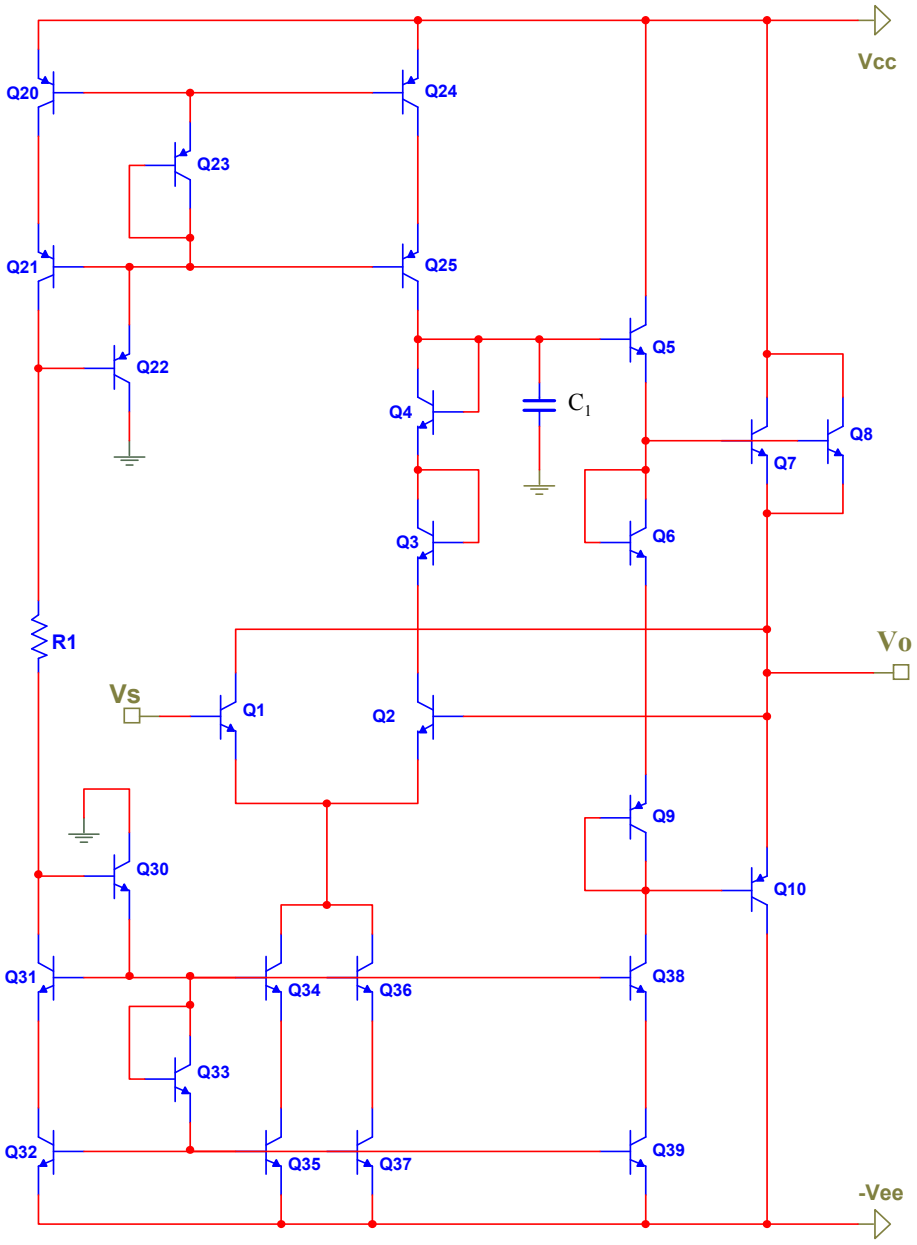


Fig.4 Full circuit of the proposed voltage-followe

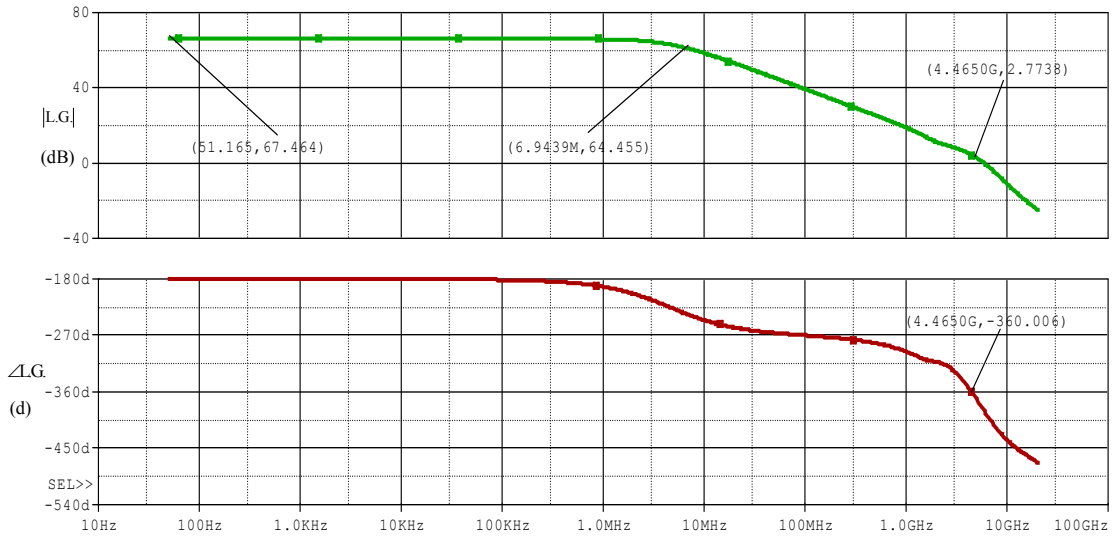


Fig.5 Loop-gain magnitude (top) and phase (bottom)

### 3.1 Investigation on stability

To achieve stability the 'dominant-pole' approach was adopted [12]. A small capacitor $C_1$ was connected to the collector of Q25 as shown in Fig.6 since this point has a comparatively high incremental resistance associated with it.

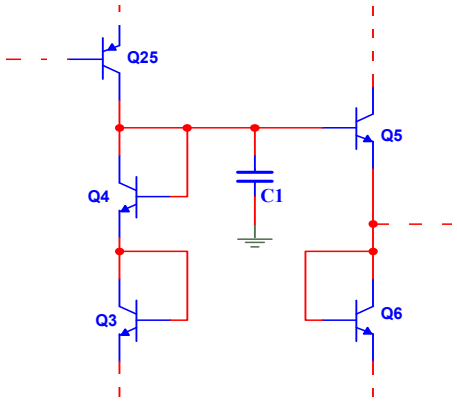


Fig.6 The 'dominant-pole' compensation technique

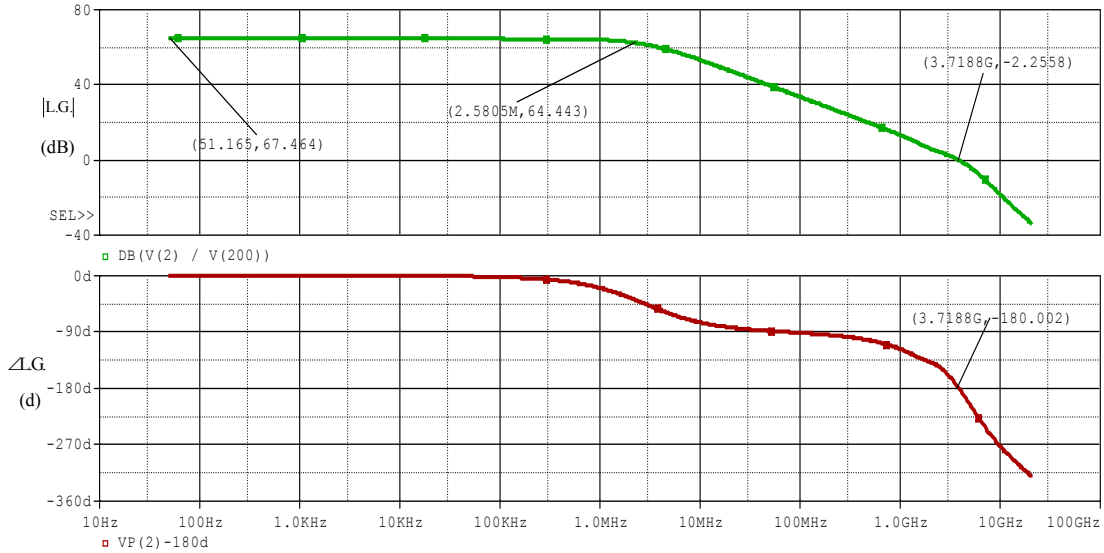


Fig.7 Loop-gain magnitude (top) and phase (bottom) after stabilization

$C_1$ has the effect of reducing the bandwidth with the result that $|\text{L.G}| < 0\text{dB}$ when $\angle\text{L.G} = 0^o$. Trial and error revealed that $C_1 = 0.2\text{pF}$ was just enough to achieve this but, in order to produce a gain and phase margin that would not only take account of circuit tolerances but also to provide acceptable peaking in the frequency response of the closed-loop gain, a value of 0.35pF was decided on. This provides a gain margin of 2.26dB, as shown in Fig.7.

A higher gain margin could be achieved with a larger value of $C_1$ but that would be at the expense of closed-loop bandwidth and chip area.

### 3.2 DC conditions of the proposed design

The simulated transfer characteristic of the new circuit, shown in Fig.8, has good linearity and unity slope, a consequence of the overall feedback [13]. The enlarged plot of Fig.8 in the vicinity of the origin, shown in Fig.9, confirms the existence of a very small offset voltage, for reasons described in the initial schematic.

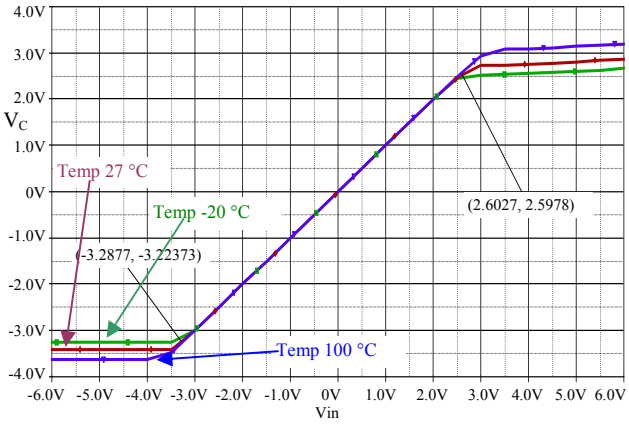


Fig.8 Simulated transfer characteristic of the VF

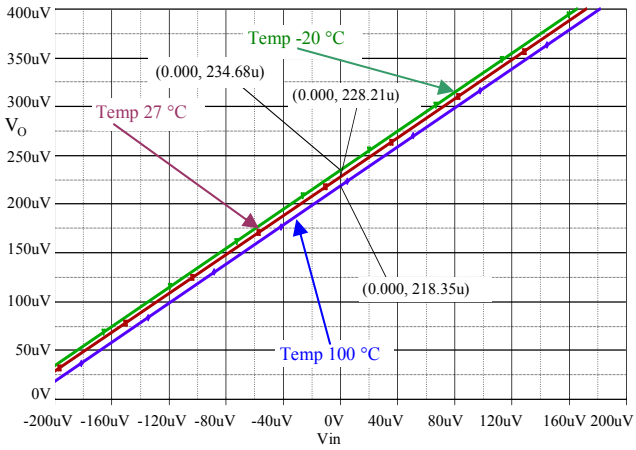


Fig.9 Expanded view of the transfer characteristic in the vicinity of the origin

Fig.8 shows a linear range extending from -3V to +2.7V. Theoretically, the linear input range is

$$(V_{CC} - 4V_{BE}) > V_S > -(V_{EE} - 3V_{BE}) \qquad (18)$$

This confirms the simulated figures if we substitute $V_{CC} = V_{EE} = 5V$ and $V_{BE} = 0.75V$. The slope of the characteristics in this region is indicative of the high incremental input resistance. The slope variation with temperature is due to the temperature dependence of $\beta_n, \beta_p$.

The quiescent power dissipation of the circuit is

$$P_Q = (V_{CC} + V_{EE}) \cdot I_Q \cdot n \qquad (19)$$

Substituting for $V_{CC} = V_{EE} = 5V$, $I_Q = 1mA$ and $n = 5$, at 27°C

$$P_Q = 50mW$$

The quiescent power dissipation produced from the simulation of the circuit was 51.6mW at room temperature, in good agreement with the theory.

### 3.4 Small-signal voltage-gain

Fig.10 shows the frequency response of the proposed circuit. Compared to conventional followers it presents considerably reduced peaking, due to the feedback loop and the stability that the negative feedback offers.

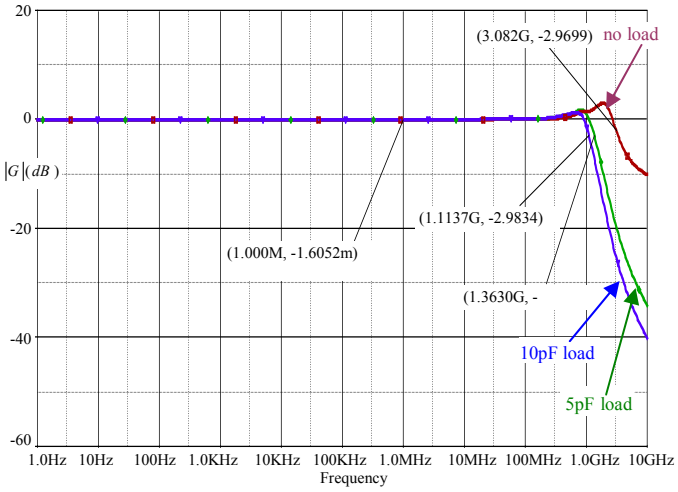


Fig.10 Frequency response for the small-signal gain $|G|$ of the proposed circuit with different loads

### 3.5 Incremental input impedance

The incremental input impedance as a function of frequency is shown in Fig.11. Spot values are shown in Table 1. The high input impedance results from the bootstrapping of the collector of $Q_1$.

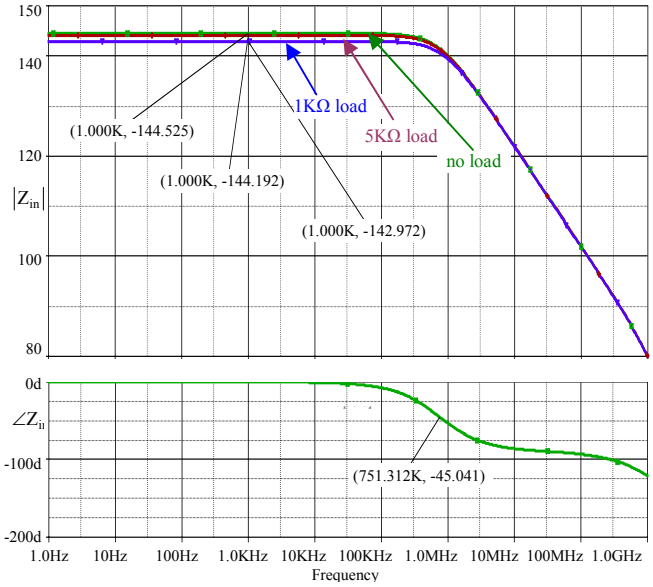


Fig.11 Bode plots for $|Z_{in}|$ for several loads and input phase

| Conditions | $\|Z_{in}\|$ (Ω) | | | | | |
|---|---|---|---|---|---|---|
| Operating temp. (°C) | -20 | 27 | 100 | -20 | 27 | 100 |
| Freq. 312.5KHz | 10.2M | 15.5M | 25.9M | 9.8M | 15.1M | 25.3M |
| Freq. 31.25MHz | 309K | 401K | 552K | 307K | 398K | 549K |
| Freq. 250MHz | 38.6K | 49.3K | 66.5K | 38.4K | 49.2K | 66.4K |
| Output load | $R_L = \infty$ | | | $R_L = 5K\Omega$ | | |

Table 1 $|Z_{in}|$ of the VF with $R_L = \infty$ and $R_L = 5K\Omega$, as a function of f and T

### 3.6 Incremental output impedance

The approach presented here, to calculate the incremental output impedance of the circuit, is based on a general property of linear voltage amplifier circuits. If the output is incrementally short-circuited, $V_O = 0$ and $i_O = i_{SC}$.

Hence

$$GV_S = i_{SC} r_O \tag{20}$$

By inspection in Fig.4, looking into the base of Q5, the incremental resistance is

$$R_{B5} = r_{X5} + r_{\pi 5} + \left[ (\beta_5 + 1) \left[ \left( \frac{r_{X7} + r_{\pi 7}}{2} \right) // r_{O5} \right] \right] \tag{21}$$

where $r_X$, with appropriate second subscript, represents the transistor base bulk resistance.

Straightforward calculations according to the operating conditions, gives

$$r_O = \frac{V_S}{i_{SC}} = \frac{V_S}{i_{B5}(\beta_5 + 1)(\beta_7 + 1)} \approx 31.3 m\Omega \tag{22}$$

Fig.12 shows $|Z_o|$ and $\angle Z_o$ as a function of frequency for three different operating temperatures. Spot values for $|Z_o|$ as a function of f and T are shown in Table 2. Some difference between theoretical and simulated values has been observed which is accounted for the extra components of $i_{SC}$ that have been ignored. These are the current flowing to the collector of Q1 and the current reaching the output via the base of Q1 and Q2. In connection with the emitter-follower outputs, $Z_o$ is inductive at high frequencies.

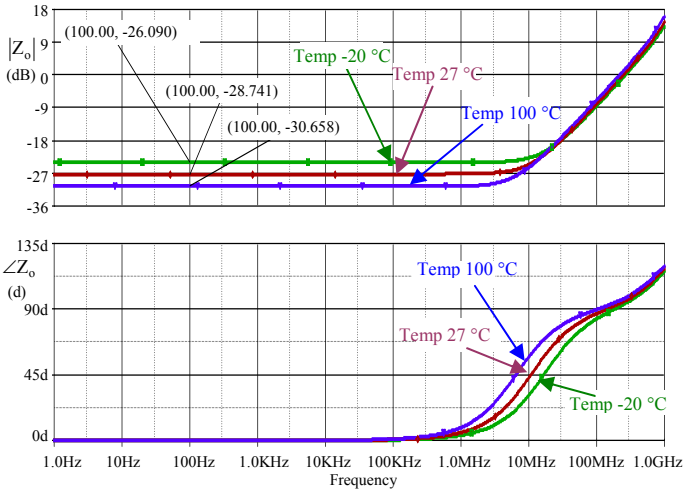


Fig.12 Magnitude (upper curve) phase (lower curve) for $Z_o$

| Conditions | $\|Z_o\|$ (Ω) | | |
|---|---|---|---|
| Operating temp. (°C) | -20 | 27 | 100 |
| Freq. 312.5KHz | 49m | 36m | 29m |
| Freq. 31.25MHz | 130m | 131m | 133m |
| Freq. 250MHz | 923m | 990m | 1130m |

Table 2 $|Z_o|$ of the circuit as a function of f and T

### 3.7 Total harmonic and intermodulation distortion

Tables 3 and 4 show, respectively, THD under specified conditions at 31.25MHz and 250MHz. The performance of the circuit at higher frequencies deteriorates mainly due to the compensation capacitor and the collector current of the output transistor. Table 5 shows the IMD performance results for the proposed circuit, as a function of operating frequency and temperature.

| Conditions | THD ( dB ) | | |
|---|---|---|---|
| Operating temp. (°C) | -20 ° | 27 | 100 |
| $Z_L = 5K\Omega$ | -74.5 | -72.4 | -70.8 |
| $Z_L = 5K\Omega$ // $5pF$ | 60.9 | -60.7 | -59.2 |

Table 3 THD of the new circuit at 31.25MHz

| Conditions | THD ( dB ) | | |
|---|---|---|---|
| Operating temp. (°C) | -20 ° | 27 | 100 |
| $Z_L = 5K\Omega$ | -53.5 | -54.2 | -54.7 |
| $Z_L = 5K\Omega$ // $5pF$ | -49.8 | -52.4 | -51.1 |

Table 4 THD of the new circuit at 250MHz

| Conditions | IMD ( dB ) | | |
|---|---|---|---|
| Operating temp. (°C) | -20 ° | 27 | 100 |
| Freq. 31.25MHz | -87.1 | -87.5 | -88.9 |
| Freq. 250MHz | -57.7 | -58.3 | -61.2 |

Table 5 IMD of the new circuit as a function of f and T

### 3.8 Pulse response

An approximate analysis of the transient response of the voltage follower has been carried out using the charge-control approach pioneered by Beaufoy and Sparkes [14]. According to that the Slew Rate, which determines the maximum sinusoidal output voltage at a given frequency, is limited by the product $C_k r_x$ or the ratio $I_o / C_L$, where

$$\left[ c_\mu + \left( \frac{C_L}{\beta_o} \right) \right] = C_k , \qquad (23)$$

$r_x$ is the extrinsic base resistance and

$c_\mu$ is the collector-base capacitance

whichever give the greater value for rise and fall times for $u_o$.

To proceed further it is necessary to decide on the nature of input signal, $u_b$. In case it has the form of a truncated ramp voltage, as shown in Fig.13, the component parts of the leading edge will the similar to that shown in Fig.14.

Accurate prediction of rise and fall times and current maximum amplitudes is not simple. In practice, it is necessary to ensure from the simulation plots that the transistor does not exceed its $i_{C(max)}$ and $P_{C(max)}$ in the event of small values of $t_r, t_f$ and large values of $C_L$.

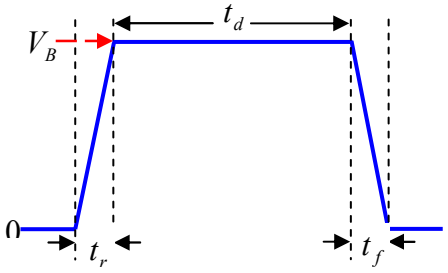


Fig.13 Assumed input voltage signal

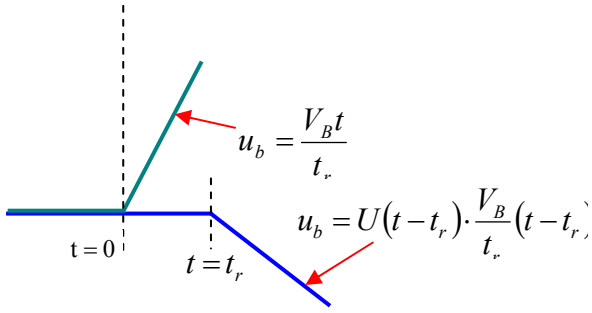


Fig.14 Components of the leading edge

Fig.15 shows the waveforms when a positive going input pulse of amplitude 1V and rise and fall times of 1nS is applied.

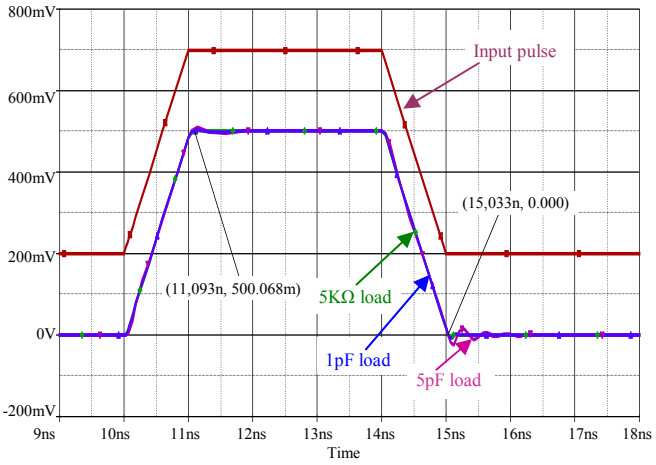


Fig.15 Pulse response for an input signal with 1nS rise and fall times

## 4 The current biasing scheme

The precise multiple-output current-mirror, also called '6-pack', is a current-mirror that combines high output resistance and excellent current transfer ratio, as well as expandability. The '6-pack' schematic, including the DC currents used for the analysis of the circuit, is shown in Fig.16.

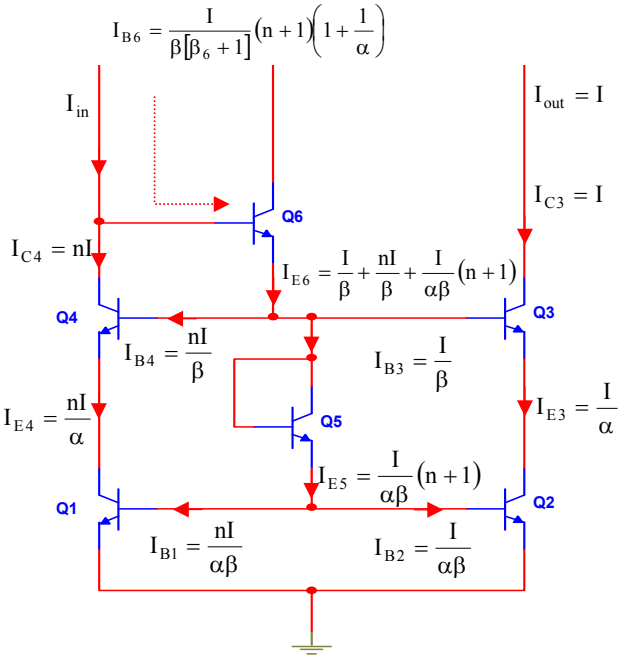


Fig.16 The '6-pack' precise current mirror

It has been shown [15] that the current transfer ratio of this mirror is,

$$\lambda = \frac{I_{out}}{I_{in}} \approx \frac{1}{n}\left[1 - \frac{\left(2+\frac{2}{n}\right)}{\beta\beta_6}\right] \approx 1 - \frac{4}{\beta^2} \pm \frac{V_{OS}}{V_T} \qquad (24)$$

where $\beta_6$ is the common-emitter current gain of Q6, which is different from the other transistors because it operates at lower $I_C$.

An advantage of the '6-pack' mirror over conventional designs is its expandability. Thus, the outputs of the circuit can be increased by adding two transistors in parallel with transistors Q2 and Q3. In this case, the current transfer ratio of the mirror will be,

$$\lambda = \frac{I_{out}}{I_{in}} \approx 1 - \frac{6}{\beta^2} \pm \frac{V_{OS}}{V_T} \qquad (25)$$

Due to the fact that the emitter of transistor Q6 is connected to a low impedance point, the output resistance is close to that of the common-base stage. Using an infinite impedance current source as the input to the mirror, the output resistance, $R_O$, is approximated by,

$$R_O \approx \beta r_o \qquad (26)$$

If the finite output resistance of the current source is taken into account, the output resistance will be,

$$R_O = r_o\left[1 + \beta\left(1 - \frac{1}{\alpha\beta_6\gamma}\right)\right] \qquad (27)$$

where $\gamma$ is the ratio between the output resistance of the current source and the resistance seen looking into the base of transistor Q6. The term $\frac{1}{\alpha\beta_6\gamma}$ cannot always be neglected.

The output impedance of the '6-pack' is shown in Fig.17, for two operating currents. Table 6 presents a comparison among several well-established current mirrors for operating current $I_C = 1mA$, and justifies the reason why the '6-pack' scheme has been chosen.

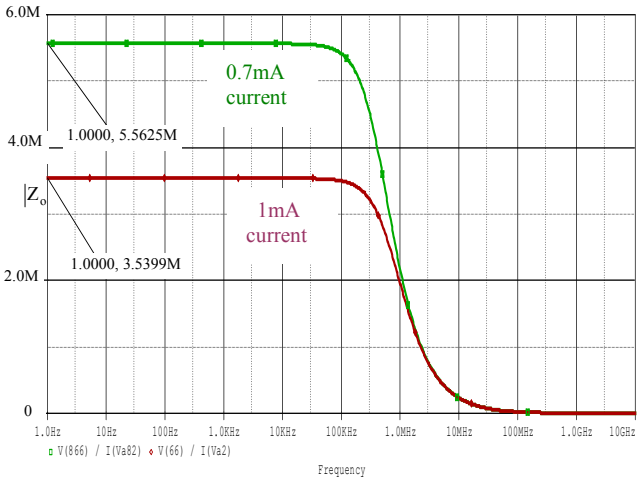


Fig.17 Output impedance of the '6-pack' for $I_C = 0.7mA$ and $I_C = 1mA$

| Configuration | Output current over Input current ratio, λ, for 1mA current | Output Impedance with 1mA current (Ω) |
|---|---|---|
| Simple C.M | 1.02 | 85.9K |
| Buffered C.M | 1.039 | 83.77K |
| Cascoded C.M | 0.929 | 2.073M |
| Buffered C.M with cascoded output | 0.992 | 3.442M |
| Wilson C.M | 0.991 | 1.835M |
| Modified Wilson C.M | 1.001 | 1.804M |
| '6pack' | 0.999 | 3.539M |

Table 6 A comparison of several current-mirrors

# 5 Conclusion

A voltage-follower for high frequency applications has been presented. The circuit has been simulated using Analog Devices' extra fast complementary transistors, with 1mA operating current. The new voltage-follower is using overall feedback in addition to local feedback which is lay to a number of improvements in the VF performance, notably with respect to input and output impedance, offset voltage and pulse response. In addition it combines good distortion levels with wide linear operating range. The price to be paid for this is a relatively restricted operating bandwidth due to the added capacitor which ensures Nyquist stability.

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