Current-Mode Filters Advanced Synthesis Methods, Based on Intermediate Transfer Function Algorithm

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Abstract: - In this paper are presented two current mode techniques for low-voltage, continuous-time, analogue filter implementation. The first presented technique is adequate for very low power application and is based on a translinear approach. The second presented technique is adequate for high frequency application. In the paper, firstly, the state-space description and the used synthesis techniques of current-mode filters are presented. Then the two different current-mode integrators are presented and analyzed. Finally, as a test vehicle for the proposed techniques, two low voltage, third order, continuous-time filters, for low power applications structure implementation are described and analyzed.

Key-Words: - Analogue signal processing circuits, CMOS analogue filters, low power and voltage circuits.

1 Introduction

The existing CMOS technologies provide ample opportunities to integrate entire system on a single chip. To date, the ability to integrate large digital systems has far out weighted the ability to integrate the analogue systems. The greatest impediment to analogue CMOS VLSI design has been the difficulty to get consistent circuit performance over the broad range of requirements for signal gain, frequency and/or phase response, delay, power consumption and signal integrity. In the same time the analogue design in mixed signal environments becomes more difficult and challenging as the IC's power supply voltage scales down, to the values slightly higher than the MOS threshold voltage.

The analogue signal processing at low values of supply voltages can best be performed in the current-operation domain, because the very low voltage swings are avoided. In translinear circuits the MOS transistors usually operate in weak inversion (or sub-threshold) region, [1], where the current-voltage characteristic is exponential. So these circuits can be used in very low power application. The main problems associated to the sub-threshold region operation are the relatively low speed capability and inferior matching. But these problems are relatively solved in sub-micron technology. Yet, significantly better performances in frequency response are obtained when the MOS transistors operate in strong inversion.

Therefore we conceived two integrator cells. In the first one the MOS transistors operate in weak inversion and in the other MOS transistors operate in strong inversion. Also we developed synthesis techniques, based on intermediate transfer functions method, for both integrator cells.

This paper first presents the synthesis techniques for continuous time current-mode filters operating at low supply voltage. Then the used current-mode integrators are presented and analyzed. The basic current-mode integrators are based:

- the first, on the translinear technique and
- the second, on an adapted form of pseudodifferential transconductor presented in [2], but ours have a folded cascod structure and presents good performances for the low-cost standard CMOS technology.

Finally the structure of a two different third order low-pass current-mode filters in 1μm CMOS technology are presented. In this technology the SPICE simulations show:

- For the first filter a 1 kHz cut-off frequency, a dynamic range greater than 45dB for 1V supply voltage and power consumption smaller than 0,5 mW.

- For the second filter an 11 MHz cut-off frequency, low distortions (about 1%), a dynamic range greater than 50 dB for a 3 V supply voltage. In these conditions the power consumption of the filter is 5 mW. The minimum operation voltage for our structure is about 1,4V.

By using the intermediate transfer function synthesis method we obtained optimized structures with low noise and maximized output signal levels for all integrators and, in consequence, with a very good dynamic range. Much higher performances could be achieved, using this synthesis technique, with a more advanced technology.

Generally, in literature low-power continuous-time filter are realized either using current-mode technique [2], [3], [4] either using Gm-C technique [5], [6], [7], [8], [9]. The current-mode technique leads to more simple structure and with a better dynamic range at the same supply voltage. Spectacular results are obtained in advanced sub-micron technology even with Gm-C cells like in [10].

2 The Synthesis Methods of Current-Mode Filters

This section presents the modality in which intermediate transfer function synthesis method [11] can be used in current-mode domain filters. The method was developed for *AO-RC* filter; basically a given *n*-th order transfer function is realized using *n* resistively interconnected integrators. The design process consists in two steps: firstly a set of intermediate transfer functions (IFs) is selected and then the set is used in synthesis of circuit that implements the given transfer function. The major advantage of this method is that the filter's performance evaluation and optimization can be performed at the abstract level of transfer function generation and not at the circuit topology level.

The state-variable formulation of the *AO-RC* is

$$\begin{aligned} \mathrm{s}\cdot\mathbf{x}(\mathrm{s}) &= \mathbf{A}\cdot\mathbf{x}(\mathrm{s}) + \mathbf{b}\cdot\mathbf{u}(\mathrm{s}) + \varepsilon(\mathrm{s}) \\ \mathbf{y}(\mathrm{s}) &= \mathbf{c}^{\mathrm{T}}\cdot\mathbf{x}(\mathrm{s}) + \mathrm{d}\cdot\mathbf{u}(\mathrm{s}) \end{aligned} \tag{1}$$

where the vector $\mathbf{x}(\mathrm{s})$ represents the circuit state (integrators outputs), matrix $\mathbf{A}$ describes the interconnections between the n integrators, vector $\mathbf{b}$ contains the coefficients that multiply the input signal $\mathbf{u}(\mathrm{s})$ in order to be applied to the integrators inputs, vector $\mathbf{c}$ contains the coefficients required to form the output, scalar d is the coefficient of the feedthrough component from input to output, and $\varepsilon(\mathrm{s})$ is the vector containing the noise component at the integrator inputs.

The dual sets of IFs, $\{f_i(\mathrm{s})\}$ and $\{g_i(\mathrm{s})\}$ are given by:

$$\begin{aligned} f_i(\mathrm{s}) &\overset{\Delta}{=} \frac{x_i(\mathrm{s})}{u(\mathrm{s})};\ \ \mathbf{f}(\mathrm{s}) = (\mathrm{s}\cdot\mathbf{I}-\mathbf{A})^{-1}\cdot\mathbf{b} \\ g_i(\mathrm{s}) &\overset{\Delta}{=} \frac{y(\mathrm{s})}{\varepsilon_i(\mathrm{s})};\ \ \mathbf{g}^{\mathrm{T}}(\mathrm{s}) = \mathbf{c}^{\mathrm{T}}(\mathrm{s}\cdot\mathbf{I}-\mathbf{A})^{-1} \end{aligned} \tag{2}$$

The set $\{f_i(\mathrm{s})\}$ contains the transfer functions from the filter input to the integrator outputs, and the set, $\{g_i(\mathrm{s})\}$, can be physically interpreted as the integrators noise gains.

Given a transfer function $t(\mathrm{s})$, IF synthesis is based on choosing a set of linearly independent functions, $\{f_i(\mathrm{s})\}$, having identical denominator polynomials, $e(\mathrm{s})$, and arbitrary numerator polynomials of degree less than n. From this set the $\{\mathbf{A}, \mathbf{b}, \mathbf{c}, \mathrm{d}\}$ parameters can be obtained using the following relation:

$$\begin{aligned} &\mathbf{A} = \mathbf{F}\cdot\mathbf{E}\cdot\mathbf{F}^{-1},\ \mathbf{b} = \mathbf{F}\cdot\mathbf{1},\ \mathbf{c}^{\mathrm{T}} = \mathbf{t}^{\mathrm{T}}\cdot\mathbf{F}^{-1}, \\ &d = t_{n+1}, t(\mathrm{s}) = \mathbf{t}^{\mathrm{T}}\cdot v(\mathrm{s}) + t_{n+1}, \\ &\mathbf{f}(\mathrm{s}) = \mathbf{F}\cdot v(\mathrm{s}),\ \ \mathbf{g}(\mathrm{s}) = \mathbf{G}\cdot v(\mathrm{s}), \\ &v_i(\mathrm{s}) = 1/(\mathrm{s}-e_i),\ i=\overline{1,n}, \\ &\mathbf{G}^{\mathrm{T}} = \mathbf{H}\cdot\mathbf{F}^{-1} \end{aligned} \tag{3}$$

where $\mathbf{t}$ is a vector containing the $t(\mathrm{s})$ n residues at the poles, t_{n+1} – the residue at s=∞, $\mathbf{F}$ – a matrix containing the residues of the f functions evaluated at the poles, $\mathbf{G}$ – a matrix of the residues of the g functions, e_i – the $e(\mathrm{s})$ roots, $\mathbf{E}$ – the diagonal matrix having the natural modes e_i as its elements, $\mathbf{H}$ – a diagonal matrix formed from the residues of $t(\mathrm{s})$, and $\mathbf{1} = (1, 1, \ldots 1)^{\mathrm{T}}$.

The sensitivities of filter directly depend of IFs set:

$$\begin{aligned} &S_{A_{ij}}^{t(\mathrm{s})} = g_i(\mathrm{s})\cdot f_i(\mathrm{s})\cdot A_{ij}/t(\mathrm{s}), \\ &S_{b_i}^{t(\mathrm{s})} = g_i(\mathrm{s})\cdot b_i/t(\mathrm{s}),\ S_{c_i}^{t(\mathrm{s})} = f_i(\mathrm{s})\cdot c_i/t(\mathrm{s}) \\ &S_d^{t(\mathrm{s})} = d/t(\mathrm{s}),\ S_{\gamma_i(\mathrm{s})}^{t(\mathrm{s})} = f_i(\mathrm{s})\cdot g_i(\mathrm{s})\cdot \mathrm{s}/t(\mathrm{s}), \\ &S_{\mu_i(\mathrm{s})}^{t(\mathrm{s})} = S_{\gamma_i(\mathrm{s})}^{t(\mathrm{s})}\cdot S_{\mu_i(\mathrm{s})}^{\gamma_i(\mathrm{s})} \end{aligned} \tag{4}$$

In the above equations γ_i is the integrator gain and $\mu_i(\mathrm{s})$ is the operational amplifier gain.

Noise signals injected at integrator inputs can be modelled by $\varepsilon(\mathrm{s})$. Assuming white input noise, with spectral density N_i^2, the output noise power spectrum is given by

$$P_{n0}(\omega) = N_i^2\cdot\sum_i\left|g_i(\mathrm{j}\omega)\right|^2 \tag{5}$$

with a rms level of

$$\left\|P_{n0}(\omega)\right\| = N_i^2 \sqrt{\sum_i \left\|g_i(\mathrm{j}\omega)\right\|_2^2} \tag{6}$$

where

$$\left\| g_i(\mathrm{j}\omega) \right\|_2^2 = \sqrt{\int_{-\infty}^{\infty} \left| g_i(\mathrm{j}\omega) \right|^2 \mathrm{d}\omega} \tag{7}$$

This description can be adapted to the current-mode filter. The current through the *k*-th capacitor of the current-mode filter is

$$\begin{aligned} C_k \dot{v}_{Ck} &= i_{Ck1} + i_{Ck2} + ... + i_{Ckn} + i_{Cbk} = \\ &= a_{k1}^* \cdot i_1 + a_{k2}^* \cdot i_2 + ... + a_{kn}^* \cdot i_n + b_k^* \cdot i_{in} + \varepsilon_k^* \end{aligned} \tag{8}$$

where i_{Ckj}, $k, j=1\div n$, is the *k*-th capacitor current component dependent on output current i_j, $j=1\div n$, i_j is the *j*-th current-mode integrator output current, i_{in} is the filter input current, a_{kj}^*, $k, j=1\div n$ and b_k^*, $k=1\div n$, coefficients describes the capacitor current components dependence on the output currents of the current-mode integrators, respectively, on the filter input current, and $\varepsilon_k^* = \sum_j \varepsilon_{kj}^*$ is the total noise current through capacitor.

Using convenient circuit technique to implement an appropriate dependence, required by the type of implementation, between capacitor voltage, v_{Ck}, and output current of current-mode integrator, i_k, one can obtain a state-variable description of the current-mode filter.

(1) For the translinear technique the dependence between the two signals must be logarithmic

$$v_{Ck} = V_x \ln\left(i_k / I_y\right) \tag{9}$$

where V_x and I_y are scale factors.

The capacitor voltage derivative, $\dot{v}_{Ck}$, becomes:

$$\dot{v}_{Ck} = \frac{V_x}{i_k} \frac{\mathrm{d}i_k}{\mathrm{d}t}. \tag{10}$$

Using the translinear loops one get for each component of the capacitor current

$$i_{Ckj}\, i_k = \overline{a}_{kj}^*\, i_j, \quad i_{Cbk}\, i_k = \overline{b}_k^*\, i_{in} \tag{11}$$

and equation (8) becomes

$$\mathrm{d}i_k / \mathrm{d}t = a_{k1} i_1 + a_{k2} i_2 + ... + a_{kn} v_n + b_k i_{in} + \varepsilon_k \tag{12}$$

where

$$a_{kn} = a_{kn}^* / (C_k V_x),\ b_k = b_k^* / (C_k V_x),\ \varepsilon_k = \varepsilon_k^* / (C_k V_x) \tag{13}$$

The circuit resulted by the interconnection of *n* current mode integrators with translinear loops can be described by the same state-variable formulation (1):

$$\begin{aligned} \mathrm{s} \cdot \mathbf{x}(\mathrm{s}) &= \mathbf{A} \cdot \mathbf{x}(\mathrm{s}) + \mathbf{b} \cdot i_{in}(\mathrm{s}) + \boldsymbol{\varepsilon}(\mathrm{s}) \\ i_{out}(\mathrm{s}) &= \mathbf{c}^{\mathrm{T}} \cdot \mathbf{x}(\mathrm{s}) + d \cdot i_{in}(\mathrm{s}) \end{aligned} \tag{14}$$

where the states x_k are represented by the integrators output current, matrix element A_{kj} is implemented by a translinear loop with input current x_k and output the component i_{Ckj} of the current through *k*-th, the vector element b_k is implemented by a translinear loop from the input i_{in} to state *k*, c_k is the multiplication coefficient of the state *k* required to form the output current of the filter i_{out}, d is the multiplication coefficient of the input current i_{in} and $\boldsymbol{\varepsilon}(s)$ can model the current noise at the input of the *k*-th current integrator.

(2) For the filter with integrators where the MOS transistors operate in strong inversion the dependence between capacitor voltage, v_{Ck}, and output current of current-mode integrator, i_k, must be linear

$$v_{Ck} = i_k / G_k \tag{15}$$

where G_k is a transconductance scale factor.

The capacitor voltage derivative, $\dot{v}_{Ck}$, becomes:

$$\dot{v}_{Ck} = \dot{i}_k / G_k \tag{16}$$

and equation (8) becomes

$$\dot{i}_k = a_{k1} \cdot i_1 + a_{k2} \cdot i_2 + ... + a_{kn} \cdot i_n + b_k \cdot i_{in} + \varepsilon_k \tag{157}$$

where

$$a_{kn} = a_{kn}^* \cdot G_k / C_k,\ b_k = b_k^* \cdot G_k / C_k,\ \varepsilon_k = \varepsilon_k^* \cdot G_k / C_k \tag{168}$$

The circuit resulted by interconnecting *n* current mode integrators can be described again by the same state-variable formulation (1):

$$\begin{aligned} \mathrm{s} \cdot \mathbf{x}(\mathrm{s}) &= \mathbf{A} \cdot \mathbf{x}(\mathrm{s}) + \mathbf{b} \cdot i_{in}(\mathrm{s}) + \boldsymbol{\varepsilon}(\mathrm{s}) \\ i_{out}(\mathrm{s}) &= \mathbf{c}^{\mathrm{T}} \cdot \mathbf{x}(\mathrm{s}) + d \cdot i_{in}(\mathrm{s}) \end{aligned} \tag{179}$$

where the states x_k are represented by the integrators output current, matrix element A_{kj} is implemented by a current-mode amplifier that has at the input the current x_i and at the output the component i_{Ckj} of the current through *k*-th capacitor, the vector element b_k is implemented by a current amplifier from the input i_{in} to the *k* integrator input, c_k is the multiplication coefficient of state *k* required to form the output current of the filter i_{out}, d is the multiplication coefficient of the input current i_{in} and $\boldsymbol{\varepsilon}(s)$ can model the current noise at the input of the *k*-th current integrator.

So the meaning of $\{f_k(\mathrm{s})\}$ IF's set is the same as in the *OA-RC* filter synthesis (the state *k* and the input signal ratio) and the physical meaning of $\{g_k(\mathrm{s})\}$ IF's set is the noise gain to the input of integrator *k* at output of filter. We can conclude that all the results obtained in the *OA-RC* filter synthesis can be applied to the current-mode filter synthesis.

3 The Basic Translinear Current-Mode Integrator

This section first presents a brief review of the MOS transistor I-V characteristics, focused on weak inversion operation, and then the translinear current-mode integrator cell.

It is well known the general expression of drain current of MOS transistor [1]:

$$I_D = I_S \cdot \exp\left(\frac{V_P}{V_T}\right) \cdot \left[\exp\left(-\frac{V_S}{V_T}\right) - \exp\left(-\frac{V_D}{V_T}\right)\right] \quad (20)$$

or in terms of V_{GS} and V_{GD} as follows

$$I_D = I_S \cdot \exp\frac{V_P - V_G}{V_T} \cdot \left(\exp\frac{V_{GS}}{V_T} - \exp\frac{V_{GD}}{V_T}\right), \quad (21)$$

where I_S is the specific current (limit of weak inversion).

The specific current is proportional to W/L, one can write

$$I_S \cdot \exp[(V_P - V_G)/V_T] = (W/L) \cdot I_\Diamond(V_G), \quad (22)$$

with $I_\Diamond(V_G)$ the zero-bias ($V_{GS} = 0$) current for a square transistor, which represents the body effect. So, the forward and reverse currents become:

$$\begin{aligned} I_F &= (W/L) \cdot I_\Diamond(V_G) \cdot \exp(V_{GS}/V_T) \\ I_R &= (W/L) \cdot I_\Diamond(V_G) \cdot \exp(V_{GD}/V_T) \end{aligned} \quad (23)$$

If $I_R << I_F$, then the MOS transistor is saturated, otherwise the MOS transistor is non-saturated.

In figure 1.a are shown the two operation regions for weak inversion, which are defined by the ratios I_D/I_F and V_{DS}/V_T [12].

Therefore, each of the drain current components (expressed by (23)) of a non-saturated transistor may be related to an equivalent saturated transistor with gate-source voltage V_{GS} and V_{GD} respectively and the non-saturated transistor may be decomposed into two identical saturated transistors anti-parallely connected [13]. This is symbolically shown in figure 1.b. The transistor that corresponds to reverse current component is shown in dashed line, and represents the effect of the non-saturated operation of the real transistor.

The basic current-mode integrator schematic, with its translinear loop for a i_{Cij}, is presented in Fig. a. and its symbolic representation in Fig. .b. The minimum supply voltage required for this circuit is given by the MOS transistor threshold voltage plus the drain-source saturation voltage. Due to this low voltage value the transistors M_4, M_{13}, M_2 and M_6 are non-saturated. Therefore, using the decomposition technique described above (see Fig. .b.), the fictitious transistors M_{2*}, M_{4*}, M_{6*} and M_{13*} (dashed line in Fig. .b) were added in order to account the non-saturated operation of these transistors.

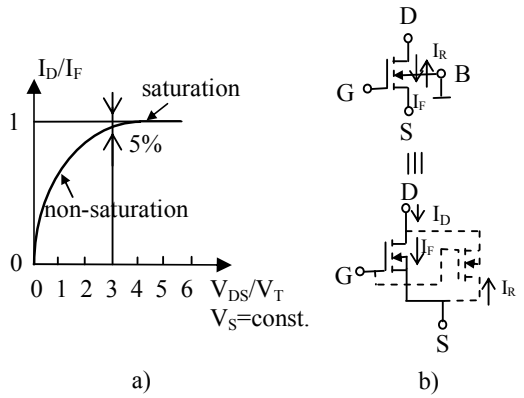


Figure 1: a) The operation regions in weak inversion of the MOS transistor; b) Non-saturated MOS

This way all transistors can now be regarded as saturated, $I_R << I_F$, and to a good approximation

$$I_{Di} = I_{Fi} = (W_i/L_i) \cdot I_\Diamond(V_{Gi}) \cdot e^{V_{GSi}/V_T} \quad i = \overline{1,10} \quad (24)$$

The integrator has four local loops: (1) M_1, M_5, M_{4*}, M_3, (2) M_1, M_5, M_{6*}, M_7; (3) M_1, M_{2*}, M_8, M_7, (4) M_{14}, M_{13*}, M_{16}, M_{15}, and a general translinear loop (5) M_1, M_5, M_{10}, M_9, M_7, M_8.

Applying the Kirchhoff law to these translinear loops, using equations (24) and assuming the equal-sized transistors, the translinear loops equations become:

$$(1)\begin{cases} V_T \ln[I_{D1}/I_\Diamond(V_{G1})] - V_T \ln[I_{D5}/I_\Diamond(V_{G5})] = \\ V_T \ln[I_{D3}/I_\Diamond(V_{G3})] - V_T \ln[I_{D4*}/I_\Diamond(V_{G4})] \end{cases} \quad (25)$$

$$(2)\begin{cases} V_T \ln[I_{D1}/I_\Diamond(V_{G1})] - V_T \ln[I_{D5}/I_\Diamond(V_{G5})] = \\ V_T \ln[I_{D7}/I_\Diamond(V_{G7})] - V_T \ln[I_{D6*}/I_\Diamond(V_{G6})] \end{cases} \quad (26)$$

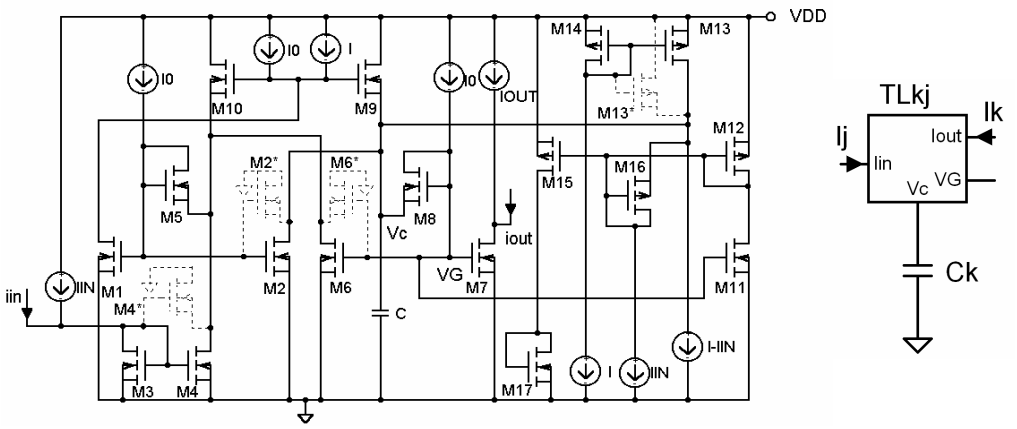
$$(3)\begin{cases} V_T \ln[I_{D1}/I_\Diamond(V_{G1})] - V_T \ln[I_{D2*}/I_\Diamond(V_{G5})] = \\ V_T \ln[I_{D7}/I_\Diamond(V_{G7})] - V_T \ln[I_{D8}/I_\Diamond(V_{G8})] \end{cases} \quad (27)$$

$$(4)\begin{cases} V_T \ln[I_{D14}/I_\Diamond(V_{G1})] - V_T \ln[I_{D13*}/I_\Diamond(V_{G5})] = \\ V_T \ln[I_{D15}/I_\Diamond(V_{G7})] - V_T \ln[I_{D16}/I_\Diamond(V_{G8})] \end{cases} \quad (28)$$

$$(5)\begin{cases} V_T \ln[I_{D1}/I_\Diamond(V_{G1})] - V_T \ln[I_{D5}/I_\Diamond(V_{G5})] + \\ +V_T \ln[I_{D10}/I_\Diamond(V_{G10})] = V_T \ln[I_{D9}/I_\Diamond(V_{G9})] - \\ -V_T \ln[I_{D8}/I_\Diamond(V_{G8})] + V_T \ln[I_{D7}/I_\Diamond(V_{G7})] \end{cases} \quad (29)$$

One can see that the oppositely connected transistor pairs have the same gate voltage. Also, the transistor pairs: M_3-M_{4*}, M_1-M_5, M_1-M_{2*}, M_7-M_8, M_7-M_{6*}, M_{15}-M_{16}, M_{13*}-M_{14} have the same gate voltage. So, the equations (25)-(28) become the classical translinear relations that do not depend on the body effect:

$$\begin{aligned} &I_{D1}/I_{D5} = I_{D3}/I_{D4*} \Rightarrow I_{D4*} = I_{D3}I_{D5}/I_{D1} \\ &I_{D1}/I_{D5} = I_{D7}/I_{D6*} \Rightarrow I_{D6*} = I_{D7}I_{D5}/I_{D1} \\ &I_{D1}/I_{D2*} = I_{D7}/I_{D8} \Rightarrow I_{D2*} = I_{D1}I_{D8}/I_{D7} \\ &I_{D14}/I_{D13*} = I_{D15}/I_{D16} \Rightarrow I_{D13*} = I_{D14}I_{D16}/I_{D15} \\ &(I_{D1}/I_{D5}) \cdot I_{D10} = I_{D9} \cdot (I_{D7}/I_{D8}) \end{aligned} \quad (30)$$



(a) (b)

Fig. 1. The current mode integrator with translinear loop for capacitor current component I_{Cij}.
(a) Circuit schematic; (b) Circuit symbolic representation.

Substituting into (30) the corresponding drain currents results:

$$\begin{aligned} I_{D4^*} &= (i_{in} + I_{IN}) \cdot I_0 / (I_0 + I) \\ I_{D6^*} &= (i_{out} + I_{OUT}) \cdot I_0 / (I_0 + I) \\ I_{D2^*} &= (I_0 + I) \cdot I_0 / (i_{out} + I_{OUT}) \\ I_{D13^*} &= I \cdot I_{IN} / (i_{out} + I_{OUT}) \\ I_{D10} \cdot (I_0 + I) / I_0 &= I_{D9} \cdot (i_{out} + I_{OUT}) / I_0 \end{aligned} \tag{31}$$

But

$$\begin{aligned} I_{D10} &= I_{D4} - I_{D4^*} - I_{D5} + I_{D6} - I_{D6^*} = \\ &= i_{in} + I_{IN} - (i_{in} + I_{IN}) \cdot I_0 / (I_0 + I) - I_0 + \\ &i_{out} + I_{OUT} - (i_{out} + I_{OUT}) \cdot I_0 / (I_0 + I) = \\ &= (i_{in} + I_{IN}) \cdot I / (I_0 + I) + (i_{out} + I_{OUT}) \cdot I / (I_0 + I) - I_0 \end{aligned} \tag{32}$$

and

$$\begin{aligned} I_{D9} &= i_C + I_x - I_0 + I_{D2} - I_{D2^*} = \\ &= i_C + I_x - I_0 + I + I_0 - (I_0 + I) \cdot I_0 / (i_{out} + I_{OUT}) = \\ &= i_C + I_x + I - (I_0 + I) \cdot I_0 / (i_{out} + I_{OUT}) \\ I_x &= (I - I_{IN}) - (I_{D13} - I_{D13^*} - I_{D16}) = \\ &= (I - I_{IN}) - [I - I \cdot I_{IN} / (i_{out} + I_{OUT}) - I_{IN}] = \\ &= I \cdot I_{IN} / (i_{out} + I_{OUT}) \end{aligned} \tag{33}$$

Substituting equations (32) and (33) into general translinear loop equations (31) yields:

$$\begin{aligned} (i_{in} + I_{IN}) I &= (i_C + I_x)(i_{out} + I_{OUT}) \\ (i_{in} + I_{IN}) I &= i_C (i_{out} + I_{OUT}) + I I_{IN} \\ i_{in} I &= i_C (i_{out} + I_{OUT}) \end{aligned} \tag{34}$$

Noting that the capacitor voltage, v_C, is the difference between the gate-source voltages of M_7 and M_8

$$\begin{aligned} v_C &= v_{GS7} - v_{GS8} = V_T \ln(i_{D7} / I_0) = \\ &= V_T \ln (i_{out} + I_{OUT}) / I_0 \end{aligned}, \tag{35}$$

substituting (35) into the capacitor current equation

$$i_C = C \cdot \mathrm{d}v_C / \mathrm{d}t \tag{36}$$

and taking into account the lower equation from the set (34), one gets the capacitor current

$$i_C = \frac{C V_T}{i_{out} + I_{OUT}} \frac{\mathrm{d}i_{out}}{\mathrm{d}t}. \tag{37}$$

Finally we get a linear integrator function:

$$i_{out} = \frac{I}{C V_T} \int i_{in} \, \mathrm{d}t \tag{38}$$

The integrator operates properly as long as the quiescent values of the currents I, I_0, I_{IN}, I_{OUT} are chosen so that the integrator's transistors drain currents should remain strictly positive for the input current range, [14].

4 The Basic Current-Mode Integrator for High Frequencies Applications

The basic current-mode integrator at the bloc diagram level is presented in figure 3.a. and its symbolic representation in figure 3.b. The implementation of this architecture is shown in figure 3.c.

The transfer function of the circuit can be easily obtained from the block diagram (see figure 3.a). The currents through the capacitors C_k are given by the relations:

$$\begin{aligned} s\cdot C_k\cdot V_k^+ &= -K_k\cdot I_{in}^+ - K_k\cdot\frac{g_{m_{2k}}}{g_{m_k}}\cdot I_k^- - K_k\cdot g_{m_{1k}}\cdot V_k^+ \\ s\cdot C_k\cdot V_k^- &= -K_k\cdot I_{in}^- - K_k\cdot\frac{g_{m_{2k}}}{g_{m_k}}\cdot I_k^+ - K_k\cdot g_{m_{1k}}\cdot V_k^- \end{aligned} \quad (39)$$

The output current's dependences of the capacitor voltages are given by:

$$\begin{aligned} I_k^+ &= -g_{m_k}V_{0k}^+ = -g_{m_k}(-g_{m_{2k}}/g_{m_{2k}})V_k^+ = g_{m_k}V_k^+ \\ I_k^- &= -g_{m_k}V_{0k}^- = -g_{m_k}(-g_{m_{2k}}/g_{m_{2k}})V_k^- = g_{m_k}V_k^- \end{aligned} \quad (40)$$

Using these relations (39 and 40) one can find the expressions for the differential and common mode transfer functions:

$$\begin{aligned} &F_{kdd}(s) = (I_k^+ - I_k^-)/(I_{in}^+ - I_{in}^+) = \\ &= \frac{g_{m_k}(V_k^+ - V_k^-)}{\frac{g_{m_{2k}}}{g_{m_k}}(I_k^- - I_k^+) + g_{m_{1k}}(V_k^+ - V_k^-) - s\frac{C_k}{K_k}(V_k^+ - V_k^-)} = \\ &= -g_{m_k}/\left[\left(g_{m_{2k}} - g_{m_{1k}}\right) + sC_k/K_k\right] \\ &F_{kcc}(s) = (I_k^+ + I_k^-)/(I_{in}^+ + I_{in}^+) = \\ &= \frac{g_{m_k}(V_k^+ + V_k^-)}{\frac{g_{m_{2k}}}{g_{m_k}}(I_k^- + I_k^+) + g_{m_{1k}}(V_k^+ + V_k^-) - s\frac{C_k}{K_k}(V_k^+ + V_k^-)} = \\ &= -g_{m_k}/\left[\left(g_{m_{2k}} + g_{m_{1k}}\right) + sC_k/K_k\right] \end{aligned} \quad (41)$$

Using, for the implementation of the blocks $-g_m$, $-g_{m1}$ and $-g_{m2}$, transistors which are sized as follows $(W/L)_{g_{m1}} = a\cdot(W/L)_{g_m}$, $(W/L)_{g_{m2}} = b\cdot(W/L)_{g_m}$, the equations (41) become:

$$\begin{aligned} F_{kdd}(s) &= -g_{m_k}/\left[g_{m_k}(b-a) + sC_k/K_k\right] \\ F_{kcc}(s) &= -g_{m_k}/\left[g_{m_k}(b+a) + sC_k/K_k\right] \end{aligned} \quad (42)$$

A lossless differential integrator is obtained when a = b:

$$\begin{aligned} F_{kdd}(s) &= -K_k\cdot g_{m_k}/(s\cdot C_k) \\ F_{kcc}(s) &= -\frac{K_k\cdot g_{m_k}/C_k}{s + 2\cdot a\cdot K_k\cdot g_{m_k}/C_k} \end{aligned} \quad (43)$$

In order to provide closed-loop common-mode stability the inequality $2\cdot a > 1$ must be satisfied. In our application we choose $a = 1$. The two elements that provide any of the output currents are: a folded-cascode circuit and respectively a part of a differential loop. Therefore the integrator has good immunity to the supply noise.

The output noise of the integrator is direct proportional to the bias current I_B, $\overline{i_{nout}^2} = P_n\cdot I_B$, where P_n depends on technology and temperature. The dynamic range can then be expressed as:

$$DR = \frac{I_{o\max}}{\sqrt{i_{n,out}^2}} = \frac{2\cdot\eta\cdot I_B}{\sqrt{P_n\cdot I_B}} = 2\cdot\eta\cdot\sqrt{\frac{I_B}{P_n}},\ \eta\in(0,1) \quad (44)$$

The minimum supply voltage required for this circuit is given by the relation:

$$V_{DD} > V_{Tn} + V_{DS,sat} + \sqrt{2\cdot I_B/\beta_p} \quad (45)$$

If the finite output transconductor resistances are considered, the differential transfer function becomes:

$$F_{kdd}(s) = -g_{m_k}/\left[g_{m_k}(b-a) + 2g_0 + sC_k/K_k\right] \quad (46)$$

A lossless integrator is obtained when one chooses:

$$b\cdot g_{m_k} + 2\cdot g_0 = a\cdot g_{m_k} \quad (47)$$

According to [15] and [16] the distortion of the integrator can be given by:

- the third intermodulation distortion

$$IM_3 \cong (3/32)\left[i_{0d}/(2I_B)\right]^2 \quad (48)$$

- the THD

$$TDH \cong \left[i_{0d}/(2I_B)\right]^2/32 \quad (49)$$

- the third order harmonic distortion due to the threshold voltage deviation of transistors M_3 and M_4, respectively M_{24} and M_{25}

$$HD_3 \cong \{\Delta V_T/[32(V_{GS} - V_T)]\}\cdot\left[i_{0d}/I_B\right]^2 \quad (50)$$

This integrator can have multiple outputs by simply adding additional output transconductors (similar to –gm, see figure 3.a).

5 The Translinear Current-Mode Filter

As an example for the application of the synthesis technique presented in Section 2 a third order current mode filter have been synthesised. The transfer function of the filter is:

$$t(s) = \frac{1}{s^3 + 2s^2 + 2s + 1} \quad (51)$$

The system parameters {**A**,**b**,**c**,d} generated by the SSAF program [17] for orthonormal IFs are:

$$\mathbf{A} = \begin{bmatrix} 0 & 0,707 & 0 \\ 0 & -1,225 & -2 \\ -0,707 & 0 & 1,225 \end{bmatrix} \quad (52)$$

$$\mathbf{b}^T = \begin{bmatrix} 0 & 0 & 0,798 \end{bmatrix}\ \mathbf{c}^T = \begin{bmatrix} 0 & 0 & 1,447 \end{bmatrix}\ d = 0$$

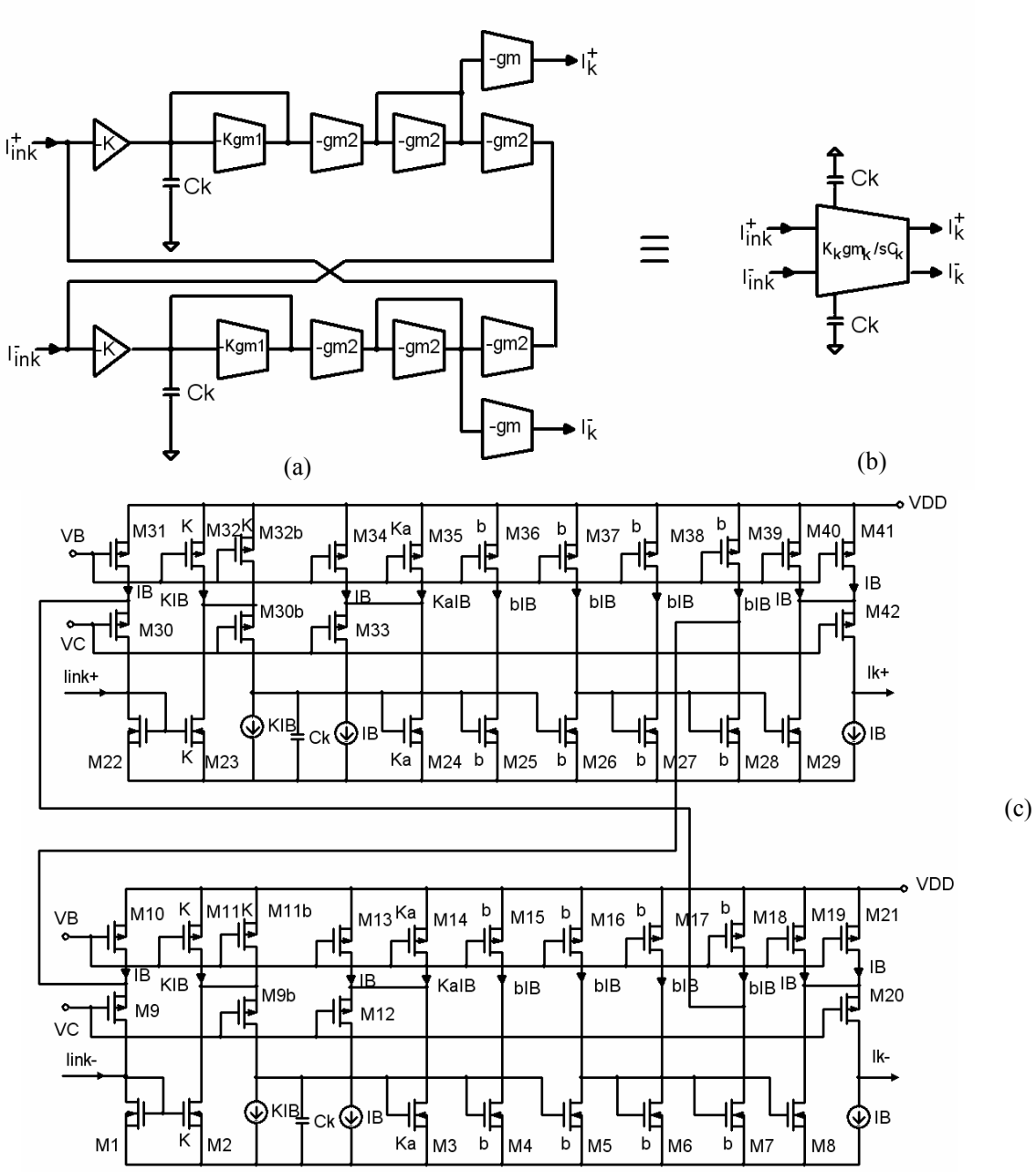


Fig. 3. The current mode integrator for high frequencies applications: (a) block diagram level; (b) circuit symbolic representation; (c) transistor level.

We choosed this type of IFs to be generated by SSAF because the structures to be synthesised using orthonormal intermediate transfer functions generally have good dynamic range, good signal swing and low sensitivity.

The structure of the current mode filter characterised by parameters (52) is presented in Fig. 4 and the system equation are:

$$\begin{aligned} &i_{C1} = i_{C12};\ i_{C2} = i_{C22} + i_{C23} \\ &i_{C3} = i_{C31} + i_{C33} + i_{Cb3};\ i_{out} = c_3\, i_{out3} \end{aligned} \tag{53}$$

Using the relations developed in Section 3 the system (53) becomes:

$$\begin{aligned} &\frac{C_1 V_T}{i_{out1} + I_{OUT1}} \frac{\mathrm{d}\, i_{out1}}{\mathrm{d}\, t} = \frac{i_{out2} I_{12}}{i_{out1} + I_{OUT1}} \\ &\frac{C_2 V_T}{i_{out2} + I_{OUT2}} \frac{\mathrm{d}\, i_{out2}}{\mathrm{d}\, t} = \\ &= -\frac{i_{out2} I_{22}}{i_{out2} + I_{OUT2}} - \frac{i_{out3} I_{23}}{i_{out2} + I_{OUT2}} \end{aligned} \tag{54}$$

$$\frac{C_3V_T}{i_{out3}+I_{OUT3}}\frac{\mathrm{d}i_{out3}}{\mathrm{d}t}=-\frac{i_{out1}I_{31}}{i_{out3}+I_{OUT3}}+ +\frac{i_{out3}I_{33}}{i_{out3}+I_{OUT3}}+\frac{i_{in}I_{b3}}{i_{out3}+I_{OUT3}} \quad (54)$$

$$i_{out}=c_3 i_{out3}$$

and the state-space description of this filter is:

$$\mathrm{d}i_{out1}/\mathrm{d}t=i_{out2}I_{12}/(C_1V_T)$$

$$\mathrm{d}i_{out2}/\mathrm{d}t=-i_{out2}I_{22}/(C_2V_T)-i_{out3}I_{23}/(C_2V_T)$$

$$\mathrm{d}i_{out3}/\mathrm{d}t=-i_{out1}I_{31}/(C_3V_T)+i_{out3}I_{33}/(C_3V_T)+ +i_{in}I_{b3}/(C_3V_T) \quad (55)$$

$$i_{out}=c_3 i_{out3}$$

It is obvious that:

$$a_{12}=I_{12}/(C_1V_T);\ |a_{22}|=I_{22}/(C_2V_T),$$
$$|a_{23}|=I_{23}/(C_2V_T);\ |a_{31}|=I_{31}/(C_3V_T),$$
$$a_{33}=I_{33}/(C_3V_T);\ b_3=I_{b3}/(C_3V_T); \quad (18)$$
$$c_3=\frac{(W/L)_{out\mathrm{MOS}}}{(W/L)_{TLb3}}.$$

The SPICE simulations were performed in order to point out the filter specific performances like bandwidth, noise, distortions and dynamic range. For a supply voltage of 1 V we obtained a cut-off frequency at 1 Khz, a dynamic range grater than 45db and a power consumption smaller than 0.5 mW.

6 The Third Order Current-Mode Filter with MOS transistors that operate in strong inversion

We needed a low pass filter with the normalised transfer function given by the following expression:

$$t(\mathrm{s})=\frac{\mathrm{s}^2+5}{8\mathrm{s}^3+13\mathrm{s}^2+17\mathrm{s}+10} \quad (57)$$

The system parameters {**A**,**b**,**c**,d} resulted using SSAF [17]. According to this program the best realization from the point of view of sensitivities, noise and dynamic range are the one obtained using the orthonormal IFs.

So, the system parameters {**A**,**b**,**c**,d} for the orthonormal IFs are:

$$\mathbf{A}=\begin{bmatrix}0 & -0,877 & 0\\ 0,877 & 0 & -1,164\\ 0 & 1,164 & -1,625\end{bmatrix} \quad (58)$$

$$\mathbf{b}=\begin{bmatrix}0 & 0 & 0,719\end{bmatrix}\quad \mathbf{c}=\begin{bmatrix}0 & 0,174 & 0,720\end{bmatrix}\quad d=0$$

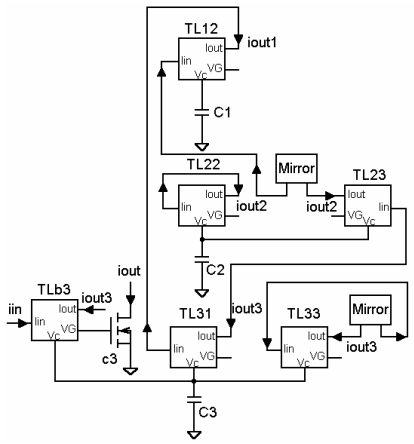


Fig. 4. The third order translinear filter structure.

The structure of the current mode filter characterised by parameters (58) is presented in figure 5 and the system equation are:

$$\begin{aligned}\dot{i}_{1d}&=a_{12}\cdot i_{2d}\\ \dot{i}_{2d}&=a_{21}\cdot i_{1d}+a_{23}\cdot i_{3d}\\ \dot{i}_{3d}&=a_{32}\cdot i_{2d}+a_{33}\cdot i_{3d}+b_3\cdot i_{ind}\\ i_{outd}&=c_2\cdot i_{2d}+c_3\cdot i_{3d}\end{aligned} \quad (59)$$

Using the relations developed in previous section we obtained the following normalised values:

$$K_1\cdot g_{m1}/C_1=0,877,\ a_{12}^*=1$$
$$K_2\cdot g_{m2}/C_2=0,877,\ a_{21}^*=-1,\ a_{23}^*=2 \quad (60)$$
$$K_3\cdot g_{m3}/C_3=1,164,\ a_{31}^*=-1,\ a_{32}^*=1,4,\ b_3^*=0,626$$

For the filter's realisation one used differential integrators with multiple outputs and current amplifiers. The structure of a multiple current amplifier is presented in figure 5. One can see the folded cascod topology of the current amplifier used to obtain better dynamic performances.

For simulation, SPICE parameters supplied by the American Microsystems Inc. for CMOS 1 μm technology were used.

The SPICE simulations were performed in order to point out the filter specific performances like bandwidth, noise, distortions and dynamic range. For a supply voltage of 3 V we obtained a cut-off frequency at 11 Mhz, a dynamic range grater than 50db for a 20 μA differential output current and a power consumption around 5mW. The simulated distortion was less than 1% at this signal level. The power supply rejection ratio was slightly greater than 50dB. The minimum operation voltage for our structure is about 1,4V.

Much higher performances could be achieved, using this synthesis technique, with a more advanced technology.

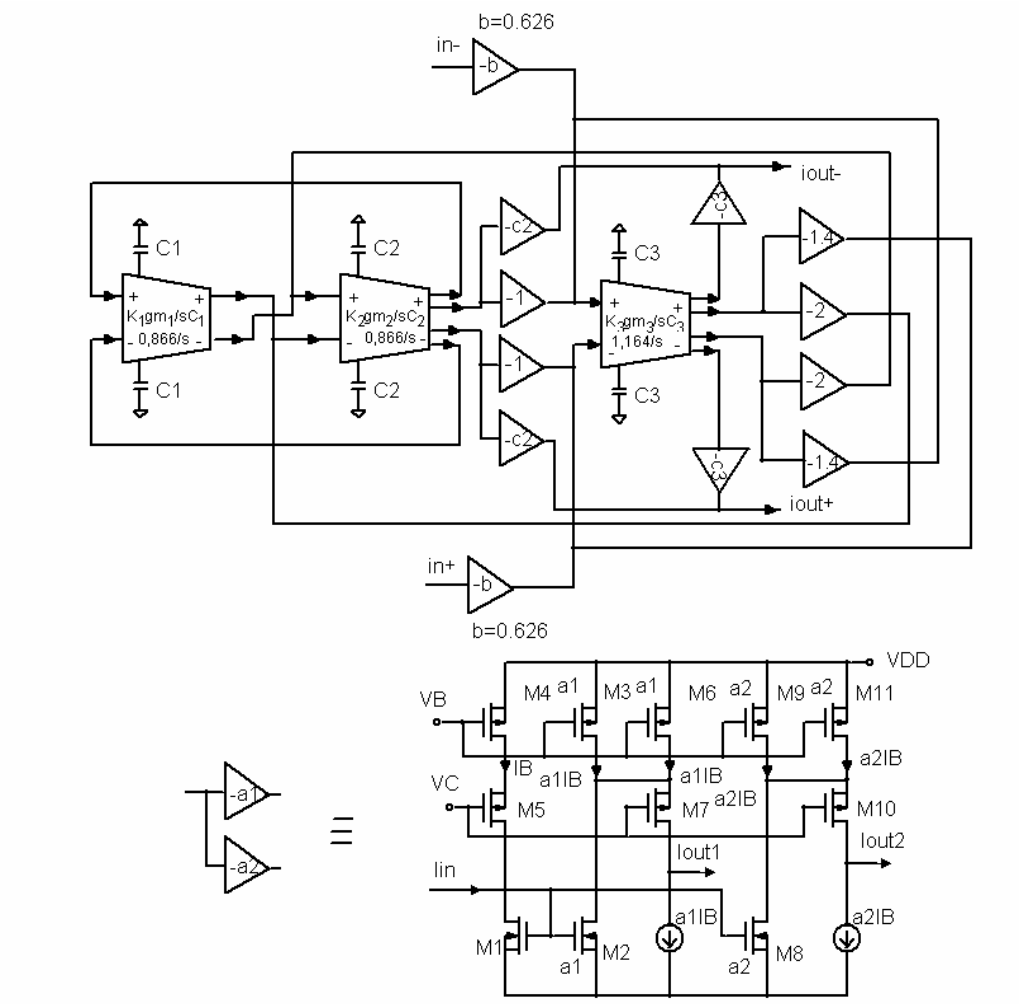


Figure 5. The third order filter structure.

5 Conclusions

Future analogue circuits will have to operate successfully at supply voltages slightly higher than the MOS transistor threshold voltage. So, the suitable topologies for signal processing at such low values of supply voltages are the circuit that operate in current domain because in this way the very small voltage swings are avoided.

This paper presents a technique for low supply voltage, continuous-time, current mode filters synthesis based on the intermediate transfer functions method. This method has the distinct advantage of filter performance optimization at the abstract level of IFs, not at the topological level. The paper also presents two basic cells suitable for low-voltage filter – the translinear current mode integrator, suitable for static and dynamic analogue signal processing at very low supply voltage operation, and the current mode integrator suitable for high frequencies applications. The minimum value of the supply voltage required for these circuits are given by:

- The sum of the MOS transistor threshold voltage and the drain-source saturation voltage for the translinear structure (approx. 1V).
- The sum of the MOS transistor threshold voltage, the V_C voltage and the drain-source saturation voltage (approx. 1.4V).

Finally, we synthesized two different low pass filters in order to test the proposed synthesis methods. In the first of them, all transistors operate in weak inversion due to the requirements of translinear principle - an exponential I-V characteristic. So, one can achieve very low power, but the circuits will be sensitive to the threshold voltage matching and the cut-off frequency is not very high. In the second filter, all transistors operate in strong inversion and we obtain the following

characteristics, pointed out from SPICE simulation: cut-off frequency at 11 MHz, dynamic range grater than 50db for a 20 μA differential output current and power consumption around 5mW. In both cases, much higher performances could be achieved, using these synthesis techniques, with a more advanced technology.

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