Examination of Non-Uniform Distribution of Current on Worst-Case Crosstalk Noise for Distributed RLC Interconnect

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Abstract - Considering circuit designs at the deep sub-micron level, the more that interconnect wires of small cross section are packed closer together, coupled with longer length of interconnect and an increase in the number of layers of interconnect may cause different parts of an interconnect line to experience a varying degree of coupling effect from other interconnects, with the consequent variation in the induced-current across the interconnect. An analytical model to examine the effect of non-uniform distribution of current on the mutual inductance and capacitance between on-chip interconnects is presented.

Key-Words: - Interconnect, crosstalk, noise, distributed RLC

1 Introduction

As process technology scales to the deep submicron (DSM) regime, the delays due to the electrical characteristics of interconnect as well as their parasitic cross-coupling tendency – i.e. crosstalk noise - have become the most dominant factor in determining the performance and reliability in high performance integrated circuits. Crosstalk noise is defined as the noise voltage on signal lines caused by a change of state in neighbouring lines [1]. The line affecting its neighbour by its switching state is often referred to as the aggressor line, while the affected one as the victim line. Crosstalk noise can lead to performance degradation and functional failure depending on the state of the conduction wire and its adjacent neighbours and of equal importance, i.e. depending on the width, peak amplitude and frequency of the generated parasitic noise [1]. Therefore, the worst-case on-chip performance degradation often occurs when crosstalk between interconnects due to capacitive and inductive parasitic coupling is considered [2] [3]. Development toward DSM technology requires that such consideration has to be taken into account to accurately and efficiently estimate interconnect crosstalk-induced noise.

To address the crosstalk-induced delay and noise issues, a number of schemes were proposed and used at different VLSI design stages. Net ordering, buffer or repeater insertion based on the principle of divide and conquer have been employed at the physical level. Such techniques may not be used in present and future VLSI as the opportunity for internal chip space becomes unavailable. Furthermore, using such techniques does not necessarily guarantee an acceptable interconnect performance of the circuit at chip level. Other techniques such as wire shielding and spacing and more recently, the encoding of the transmitted data were proposed to reduce crosstalk noise. However, it must be emphasised that the impact of parasitic coupling on interconnect delay is not only data-dependent but is also dependent on the specific combination of each individual wire and their adjacent neighbours [4][5][6].

Prior to VLSI, on-chip interconnects were modelled as lumped capacitance, then as lumped and distributed *RC* lines. At those stages, the concern for circuit performance was addressed using the Elmore delay model to estimate delays in an *RC* tree. Although popular due to its simplicity, the Elmore delay can produce pessimistic results - sometimes underestimating the delay up to error magnitudes as much as 60% [7]. Furthermore, moving toward DSM integration, coupled with the use of high clock frequencies, has resulted in the average length of an interconnect line being often resistive compared to its driver resistance; therefore

requiring that the inductive and distributed nature of on-chip interconnect has to be properly modelled. In order to account for the signal-distorting effects the use of high operation frequency, present interconnects require to be modelled as distributed RLC lines. A four-poles based model for distributed RLC lines was presented in [8]. Although the accuracy has been improved in comparison with that of the two poles expression [9], no closed form solution was developed. In reference [4], an RLC model based on Fourier analysis for delay and crosstalk prediction was proposed, with higher accuracy is obtained by including more harmonics in the model. Several works have modelled capacitive crosstalk using distributed networks [10][11][12]. However, all above works assume uniform distribution of current across the interconnect line. Advances in DSM technology have resulted in that longer interconnect wires of small cross section are packed closer together. This may give rise to the possibility that different parts of an interconnect line – i.e. the victim line - may experience a varying degree of coupling effect from other interconnects – i.e. aggressor lines – with the consequent variation in the induced-current across the victim line. The work in this paper is based on the model developed in [13] to examine the effect of non-uniform distribution of current on the estimation of crosstalk noise.

This paper is organised as follows. Section 2 presents the mathematical modelling of a distributed RLC, including time-domain expressions of the line voltage response under finite and infinite ramp input. Section 3 introduces the distributed-coupled *RLC* transmission line model for the crosstalk noise estimation. Section 4 presents the experimental simulation results. Conclusions are given in Section 5.

2 Mathematical Modelling

A distributed *RLC* interconnect of length *d*, with driver resistance and load capacitance is depicted in Fig.1.

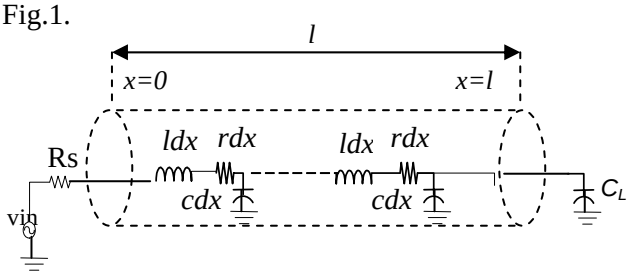


Fig.1. Distributed *RLC* transmission Line

From Fig.1:

$$z\partial x = (r + sL)\partial x \quad (1)$$

$$y\partial x = sC\partial x \quad (2)$$

$$\partial V = (v + \partial V) - V \quad (3)$$

Using (1), (2) and (3), the voltage and current equations for the interconnect line, shown in Fig.1, are as follows:

$$V = v_1 e^{\partial x} + v_2 e^{-\partial x}\Big|_{\partial x=\sqrt{ZY}} \quad (4)$$

and

$$I = v_3 e^{\partial x} + v_4 e^{-\partial x}\Big|_{\partial x=\sqrt{ZY}} \quad (5)$$

At x = 0:

$$V_1 = 0.5V_s + 0.5\sqrt{Z/Y}\,I_s \quad (6)$$

and

$$V_2 = 0.5V_s - 0.5\sqrt{Z/Y}\,I_s \quad (7)$$

Substituting (6) and (7) in (4) and applying the boundary conditions at the end of the line:

$$\begin{bmatrix} V_S \\ I_s \end{bmatrix} = \begin{bmatrix} \cosh(dl) & Z_C \sinh(dl) \\ \frac{1}{Z_C}\sinh(dl) & \cosh(dl) \end{bmatrix} \begin{bmatrix} V_o \\ I_O \end{bmatrix} \quad (8)$$

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1 & R_s \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cosh(dl) & Z_C \sinh(dl) \\ \frac{1}{Z_C}\sinh(dl) & \cosh(dl) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sCL & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_O \end{bmatrix} \quad (9)$$

where Z_C is the characteristic impedance of the distributed line is

$$Z_C(s) = \sqrt{\frac{l}{c}}\sqrt{1 + \frac{r}{sl}} \quad (10)$$

r, l and c are respectively the per unit length resistance, inductance and capacitance of the line.

Assuming the line is terminated with load capacitance C_L, the transfer function of the distributed line is given by:

$$H_P(s) = \frac{1}{1 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4} \quad (11)$$

where the b_i's coefficients are as in [13], with the infinite ramp-response v_{inf}:

$$v_{\inf}(t) = \frac{V_{DD}}{T_R}\left[-b_1 + t + \sum_{i=1}^{4} d_i e^{s_i t}\right] u(t) \quad (12)$$

where T_R is the finite ramp rise time.

The time-domain response of a finite ramp $v_{fin}(t)$ is [13]

$$v_{fin}(t) = v_{\inf}(t) - v_{\inf}(t - T_R)$$

$$= \frac{V_{DD}}{T_R}\left[T_R + \sum_{i=1}^{4} d_i\left(e^{s_i t} - e^{s_i (t-T_R)}\right)\right]u(t) \quad (13)$$

where d_i and poles s_i represent the residues and poles of the function, respectively.

3 Worst-Case Crosstalk Noise

Depending on the layout of a highly complex integrated circuit, different parts (section, or segment) of an interconnect line may experience different cross-coupling effects. Consequently, this may yield variation in, for instance, the amplitude of the current across the victim line. This may give rise to different coupling inductive and capacitive effects on different parts (sections) of an interconnect line, with the subsequent variation in the self and mutual inductance and capacitance of the line. The work in this paper assumes that the victim line is split into n sections (0 < n), with only a subset of n having experiencing variations in the current.

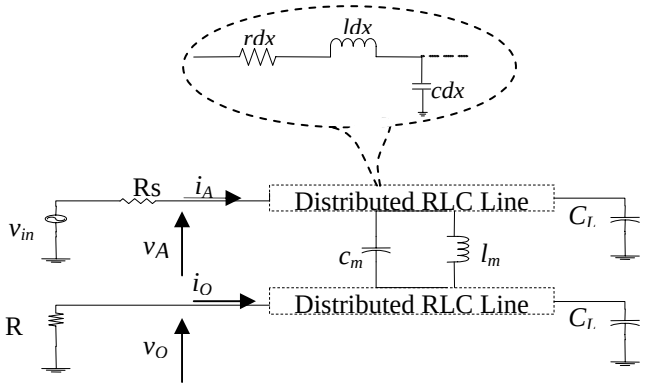


Fig.2 Coupled distributed RLC Line

The relationship between the coupled lines is given by [2][10]:

$$\frac{\partial^2 V^+(x,t)}{\partial x^2} = \lambda_1^2 V^+(x,s) \quad (14)$$

$$\frac{\partial^2 V^-(x,t)}{\partial x^2} = \lambda_2^2 V^-(x,s) \quad (15)$$

where V^+ and V^- represent the voltage at the end of the line in common and differential mode, respectively.

$$\lambda_1 = s\sqrt{c(l+l_m^{\sim})}\sqrt{1+\frac{r}{s(l+l_m^{\sim})}} \quad (16)$$

$$\lambda_2 = s\sqrt{(c+2c_m^{\sim})(l-l_m^{\sim})}\sqrt{1+\frac{r}{s(l-l_m^{\sim})}} \quad (17)$$

where

$$l_m^{\sim} = Kl_m\Big|_{\|K\|<0.2} \text{ and } \quad c_m^{\sim} = Qc_m\Big|_{\|Q\|<0.2} \quad (18)$$

K and Q are multiplicative constants representing a small fractional change in the mutual inductance and capacitance.

Non-uniform distribution current may introduce a fractional increase or decrease in the nominal value - i.e. when the current is evenly distributed - of the mutual inductance and capacitance as well as the self-inductance and self-capacitance of the interconnect line. In this paper, the fractional change in current is considered to be step-wise increasing from the nominal value. For an interconnect line represented by n sections, where the length of each section is defined as the unit length:

$$l_m^{\sim} = l_m^{\sim,1} + l_m^{\sim,2} + ... + l_m^{\sim,n-1} + l_m^{\sim,n} \quad (19)$$

and

$$c_m^{\sim} = c_m^{\sim,1} + c_m^{\sim,2} + ... + c_m^{\sim,n-1} + c_m^{\sim,n} \quad (20)$$

with

$$l_m^{\sim,i} = \kappa^i l_m\Big|_{\kappa^i \subset K}, \quad \text{and} \quad c_m^{\sim,i} = q^i l_m\Big|_{q^i \subset Q} \quad (21)$$

i:integer ($i > 0$).

To account for the non-uniform distribution of current, the transfer function of the distributed RLC line in (11) can be represented as follows:

$$H_p(s) = \frac{1}{1 + b_1^T s + b_2^T + s^2 + b_3^T s^3 + b_4^T s^4} \quad (22)$$

with

$$b_i^T = b_i + b_i^{\sim}\Big|_{i>0} \quad (23)$$

where b_i s and $b_i^{\sim}$ are the nominal coefficients of H_p, as in [13], and the fractional change in b_i s as a result of non-uniform distribution of current, respectively. In the case of the former, the overall mutual inductance l_m and mutual capacitance c_m of the line can be represented as:

$$l_m = \sum_{i=1}^{i=n} l_m^i, \quad c_m = \sum_{i=1}^{i=n} c_m^i \quad (24)$$

or

$$l_m = \sum_{i=1}^{i=n} \kappa^i l_m, \quad c_m = \sum_{i=1}^{i=n} q^i c_m \quad (25)$$

The overall inductance and capacitance of the line can be represented as:

$$L = \sum_{i=1}^{i=n} l^i + \sum_{i=1}^{i=n} l_m^i, \quad C = \sum_{i=1}^{i=n} c^i + \sum_{i=1}^{i=n} c_m^i \quad (26)$$

For the fractional change in the mutual inductance and mutual capacitance as a result of variation in the current across the interconnect line.

$$l_m^{\sim} = \sum_{i=1}^{i=n} l_m^{\sim}, \quad c_m^{\sim} = \sum_{i=1}^{i=n} c_m^{\sim} \tag{27}$$

Under worst-case noise, the use of equations (13) and (15) to determine the coupled lines voltage responses require the following adjustments

$$C_{eff} = c + 2c_m^{\sim}, \quad l_{eff} = l - l_m^{\sim} \tag{28}$$

where c_{eff} and l_{eff} represent the effective capacitance and effective inductance, respectively. The respective infinite and finite time-domain responses of the aggressor line under ramp input could be determined based on the expression of the single line as follows:

$$v_{Ainf}(d,t) = v_{inf}(d(l_{eff}, c_{eff}), t) \tag{29}$$

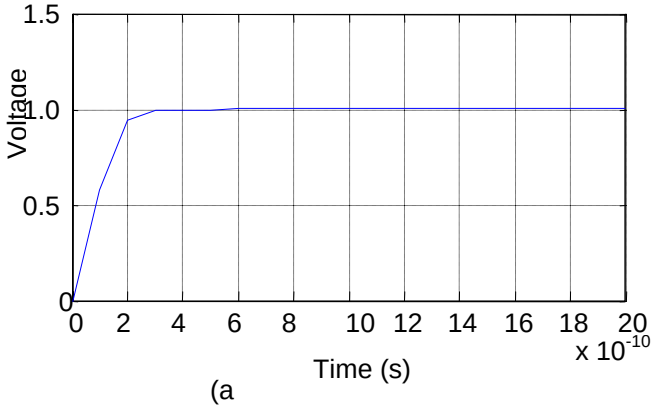
$$v_{Afin}(d,t) = v_{fin}(d(l_{eff}, c_{eff}), t) \tag{30}$$

Equally, under this worst-case scenario, the time-domain response of the noise peak voltage at end of the victim line is given by [2]:

$$v_V(d,t) = \frac{1}{2}(v_{fin}^{+}(d,t) - v_{fin}^{-}(d,t)) \tag{31}$$

4 Simulation Results

To assess the effect of non-uniform distribution of current on the crosstalk noise induced by the aggressor line on the victim line, a typical interconnect of length 2000 is used. The per length mutual inductance, resistance and capacitance are 0.246pf, 0.0015Ω and 0.000176pf respectively. The source resistance and load capacitance are 100 Ω and 0.01 *pf*, respectively. For comparison purposes, we used the results from obtained from Spice to examine the extent to which variation in the current across an interconnect line influence the crosstalk noise peak-voltage at the end of the victim line. Fig.3 shows a noticeable increase in the crosstalk noise voltage when the change in he mutual inductance – caused by variations in the current – exceeds 5% of the nominal value.



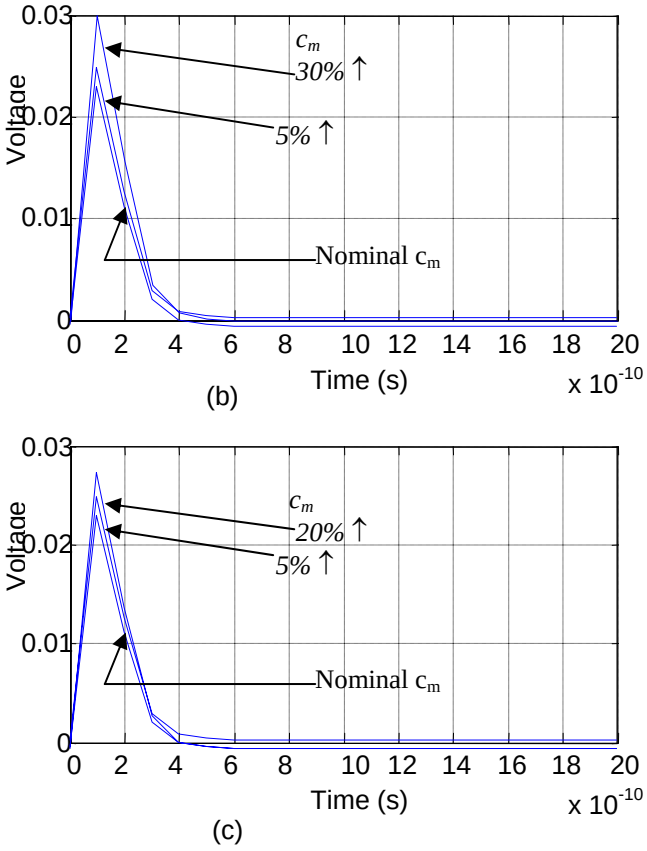


Fig.3 (a) Aggressor line Transient response, (b)and (c) Noise peak estimation for varying c_m.

5 Conclusion

As on-chip interconnects are packed closer together, coupled with the increase in the operating frequency, different parts (sections) of an interconnect line may experience varying coupling effects. This may give rise to variation in the current across the interconnect line, with subsequent fluctuations in its self and mutual inductance and capacitance. This analytical approach proposed in this paper takes into account non-uniform distribution of current across interconnect lines – thus accurate estimation of crosstalk noise and its induced time-delay.

References:

[1] T. Sakurai and K. Tamaru, “Simple formula for two and three dimensional capacitances,” IEEE Trans. Electron Devices, vol. ED-30, No. 2, 1983, pp. 183-185.

[2] L. Coulibaly and J. H. Kadim, ”Analytical Crosstalk Noise and Its Induced-Delay Estimation for Distributed RLC

Interconnects under Ramp Excitation," IEEE Int. Symp. on Cir. and Sys., Japan, 2005, pp 1254-1257.

[3] A. Deutsch , "When are transmission-line effects important for on-chip interconnects?," IEEE Trans. Microwave Theory Tech. Vol. 45, pp. 1836-1846, Oct. 1997.

[4] G. Chen and E. Friedman, "An RLC interconnect model based on Fourier analysis," IEEE Trans. Computer-Aided Design, vol. 24, no.2, 2005, pp. 170-183.

[5] H.J. Kadim, L.M. Coulibaly, "EM-based Analytical Model for Estimation of Worst-Case Crosstalk Noise", Proc. of IEEE Int. Symposium on Circuits and Systems, Kos, Greece, paper accepted for presentation on 21-24 May 2006.

[6] H.J. Kadim, "Predictive State-Space for on-Chip Crosstalk Noise", Proc. of the IEEE EUROCON International Conference on Computer as a Tool, Warsaw, September 2007, pp.2576-25-79

[7] K. Banerjee and A. Mehrotra, "Analysis of on-chip inductance effects for distributed RLC interconnects", IEEE Transactions on Computer-Aides design of Integrated Circuits and Systems, vol. 21, No. 8, August 2002

[8] K. Banejee and A. Mehrotra, "Accurate analysis of on-chip inductance effects and implications for optimal repeater insertion and technology scaling," in Proc. IEEE Symp. VLSI Circuits, 2001, pp.195-198.

[9] A.B. Kahng and Muddu, "An analytical delay model for VLSI interconnects," IEEE Trans. Compter-Aided Design Integ. Circuits and Systems, vol. 16, no.12, 1997, pp. 1507-1514.

[10] H.J. Kadim, "State-Space for Examination of Cross-Coupling Effects on Circuit Parameters", WSEAS Trans. on Circuits and Systems, Issue 8, Vol. 5, No.1, 2006, pp. 1147-1152, ISSN: 1109-2734.

[11] H.J. Kadim, L.M. Coulibaly, "Time-delay Estimation: Two Comparative Models for Distributed On-Chip RLC Interconnects under Ramp Excitation," Proc. of the 23rd Norchip Conference, Oulu, Finland, November 2005, pp245-248.

[12] H.J. Kadim, "State-Space based Analytical Modelling of on-Chip Coupling Effects", In the Proc. of WSEAS Inter. Conf. on Circuits and Systems, Athens, July 2006, pp.70-74

[13] L. Coulibaly and J. H. Kadim, "Analytical Ramp Delay Model for Distributed On-Chip RLC Interconnects," *47th IEEE International Midwest Symp. on Circuits and Systems*, Japan, July 2004, pp. I 457-I 460.