# Design and Analysis of 4-GHz SOP FMCW HMIC Radar

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*Abstract:* - The demand for higher performance systems that are smaller and have the potential to be more cost effective has lead hardware designers to adopt integration of many components and modules in a package (SOP) or on a chip (SOC). A compact SOP (single-substrate) L-band FMCW HMIC radar module for high-resolution sensor application has been demonstrated. For use with a single transmit-receive antenna, a miniature microstrip hexaferrite circulator has been integrated to the transceiver module. The module was based on a transceiver HMIC with an integrated branch divider and 5-port ring coupler to enable both broadband modulation and single-antenna operation. The integrated substrate size could be reduced to 40 $cm^2$. The analysis of the designed radar is introduced which reflects a good performance and achieves a higher efficiency.

*Key Words:* - Computational Microstrip Circuit Design, Microwave Circuits, Computer Aided Design

## 1 Introduction

Microwave integrated circuits (MICs) have been increasingly adopted in many electronic civilian and military systems such as satellite communications, radar, electronic warfare, navigation, guidance systems. Comparing with the conventional waveguide and coaxial microwave circuits, MICs have advantages of high reliability, good performance, reproducibility, small size and low cost. Three general types of components can be utilized for MICs: (1) Distributed transmission lines (microstrip, coplanar, stripline, etc., (2) Lumped elements (resistors, inductors, and capacitors), (3) Solid-state devices (field-effect transistors, bipolar junction transistors, Schottky-barrier diodes, etc.)[1-4]

Microstrip line, which is a transmission line consisting of a strip conductor and a ground plane separated by a dielectric medium, is used extensively in fabrication of MICs because of the following particularly useful characteristics [1-2]: (1) The microstrip lines are easily fabricated with low cost, (2) the network interconnection and placement of the lumped elements and active devices are easily made on its metal surface, (3) DC as well as AC signals can be transmitted, (4) line wavelength is reduced considerably because of the substrate fields; hence distributed component dimensions are relatively small, and (5) the structure is quite rugged and can withstand moderately high power level.

Recently many works have been performed for the design and fabrications of the individual parts of the microwave transceiver circuit such as amplifiers, oscillators and mixers using microstrip technique. In the beginning of 1990 [4-9], the works of fabrication of a complete microstrip transceiver has been started especially for the military applications. This paper will be considered as an extension of the previous work that produce a perfect and reliable L-band transceiver with Microstrip Patch Antenna (MPA) to be used in civilian application especially in wireless communications.

## 2 HMIC Technology and SOP Package

The evaluation of HMICs began in 1955 when the microstrip line was introduced. In HMIC, active device such as transistors and diodes, passive discrete components such as, inductors, capacitors, and resistors and distributed passive components such as filters, couplers, and combiners are attached externally to an etched circuit on alumina (the most common microwave ceramic) or some soft substrate.

HMIC technology has matured to the extend that microwave single-function circuits (including amplifiers, oscillators, switches, phase shifters, and mixers) and multifunction circuits (including transmitters, and receivers) were in large-scale production. The current trend in the HMIC technology is to reduce the system cost by integrating as many components and circuits functions on a single substrate. The System On Package (SOP) is the current trend of HMIC where multifunction circuits including transmitter and receiver are fabricated on a single substrate[10]. HMIC microstrip FMCW radar is a good example that illustrates HMIC to built SOP. The following sections illustrate the recent extension of HMIC to build a complete system on a package.

## 3 4-GHz SOP FMCW HMIC Radar

Figure 1 shows the block diagram of the designed FMCW radar. Figure 2 shows the layout of the fabricated HMIC transceiver and MPA array. The designed FMCW radar has three modules. The first module is a microstrip receiver contains 4 GHz broadband microstrip amplifiers (BMA), and singly balanced diode mixer (SBDM) with 5-port ring coupler. The second module is a microstrip transmitter operated at 4 GHz. It comprises a 4 GHz CW microstrip oscillator (CWMO) and a 7db power splitter using microstrip branch coupler (MBC). The third module is a microstrip-patch antenna (MPA) resonated at 4 GHz. The first two modules are integrated on a single package (substrate) where the MPA are attached through a ferrite circulator.

Figure 3 shows the layouts of designed HMIC transceiver and MPA array configurations connected with the external ferrite circulator and the DC power supply. The circuit uses singly balanced diode mixer with rate-race hybrid. The input signals for the rate-race hybrids are: 1) the reference LO input signal comes from 4-GHz CWMO through the coupled port of 7 dB MBC and 2) the received RF signal comes from 4-elements MPA array through a circulator and 4-GHZ BMA. The IF output signal is extracted from the mixer output through microstrip low-pass filter (LPF). The transmitted CW signal is directed to the MPA through the direct port of the 7 dB rectangular coupler [4-9]. The design of the 4 GHz SOP FMCW HMIC Radar is performed completely with the aid of the developed full-scale computer program developed by the author and others [11-12]. The microstrip substrate parameters with 50-Ω normalized impedance are: relative permittivity ($\varepsilon_r$) = 6.15, substrate height (H) = 0.635 mm, and conductor thickness (T) = 0.005 mm. The designed modules were analyzed and optimized using the recent packages such as APLAC, PUFF, and C/NL2 [13-15]. The designed modules were fabricated at the electronic research development center (Dar El-Salaam, Cairo, Egypt).

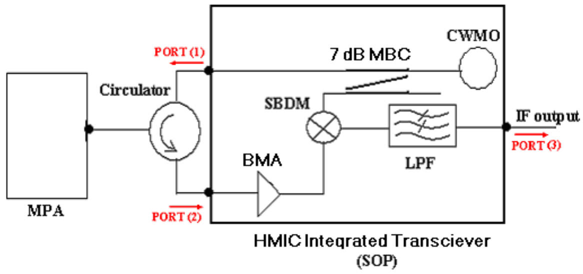


Fig. 1: Block diagram of the HMIC SOP Radar

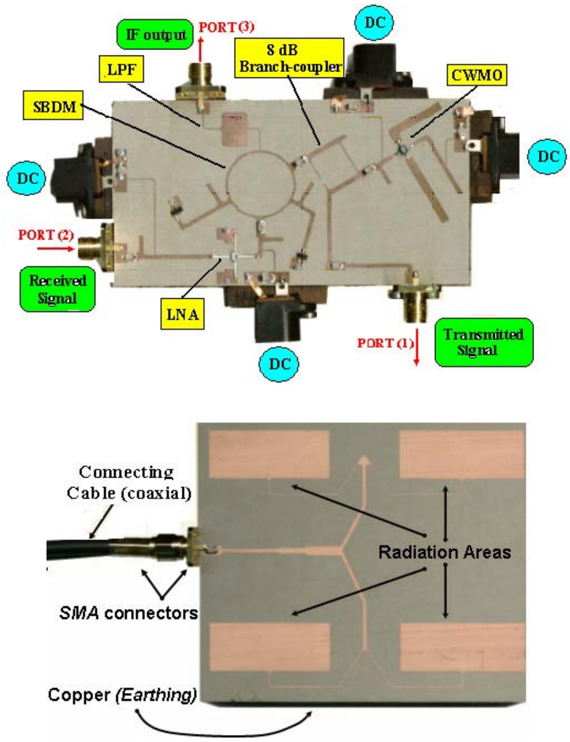


Fig. 2: The layout of designed HMICs transceiver and MPA array

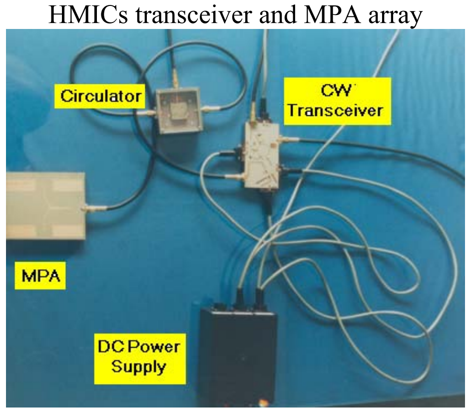


Fig. 3: The layout of HMICs transceiver and MPA configurations connected with ferrite circulator and the DC power supply

### 3.1 Design of the 4 GHz CWMO

Transistor oscillators can be designed using either bipolar or GaAs FET devices [1-9, 16-19]. Using the [S] parameters of the active element, the design of the microwave oscillator is performed using our full-scale computer simulation program. The scattering parameters of the used transistor (HXTR

42086) at 4 GHz and $I_c$ = 10 mA are: $S_{11}$= 0.75∠115°, $S_{12}$=0.122∠51°, $S_{21}$=1.51∠14° , and $S_{22}$=0.3 ∠80°.

The stability of the used transistor at the frequency of 4 GHz is calculated through calculation of the stability factor, K, and Δ[8, 14, 16]. For the given [S] parameter of the used transistor at the operated frequency the values of K and Δ are - 0.174, and 1.05 ∠90°. respectively. They reflect the transistor potential unstability.

The terminating circuit is designed to get maximum reflection coefficient at the transistor output. The analytical design of the terminating circuit and the output matching circuit are performed using the developed computer program [11, 12]. As a result of the developed program and the optimization process described elsewhere [16-19] the lengths and widths of the termination and matching circuits are:

***Terminating Circuit: Length*** of open circuit series line (50 Ω)= 22.4569 mm, and width of open circuit series line = 1 mm.

***Load matching circuit:*** Length of series line (50 Ω) =5.318 mm, width of series line = 1 mm, length of open single shunt stub = 5.105 mm, and width of open balanced shunt stub = 1 mm.

A series feedback is added to the base of the transistor using microstrip line to maximize the value of $S_{11}$ of the oscillator operated at 4 GHz. As the result of the optimization process the length and width of the microstrip line connected to the base of the transistor are 18.944564mm **and** 2 mm, respectively. Figure 4 shows the circuit layout of the designed 4 GHz CWMO.

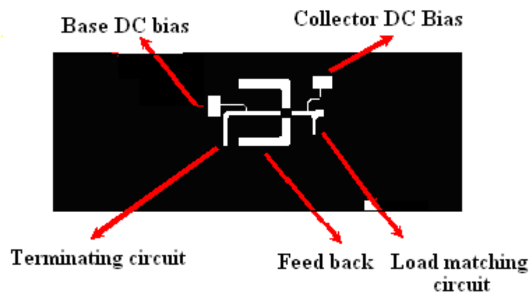


Fig.4: circuit layout of the deigned 4 GHz CWMO

Figure 5 shows $|S_{11}|$ in dB versus frequency for the deigned 4 GHz microstrip oscillator using C/NL2 package.

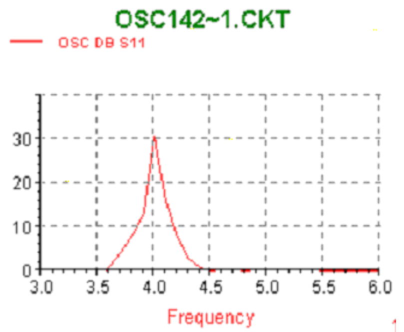


Fig. 5: $|S_{11}|$ (dB) versus the frequency for 4 GHz microstrip oscillator.

## 3.2 Design of 4 MPA

MPA consists of a conducting patch of any planar geometry on one side of a dielectric substrate backed by a ground plane on the other side [20-22]. Such antennas received considerable attention starting in 1970s and are used now to implement HMIC and MMIC transceiver modules. There are numerous substrates that can be used for the design of microstrip antennas, and their dielectric constants are usually in the range of ( $2.2 \le \varepsilon_r \le 12$ ). The substrates that are most desirables for antenna performance are thick substrates whose dielectric constants are in the lower end of the range. This provides better efficiency, larger bandwidth, and loosely bound fields for radiation into space, but at the expense of larger element size. On the other hand, the microwave circuit attached to the antenna requires thin substrate with high dielectric constant since this ensures tightly bound fields. Hence the undesired radiation and coupling can be minimized. In addition the microwave circuit size can be reduced. Since microstrip antennas are integrated with the circuit in our module, a compromise has to be reached between good antenna performance and circuit design. The microstrip substrate whose parameters are given in the previous section was found to represent the optimum compromise. A computer program is developed in order to design the MPA and to calculate its parameters. The equations used in the program are based on using the transmission-line model for the antenna [20-24]. The E-plane and the H-plane patterns are based on using the cavity model [20-22]. Figure 6 shows a sample run of the computer program for MPA design.

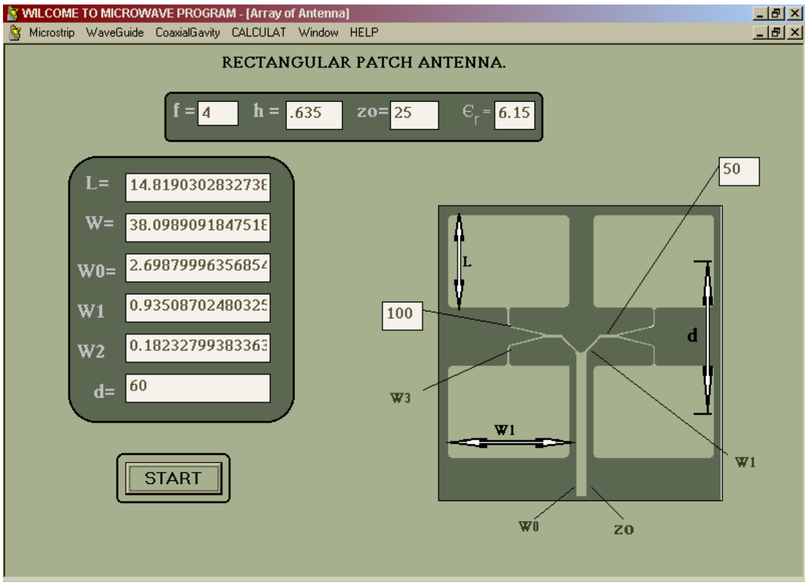

Fig. 6: Sample run of the computer program for MPA design

As a result of the program, the parameters of the designed MPA are: Distance between two section of array = 6 cm, length of batch antenna = 14.819mm, width of batch antenna = 38.099mm, width of 25Ω line = 2.6988 mm, width of 50Ω = 0.935087mm, width of 100Ω = 0.18232mm, the computed input resistance is 200 Ω.

### 3.3 Design of 7 dB MBC

The 7 dB MBC is used to direct the CWMO output to the MPA through a circulator and to couple a reference signal to the SBDM. The developed full-scale computer simulation program is used to design the 7 dB rectangular branch coupler operated at central frequency $F_o$=4 G Hz. As a result of the developed program, the parameters of the 7 dB rectangular branch coupler are: width of series lines = 1.11819 mm, length of series lines = 8.8553 mm, impedance of series lines = 44.7346 Ω, width of branch lines = 0. 180118 mm, length of branch lines = 9.4026 mm, impedance of branch lines = 100. 1483 Ω. Figures 7 through 9 show the circuit analysis, and schematic circuit description for the designed 7 dB MBC using APLAC and PUFF packages [13, 14]

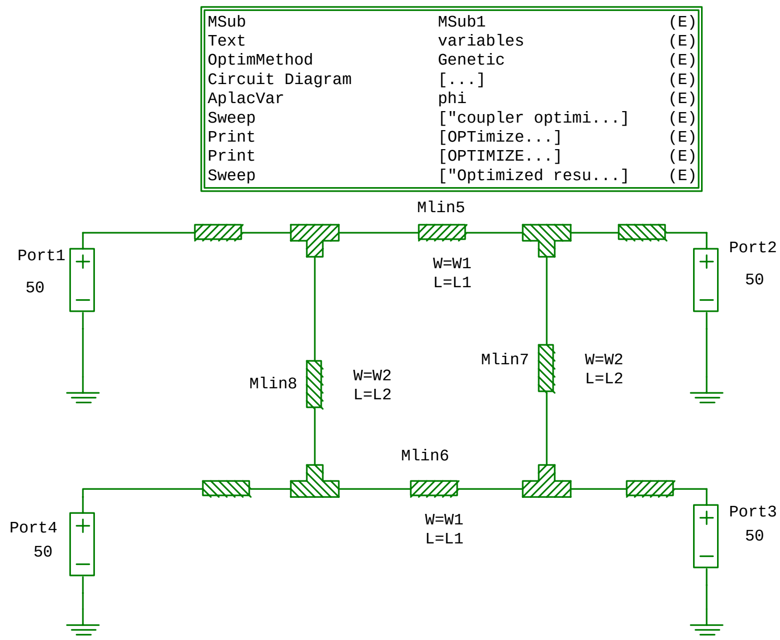

Fig. 7: The Schematic circuit description for the 7 dB MBC (APLAC 7.61)

### 3.4 Design of 4 GHz BMA

The design of a 4 GHz broadband microstrip amplifier, using the RF bipolar junction transistor (HXTR 41435) as an active element, is performed using our computer simulation program [10-11]. The developed design methodology is based on the use of scattering-matrix parameters of the active element. The computer simulation program [9, 10] is used for stability considerations and for the design of input and output matching circuits at a 4 GHz center frequency. An optimization program adjusts the designed circuit parameters (e.g., circuit-element values, transmission line lengths, etc.) to user-specified performance goal.

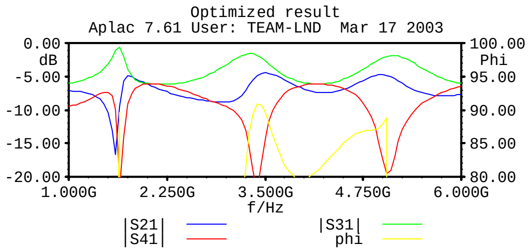


Fig 8: $|S_{11}|$, $|S_{21}|$ $|S_{12}|$ and $|S_{22}|$ in dB versus frequency for the designed branch hybrid (APLAC 7.61)

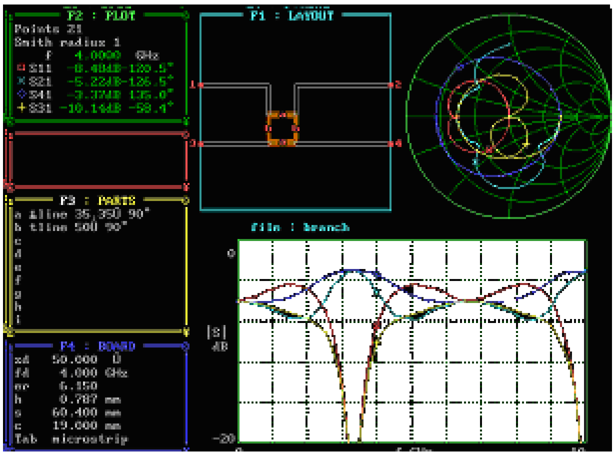


Fig. 9: The circuit disruption, circuit layout, and $|S_{11}|$, $|S_{21}|$ $|S_{11}|$ and $|S_{21}|$ for the 7dB MBC (PUFF2.1)

In order that the amplifier delivers a maximum power to the load, it must be properly terminated at both input and output ports [25-28]; hence the need of an input/output matching circuit arises. The Scattering parameters of the used transistor (HXTR 41435) at 4 GHz and $I_c$ = 10 mA are: $S_{11}$ = 0.46∠127°, $S_{12}$ = 0.153 ∠ 53°, $S_{21}$ = 1.91 ∠ 23°, and $S_{22}$ = 0.45 ∠ -60°. For stability consideration, our developed program is used to calculates the values of K and |Δ|. The calculated values of K= and |Δ| are 1.006 and 0.0857 respectively. They reflect the transistor unconditional stability.

The optimization process [15, 25, 26] adjusts the circuit parameters (microstrip stub line lengths and widths of the input and output matching circuits to achieve the broadband for the designed amplifier. Using the developed computer program [9-11], and the optimization process through C/NL2 package the lengths of the input and output matching circuits, at 4 GHz center frequency are: **Input matching circuit :** width of series line and shunt stub = 1 mm, length of series line = 17.966 mm, and length of open circuit single stub = 4.19 mm. **Output matching circuit :** width of series line and shunt stub =1 mm, length of series line = 8.55 mm, and length of open circuit single stub = 5.03 mm. Figure 10 shows |S21| versus the frequency for a high gain 4 GHz amplifier before the optimization process. Figures 11 and 12 show the circuit analysis, and the schematic circuit description for the designed broadband microstrip amplifier using APLAC 7.61 package [14]. Figure 13 shows the circuit layout of the designed 4 GHz BMA

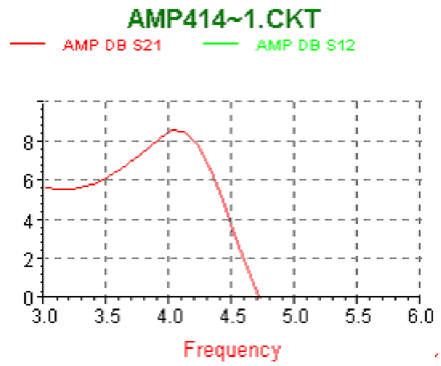


Fig.10: |S21| versus the frequency for the 4 GHz BMA (C/NL2)

### 3.5 Design of Microstrip Mixer.

The design of a microstrip mixer is performed using the full-scale developed program. The design is performed for a singly balanced mixer with the following three stages [29]: a) Design of hybrid coupler (rate-race coupler), b) Design of matching circuit that matches the diode input impedance to the coupler, c) Design of lowpass filter that passes the IF output signal.

#### 3.5.1 Design of 180°-hybrid rate-race coupler

The rate-race coupler is designed for the coupling factor C = 3 dB at the operating frequency = 4 GHz. As a result of the developed program, the parameters of the rate-race are [1, 2, 9-11]: total length of circular line = 54.9421395 mm, length of ( ¼ $\lambda_g$ ) circular lines = 9.157023 mm, length of (3/4 $\lambda_g$) circular lines = 27. 107 mm, width of circular lines = 0.46526 mm, impedance of circular lines = 70. 79478 mm, and width of output (50 Ω) lines = 0.935087 mm.

Figures 14 through 16 show $S_{31}$, $S_{41}$, and $S_{21}$, versus frequency for the rate race coupler operated at 4 GHz using C/NL2 package. Figure 17 shows the circuit disruption, circuit layout, and $|S_{11}|$ ,$|S_{21}|$ $|S_{41}|$ and $|S_{31}|$ for the designed rate-race hybrid using PUFF package

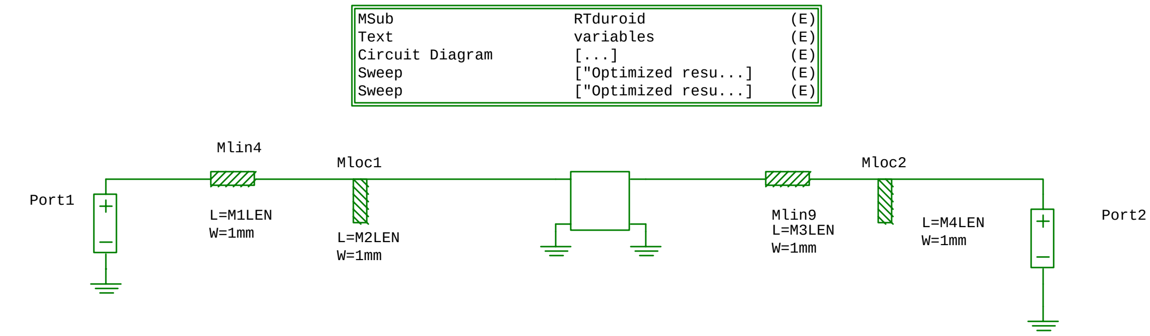


Fig. 11: Schematic circuit description for the 4 GHz BMA (APLAC 7.61)

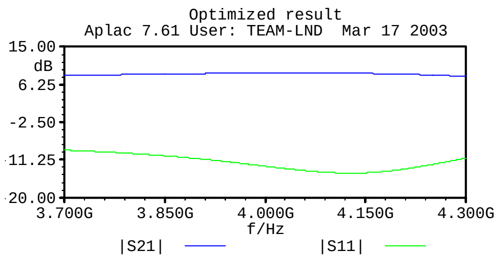


Fig. 12: $|S_{21}|$ and $|S_{11}|$ in dB versus frequency for the designed 4 GHz BMA (APLAC 7.61)

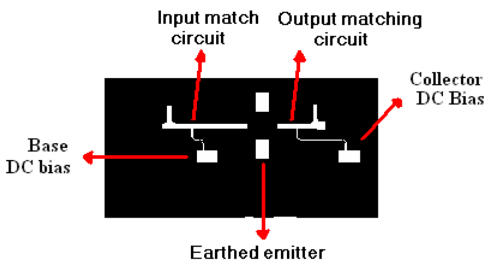


Fig 13: circuit layout of the designed 4 GHz BMA

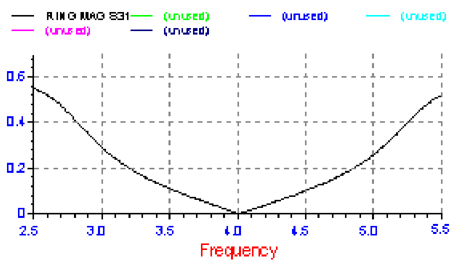


Figure 14 $S_{31}$ versus the frequency for the rate-race coupler operated at 4 GHz

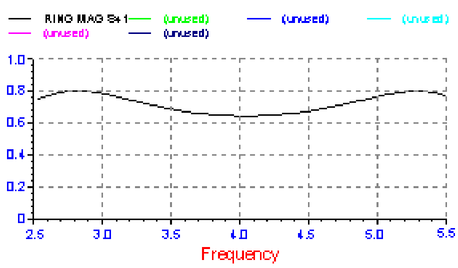


Fig. : 15 $S_{41}$ versus the frequency for the rate-race coupler operated at 4 GHz.

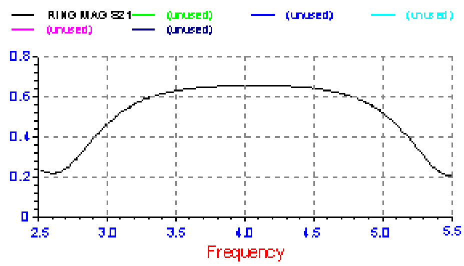


Fig. : 16 $S_{21}$ versus the frequency for the rate-race coupler operated at 4 GHz.

### 3.5.2 Design of matching circuit

The Schottky barrier diode (5082-2765) is used for the design of the mixer. The diode has the following parameters :$R_J$ = 258 Ω, $C_J$ =-. 255 pF, $L_P$ =0.435 nH, $C_P$ = 0.085 pF, $R_S$ = 14.5 Ω, and the ideality factor = 1.02[29-30]. The diode matching circuit is designed at 4 GHz. As a result of the developed program, the normalized input impedance and the input reflection coefficient are: $Z_{in}$ = 1.2752 – j 1.968 Ω, and $\Gamma_{in}$ = 0.66 ∠41.18°. For the calculated normalized impedance and the input reflection coefficient, the matching circuit is designed using the developed program. The lengths of and widths of the matching circuit are: length of series line = 15.1525, length of open circuit single stub = 6.4521, and width of series and shunt stub= 1 mm. Figure 18 shows the circuit layout of the designed 5-port-rate-race with diode matching circuits

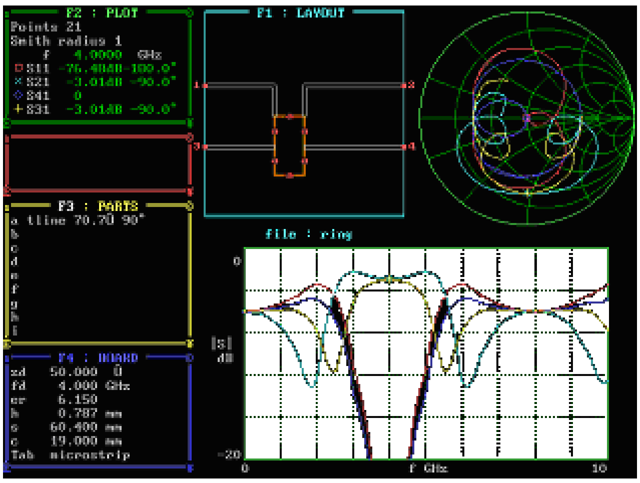


Fig. 17: The circuit disruption, circuit layout, and $|S_{11}|$ ,$|S_{21}|$ $|S_{41}|$ and $|S_{31}|$ for the designed rate-race hybrid (PUFF)

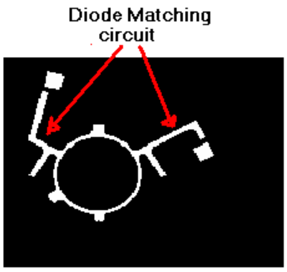


Fig. 18: The circuit layout of the designed 4 rate-race with diode matching circuits

### 3.5.3 Design of lowpass filter

The maximally flat lowpass prototype filter is used in the design of the lowpass filter with the following specifications :[1,2] : the operating frequency, $f_o$, = 4 GHz, the cut-off frequency, $f_c$, 0.75 GHz., the characteristic impedance of the series conductance is 100Ω̃, and the characteristic impedance of the shunt capacitance is 20Ω. One section maximally flat lowpass filter is considered. As a result of our developed program, length and width of the inductive microstrip line are 8.75 mm and 1 mm, respectively . Length and width of the capacitive microstrip line are 6.555 mm and 9 mm, respectively . The properties of a microstrip lowpass filter are analyzed by computing the electromagnetic field distribution in the device across a spectrum of frequencies (1– 20) GHZ. Figure 19 shows the schematic circuit description for the designed low-pass filter (APLAC 7.61). Figure 20 shows $|S_{11}|$ and $|S_{21}|$ in dB versus frequency for the designed low-pass filter (APLAC 7.61 package). Figure 21 shows the circuit disruption, circuit layout, and $|S_{11}|$ and $|S_{21}|$ for the designed low-pass filter (PUFF 2.1 Package). Figure 22 shows the distributed and lumped one-section maximally flat lowpass filter.

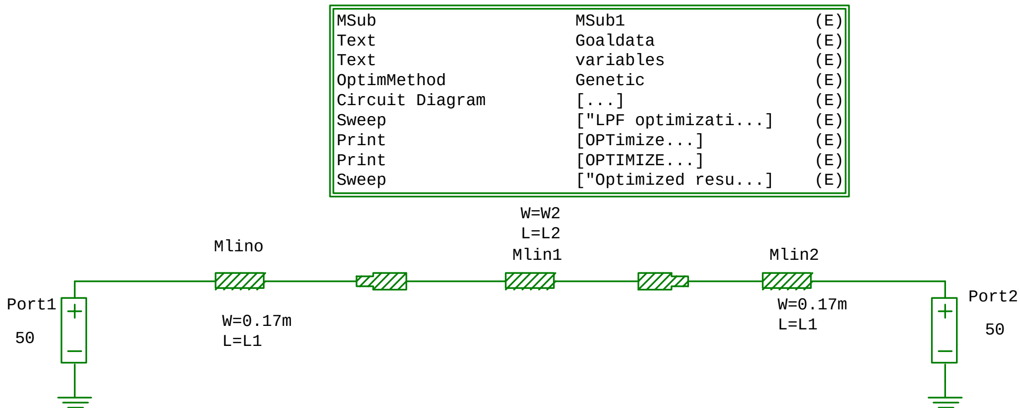


Fig. 19: The Schematic circuit description for the designed low-pass filter (APLAC 7.61)

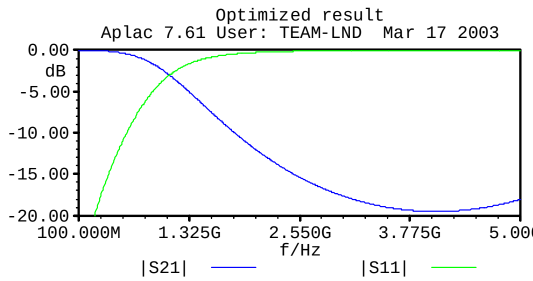


Fig 20: $|S_{11}|$ and $|S_{21}|$ in dB versus frequency for the designed low-pass filter (APLAC 7.61 package)

Figures 23 through 25 show the schematic circuit description, the IF output waveform and spectrum of the output signal of the designed SBDM using APLAC 7.61 package.

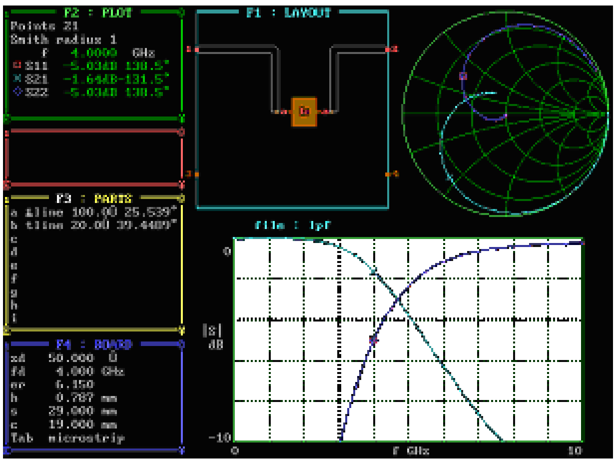

Fig. 21: The circuit disruption, circuit layout, and $|S_{11}|$ and $|S_{21}|$ for the designed low-pass filter (PUFF)

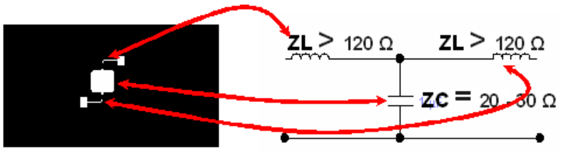


Fig. 22: The distributed and lumped one-section maximally flat lowpass filter.

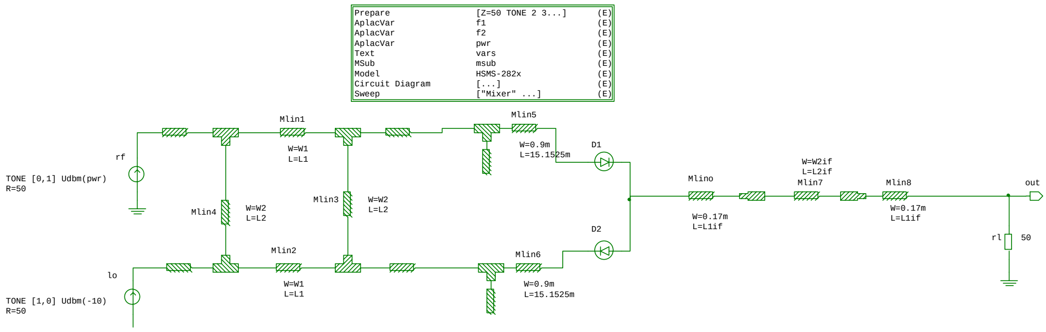


Fig. 23: The Schematic circuit description for the designed SBDM (APLAC 7.61)

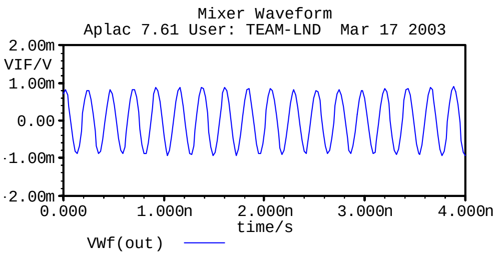


Fig. 24: The IF output waveform of the designed SBDM (APLAC 7.61)

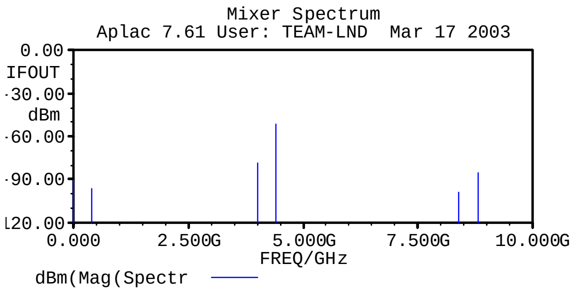


Fig. 25: The spectrum of the output signal for the designed SBDM (APLAC 7.61)

# 4 Conclusion

Distributed microwave integrated circuits have been increasingly adopted in many electronic systems such as communication, radar, electronic warfare, navigation, surveillance, and weapon guidance systems. These systems are mostly military in nature and have been supported strongly by the defense community. The objective of this work is to present a complete design analysis and implementation of 4 GHz SOP FMCW HMIC radar. A full-scale simulation computer program developed by the author is used for the designed modules. The designed modules are analyzed using the microwave packages such as APLAC 7.6, Puff 2.1, and C/NL2.1. A new approach for designing the broadband microstrip amplifiers is proposed. This approach depends on the optimization process of the initial design of narrow-band high-gain amplifier. The initial design is performed using our developed full-scale CAD programs while the optimization process is performed by C/NL2 and APLAC 7.61 packages. The complete layout of the designed 4 GHz transceiver module coupled with the MPA through ferrite circulator is introduced. The designed module can be used in many applications, including: wireless communications, radar systems (ground based, airborne, personal vehicles), target detection and identification, deep space Communications, and radio spectrometry. As a future work the designed module can be optimized using some of the current optimization techniques such as GA. Also as a future work, a complete circuit simulation using the most recently new approaches for coupling FDTD with circuit functionality, device physics (drift-diffusion and hydrodynamic particle transportation) and the thermodynamic effects can be performed

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