An Approach to Worst-Case Circuit Analysis

ELENA NICULESCU*, DORINA-MIOARA PURCARU* and MARIUS-CRISTIAN NICULESCU**
Electronics and Instrumentation Department* and Mechatronics and Robotics Department**
University of Craiova, Craiova, C.P. 200585, A. I. Cuza Street, No. 13, ROMANIA
eniculescu@electronics.ucv.ro; dpurcaru@electronics.ucv.ro

Abstract: - In this paper, the authors intend to show how to apply the circuit description in parameter space for a standard worst-case circuit analysis (WCCA). DC or AC or transient worst-case circuit analysis can be performed only by testing the circuit for the vertices of a polytope in conjunction with a circuit simulator or computational environment. In order to validate and show the effectiveness of this approach, DC and AC worst-case circuit analyses of an analog electronic circuit performed in conjunction with a general-purpose circuit simulator are presented and discussed.

Key-Words: - Worst-case circuit analysis, Analog electronic circuit, Polytope.

1 Introduction

The behaviour of an electronic circuit is affected when certain parameters in specific components change. Worst-case circuit analysis (WCCA) examines the effects on electronic circuits caused by potentially large magnitudes of variations of electronic piece-parts beyond their initial tolerance. WCCA provides a rigorous mathematical evaluation of the performance specification of a circuit against performance tolerance limits, under simultaneous existence of all the most unfavorable conditions being at realizable limits. This process is accomplished by analyzing the variability of a circuit with respect to part parameter tolerance extremes. The variations can be the result of both internal and external factors as aging or environmental influences, which can cause circuit outputs to drift out of specification [1], [2]. WCCA helps to design reliability into hardware for long-term, trouble-free field operation because the overstresses in worst-case conditions and improper applications are identified and eliminated prior to and during test, production and delivery [3], [4]. WCCA has been accepted by many design companies as a design verification tool. Also, the methods described for developing a worst-case parts variation database and sensitivity analysis, as well as extreme value analysis (EVA), root-sum-square (RSS), and Monte Carlo analysis for solving circuit equations and combining variables, have become accepted industry standards over the last two decades [5], [6]. Comparisons of the three WCCA techniques namely EVA, RSS, and Monte Carlo analysis are given in [1]-[4], [7]. The extreme value analysis is a nonstatistical method for handling the variables that affect circuit performance. Its application in WCCA needs to determine the mathematical sensitivity of the circuit performance to the variations in component parameters.

Automated fault detection for analog circuits is subject to specific problems, such as the unknown deviation in tolerances of non-faulty component values, the location of soft faults and the presence of noise. The techniques for soft fault diagnosis in analog electronic circuits are based on the simulation before test, approach where a fault dictionary is a priori generated by collecting signatures of different fault conditions [8]-[12]. Worst-case circuit analysis can be considered as a step in the soft-fault diagnosis allowing us to find out the bound outputs or performance attributes of a circuit.

A method to create a worst-case scenario and to detect the worst case min/max values of the outputs and performance attributes of the analog circuits is proposed in this paper. It is based on the fact that if a circuit output and/or performance specification is monotonic with respect to the changes in a circuit parameter value, then the extreme values of the response occur at the extreme values of that parameter. The monotonicity is identified by the sensitivity band computation over the parameter space [8], [9], [12]. Unlike EVA, the sensitivity analysis in our proposed approach is only used to identify the monotonicity of circuit outputs and performance attributes with respect to each variable and not for combining the variation contributions of the variables to obtain the extreme values of the performance.

The paper is organized as follows. The analog

circuit description in the parameter space by a polytope is given in Section 2. In Section 3, the problem formulation of the worst-case circuit analysis based on aforementioned circuit description is presented. Then, in Section 4, we show how to implement and validate the proposed procedure using a standard circuit simulator. Two case studies are presented and discussed using a small-signal amplifier with JFET as example, in order to illustrate the proposed procedure and to demonstrate its effectiveness. Section 5 concludes the paper.

2 Circuit Description

2.1 Circuits with symmetrical tolerances

The concept of the circuit design approach and tolerance selection, based on the floating and expanding polytope, has been proposed by Bandler for an optimal design of the nominal parameter values of the circuit and tolerances [13]. But this concept is appliable to the circuits with symmetrical tolerances.

Briefly, we resume this theorem looking for the circuit description as follows. Let us consider $\mathbf{\Phi} = [\Phi_1 \ \Phi_2 \ ... \ \Phi_k]^T$ a vector with k elements that correspond to the parameter circuit values. This vector has a correspondent point $\boldsymbol{P}(\Phi_1 \ \Phi_2 \ ... \ \Phi_k)$ in the *k*-dimensional space of parameters. The nominal point $\boldsymbol{P^0}=\left(\Phi_1^0 \ \ \Phi_2^0 \ .. \ \Phi_k^0\right)$ corresponds to $\Phi^0 = \left[\Phi_1^0 \ \ \Phi_2^0 \ .. \ \Phi_k^0\right]^T$ the vector of the parameter nominal values) and is associated with a non-negative tolerance set $\varepsilon = \left[\varepsilon_1 \ \ \varepsilon_2 \ .. \ \varepsilon_k\right]^T$. The tolerance region $\Re_t$, in the parameter space, is given as

$$\Re_t = \left\{P \middle| \Phi_i^0 - \varepsilon_i \le \Phi_i \le \Phi_i^0 + \varepsilon_i, i \in I_\Phi\right\} \qquad (1)$$

where $I_\Phi = \{1,2,...k\}$.

The tolerance region $\Re_t$ is a *k*-dimensional convex regular polytope, centered at P^0, in the *k*-dimensional space of parameters, and $2\varepsilon_i$, $i \in I_\Phi$, is the length of the *i* side of this polytope. The polytope has 2^k vertices, which are the extreme points of $\Re_t$. Then, the set of vertices can be defined as

$$\Re_v = \left\{P \middle| \Phi_i = \Phi_i^0 + \varepsilon_i \mu_i, \mu_i = \pm 1, i \in I_\Phi\right\}. \qquad (2)$$

The number of points contained by $\Re_v$ is 2^k: $\Re_v = \left\{P^1 \ \ P^2 \ .. \ P^{2^k}\right\}$. These points are indexed by P^i, $i \in I_v$, $I_v = \left\{1,2,...,2^k\right\}$. Looking for an optimal design of circuit, an accepted region $\Re_a$ is defined and it is demonstrated that if $\Re_v \subseteq \Re_a$, then $\Re_t \subseteq \Re_a$. According to this theorem, only the polytope vertices must be tested to be sure that $\Re_t \subseteq \Re_a$.

2.2 Circuits with asymmetrical tolerances

The operating characteristics of active devices and analog integrated circuits are often unpredictable because of their internal geometric dependence. We can create component models that more closely represent actual real world devices by converting measurement or catalog data into model parameters by means of various tools type parameter extractor. Usually, the model parameter range of a device lot is not centered at nominal values of the model parameters of a given device sample. The spread of the parameter values due to the manufacturing process as well as the drifts due to aging, and high and low temperature, are generating sources of asymmetrical tolerances of the parameters. Also, the deviations of the supply voltages can be asymmetrical with rapport to their nominal values.

This problem of the analog circuits with asymmetrical tolerances becomes easy to solve if the asymmetrical tolerance case can be reduced to that of the symmetrical tolerance case. In order to solve this kind problem, a polytope with averaged-nominal point was defined and its equivalence with the polytope with symmetrical tolerance was demonstrated.

We supposed that the nominal point is $\{\Phi_{0i}\}$ with $i \in I_\Phi$, the positive tolerances ε_{pi} and ε_{ni} are lop-sided, i.e. there is $i_0 \in I_\Phi$ for which $\varepsilon_{pi_0} \neq \varepsilon_{pi_0}$. Some tolerances can be symmetrical. Now, the tolerance region is

$$\Re_t = \left\{P \middle| \Phi_{0i} - \varepsilon_{ni} \le \Phi_i \le \Phi_{0i} + \varepsilon_{pi}, i \in I_\Phi\right\}. \qquad (3)$$

The tolerance region $\Re_t$ is a *k*-dimensional polytope with side *i* of $(\varepsilon_{pi} + \varepsilon_{ni})$ length, $i \in I_\Phi$, and with 2^k vertices. We replaced the nominal point Φ_i^0 of the polytope $\Re_t$ with the averaged-nominal point Φ_{mi}^0, where

$$\Phi_{mi}^0 = \Phi_{0i} + \frac{\varepsilon_{pi} - \varepsilon_{ni}}{2}, \qquad (4)$$

and we denote the mean values of tolerances, i.e. the symmetrical tolerances,

$$\varepsilon_{mi} = \frac{\varepsilon_{pi} + \varepsilon_{ni}}{2} \text{ for all } i \in I_\Phi. \qquad (5)$$

Then, we demonstrated

$$\Re_{mt} = \left\{ \begin{matrix} P \left| \Phi^0_{mi} - \varepsilon_{mi} \le \Phi_i \le \Phi^0_{mi} + \varepsilon_{mi}, \right. \\ for \quad all \quad i \in I_\Phi \end{matrix} \right\} = \Re_t . \quad (6)$$

Replacing the polytope with asymmetrical tolerances with its equivalent polytope with symmetrical tolerances allows us to apply the Bandler's theorem to an analog circuit with asymmetrical tolerances.

3 Worst-Case Circuit Analysis

An analog circuit can be described in the parameter space by a polytope, i.e. $\Re_t$ or $\Re_{mt}$, of which vertices represent the extreme values of parameters. A DC or AC or transient analysis performed for the vertices of the polytope $\Re_t$ will produce corresponding value bands of the circuit outputs or performance attributes. The bounds of these value bands represent the worst case values of the circuit outputs or performance attributes.

Consider a circuit of k parameters, $\boldsymbol{P} = [p_1, p_2, ...,p_k]$, where p_i may be the resistance of a resistor, the capacitance of a capacitor, the β transconductance parameter or W/L ratio of a FET, the V_{th} threshold voltage, the λ channel length modulation coefficient etc. The circuit parameters have the nominal values $\boldsymbol{P_0} = [p_{01}, p_{02}, ...,p_{0k}]$ and the tolerances $\varepsilon = [\varepsilon_{p1}, \varepsilon_{n1}, \varepsilon_{p2}, \varepsilon_{n2},\ldots \varepsilon_{pk}, \varepsilon_{nk}]$. Some tolerances can be symmetrical, i.e. $\varepsilon_{pj} = \varepsilon_{nj} = \varepsilon_j$.

Let be the polytope $\Re_{mt}$ with the averaged nominal point

$$P^0_{mi} = p_{0i} + \frac{\varepsilon_{pi} - \varepsilon_{ni}}{2} \quad (7)$$

and the tolerances

$$\varepsilon_{mi} = \frac{\varepsilon_{pi} + \varepsilon_{ni}}{2}, \text{ with } i = 1,\ldots, k. \quad (8)$$

The vertices of the set $\Re_{mt} = \{P^l_m\}$, where $l = 1,., 2^k$, are denoted as follows:

$$P^1_m = \begin{bmatrix} p^0_{m1} - \varepsilon_{m1} \\ p^0_{m2} - \varepsilon_{m2} \\ .... \\ p^0_{mk} - \varepsilon_{mk} \end{bmatrix}, \; P^2_m = \begin{bmatrix} p^0_{m1} + \varepsilon_{m1} \\ p^0_{m2} - \varepsilon_{m2} \\ .... \\ p^0_{mk} - \varepsilon_{mk} \end{bmatrix},$$

$$P^3_m = \begin{bmatrix} p^0_{m1} - \varepsilon_{m1} \\ p^0_{m2} + \varepsilon_{m2} \\ .... \\ p^0_{mk} - \varepsilon_{mk} \end{bmatrix}, ..., P^{2^k}_m = \begin{bmatrix} p^0_{m1} + \varepsilon_{m1} \\ p^0_{m2} + \varepsilon_{m2} \\ .... \\ p^0_{mk} + \varepsilon_{mk} \end{bmatrix}. \quad (9)$$

We suppose that the behaviour of the circuit is characterized by m circuit outputs $\boldsymbol{y} = [y_1, y_2, \ldots, y_m]$ and n performance attributes $\boldsymbol{S} = [s_1, s_2, ..., s_n]$. The circuit DC outputs $\boldsymbol{Y} = [Y_1, Y_2, \ldots, Y_m]$ are DC voltages of nodes or DC currents through circuit branches that describe the DC operating point of circuit. A transient analysis yields the circuit outputs $\boldsymbol{y}(t) = [y_1(t), y_2(t), \ldots, y_m(t)]$. A circuit output, for example the r-th output, or a performance attribute, for example the t-th attribute, can be represented as a function of all parameters, i.e.

$$y_r = f(p_1, p_2, ...,p_k) \text{ and } s_t = f(p_1, p_2, ...,p_k). \quad (10)$$

Regardless of symmetrical or asymmetrical tolerance case, the circuit outputs and performance attributes at nominal values of parameters will be:

$$\boldsymbol{y_0} = [y_1(\boldsymbol{P_0}), y_2(\boldsymbol{P_0}), \ldots, y_m(\boldsymbol{P_0})], \quad (11)$$

$$\boldsymbol{S_0} = [s_1(\boldsymbol{P_0}), s_2(\boldsymbol{P_0}), ..., s_n(\boldsymbol{P_0})]. \quad (12)$$

Each output and performance attribute of a circuit is expressed by a value or a curve at nominal point in parameter space.

Considering the variations in the parameter space and testing the circuit for the polytope vertices, there will correspondingly be variation in the circuit outputs and attributes:

$$\boldsymbol{y}(\boldsymbol{P^l_m}) = [y_1(\boldsymbol{P^l_m}), y_2(\boldsymbol{P^l_m}), \ldots, y_m(\boldsymbol{P^l_m})], \quad (13)$$

$$\boldsymbol{S}(\boldsymbol{P^l_m}) = [s_1(\boldsymbol{P^l_m}), s_2(\boldsymbol{P^l_m}), ..., s_n(\boldsymbol{P^l_m})]. \quad (14)$$

The relationships between a circuit output or performance specification and the parameters will become a band instead of a single curve. So, the circuit output y_r is bounded by y_{rmin} and y_{rmax}, the performance specification s_t is bounded by s_{tmin} and s_{tmax}:

$$y_{rmin} \le y_r \le y_{rmax} \text{ and } s_{tmin} \le s_t \le s_{tmax}. \quad (15)$$

If the circuit outputs and/or performance attributes are monotonic with respect to the changes in value of each circuit parameter, then the extreme values of the response occur at the extreme values of that parameter. The bounds y_{rmin} and y_{rmax}, s_{tmin} and s_{tmax} are the worst values of circuit outputs and performance attributes for a worst-case circuit analysis. For a fault detection problem, the same bounds delimit the operation of the fault-free circuit. The upper bound of a circuit output can be looked as stress analysis result.

The proposed procedure to WCCA can be implemented in conjunction with a circuit simulator or computational environment (MatLab, MathCAD, Mathematica etc.) when an appropriate model of the device/circuit is available. First of all, the monotonicity of circuit outputs and/or performance attributes with respect to circuit parameters must be identified by the sensitivity computation over the parameter space. As it will be shown in the following, this procedure can be applied to perform

the worst case analysis of the analog circuits with symmetrical and/or asymmetrical tolerances.

4 Case Studies

Using a general-purpose circuit simulator, we will show how to implement and validate the proposed procedure. The circuit simulator is used to perform the DC Operating Point Analysis and AC Analysis of the amplifier circuit for the polytope vertices. In order to verify the proposed procedure for the worst-case analysis of an analog circuit, its results will be compared with those produced by the Worst Case Analysis allowed by the circuit simulator and an experimental setup. For this purpose, we consider a small-signal amplifier with a NJFET type BFW11. The circuit diagram of the test circuit is shown in Fig. 1.

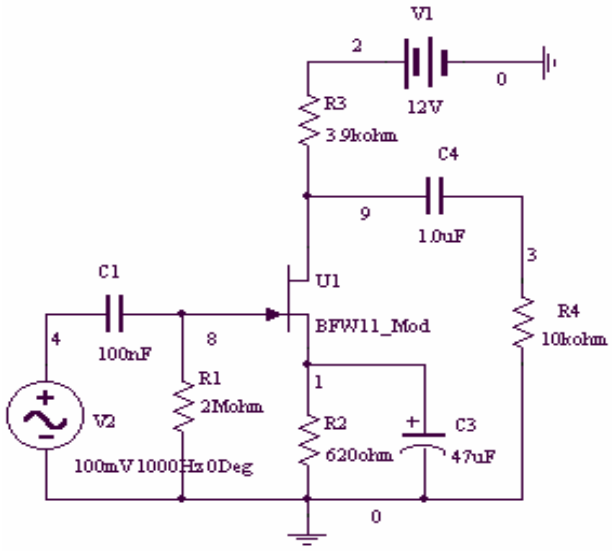

Fig. 1. Circuit diagram of the small-signal amplifier with JFET type BFW11_Mod

Firstly, we consider the circuit with symmetrical tolerances of two resistors in circuit that means their initial tolerances and perform the DC and AC worst case analysis based on the dedicated menu of simulator and our procedure. Secondly, the bounds of the parameter dispersion of the transistor at constant temperature are taken into account as asymmetrical tolerances of circuit with rapport to a JFET sample.

Our NJFET sample type BFW11 was chosen from a lot of ten transistors for which the characteristic curves were measured. We extracted the threshold voltage, nominal saturation current and output conductance of each transistor from its characteristic curves. Then, converting the measurement data, we created a device model.

Such a model has been created for three devices namely: NJFET sample and two NJFETs of which characteristic curves represent the lot dispersion. For the NJFET sample model, we find out the following parameters: V_{T0} (V) = - 2 (threshold voltage), β (mA/V^2) = 1.24685 (transconductance parameter) and λ (V^{-1}) = 0.0246 (channel length modulation coefficient). The rest of model parameters holds the value set for the NJFET type BFW11 contained by the Master Database of the circuit simulator. The new device with its model was saved in User Database as a component named BFW11_Mod. The bias circuit was designed to set the DC operating point into the active forward region with the following nominal coordinates: $I_{DQ} \cong 1.5$ mA, $V_{GSQ} \cong -1$ V and $V_{DSQ} \cong 6$ V. Consequently, we obtain the following values of resistances: R_1 = 2 MΩ, R_2 = 620 Ω and R_3 = 3.9 kΩ. All the passive components have an initial tolerance of ±5%. We consider a constant temperature (27^{o}C), for the sake of brevity and a better match of the measurement and simulation conditions.

4.1 Worst case analysis of an analog circuit with symmetrical tolerances

At this point, the effects of the model parameter tolerances of the JFET are not considered. Looking for DC and AC worst case analysis of the given circuit, only the effects of variations of two resistive parameters namely R_2 and R_3 on the circuit operating are taken into account. So, the circuit parameters are as follows: $p_1 = R_2$, p_{10} = 620 Ω, ε_1 = 31 Ω; $p_2 = R_3$, p_{20} = 3.9 kΩ , ε_2 = 195 Ω.

Firstly, we examine the effects of these symmetrical tolerances on three DC outputs of circuit namely: the voltages of drain and source nodes ($Y1$ = V9 and $Y2$ = V1), and the supply branch current ($Y3$ = vv1#branch = I_D). Then, we verify if the proposed procedure can yield the worst case values of the mid-band voltage gain of the amplifier that was chosen herein as performance attribute.

In order to apply and validate the proposed procedure, the following steps must be done:

1. The circuit from the Fig. 1 is simulated for the DC and AC Sensitivity Analysis in order to verify that the DC outputs and mid-band voltage gain are monotonic with respect to the changes in parameter values of the two circuit components.
2. The circuit from the Fig. 1 is simulated for the DC and AC worst case analysis using the aforementioned tolerances, i.e. ε_1 and ε_2. The DC worst case analysis results are shown in Table 1. The AC worst case analysis yields the following

results: nominal value of the voltage gain of the amplifier at f = 39.8 kHz is equal to 7.5 while its worst-case value is equal to 7.44. The AC worst case analysis result corresponds to R_2 increased to 651 Ω and R_3 =3.9 kΩ (unchanged).

3. In order to find out the bounds of the specified circuit outputs, the R_2 and R_3 parameter values are modified according to each vertex of polytope. Then, the new circuit is simulated for perfoming the DC Operating Point Analysis and AC Analysis. The polytope with symmetrical tolerances are four vertices:

$$\boldsymbol{P}^1 = \begin{bmatrix} 589 \\ 3705 \end{bmatrix}; \boldsymbol{P}^2 = \begin{bmatrix} 651 \\ 3705 \end{bmatrix}; \boldsymbol{P}^3 = \begin{bmatrix} 589 \\ 4095 \end{bmatrix};$$

$$\boldsymbol{P}^4 = \begin{bmatrix} 651 \\ 4095 \end{bmatrix}.$$

The analysis results concerning the DC circuit outputs are given in Table 1 while those of the performance attribute as magnitude – frequency plots of the voltage gain are shown in Fig. 2.

Table 1. The results of the DC worst case analysis performed with the dedicated menu of a circuit simulator, proposed technique and experimental setup.

Approach		DC circuit outputs		
		Y_1(V)	Y_2(V)	Y_3(mA)
DC WCA menu		6.4647 (R2=651Ω; R3=3705Ω)	0.97259 (R2=651Ω; R3=3705Ω)	1.48777 (R2=651Ω; R3=4095Ω)
Polytope vertices	$\boldsymbol{P}^1$	6.21161	0.9202	**1.56232**
	$\boldsymbol{P}^2$	**6.55433**	**0.95685**	1.46982
	$\boldsymbol{P}^3$	**5.63123**	**0.91604**	1.5552
	$\boldsymbol{P}^4$	6.00551	0.95297	**1.46386**
Experi-mental	$\boldsymbol{P}^1$	6.24147	0.91545	**1.55426**
	$\boldsymbol{P}^2$	**6.58225**	**0.95194**	1.46228
	$\boldsymbol{P}^3$	**5.6643**	**0.91128**	1.54718
	$\boldsymbol{P}^4$	6.03643	0.94805	**1.4563**

4. The three DC outputs of the circuit constructed with the NJFET sample for the four pairs of values of resistances R_2 and R_3 are measured. The DC experimental results are given in Table 1. Also, the magnitude of voltage gain at f = 39.8 kHz was measured for the nominal point and each vertex of the polytope. These AC experimental results and their simulated correspondents are shown in Fig. 3 in order to facilitate their comparison.

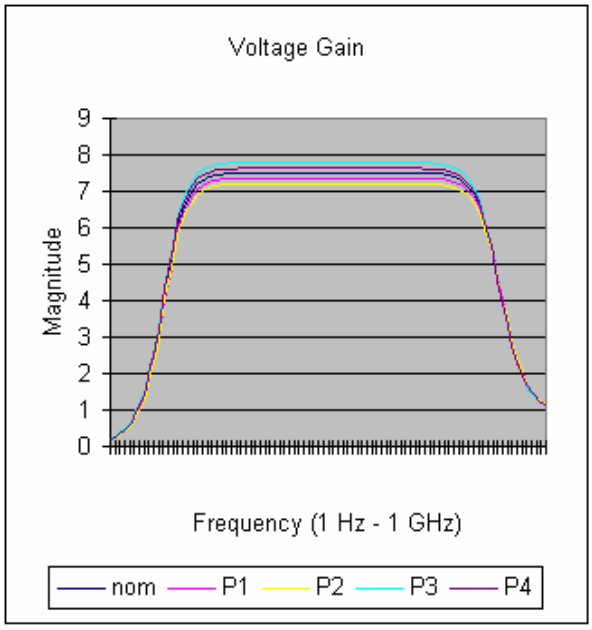

Fig. 2. Magnitude-frequency plots of voltage gain obtained by the proposed procedure.

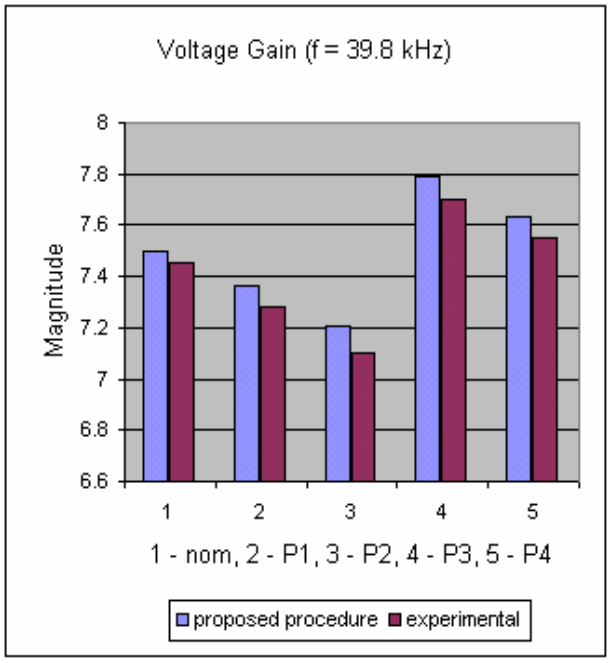

Fig. 3. Magnitudes of voltage gain at f = 39.8 kHz as they are obtained by measurement and proposed procedure.

5. Comparison between the results of the worst case analysis performed with the dedicated menu of a circuit simulator, proposed technique based on the testing of the polytope vertices, and experimental setup show the following:

a. The worst case analysis performed by means of the dedicated menu of simulator provides an only value for each DC output of circuit: $Y_{1w.c.a}$ (V) =

6.4647, $Y_{2w.c.a.}$ (V) = 0.97259, $Y_{3w.c.a.}$ (mA) = 1.48777. The supplementary index marks the worst case value (w.c.a.) of DC outputs.

b. The proposed technique provides a value band for each DC output of circuit. The minimum and maximum values of each band (bolded in Table 1) represent the results of the worst case analysis based on testing the circuit for the polytope vertices. The band limits of DC outputs correspond to following pairs of vertices of polytope: $\boldsymbol{P^2}$ and $\boldsymbol{P^3}$ for outputs Y_1 and Y_2, and $\boldsymbol{P^1}$ and $\boldsymbol{P^4}$ for output Y_3. As it was expected, the band limits of the magnitude of voltage gain are obtained for the vertices $\boldsymbol{P^2}$ and $\boldsymbol{P^3}$.

c. The worst case values of the DC circuit outputs supplied by dedicated menu of the simulator (DC WCA) are nearly recovered for the $\boldsymbol{P^2}$ and $\boldsymbol{P^4}$ vertices of polytope.

d. The two value bands of the DC outputs and voltage gain magnitude, and their bounds from the experimental results are nearly the same as those obtained utilizing the proposed procedure.

4.2 Worst case analysis of an analog circuit with asymmetrical tolerances

In this section, we will illustrate how to apply the proposed procedure on a circuit with some asymmetrical tolerances by means of a circuit simulator. The asymmetrical tolerances describe the NJFET lot dispersion with rapport to NJFET sample. In our circuit simulator version, the sensitivity analysis and consequently the worst case analysis with rapport with the model parameters of active devices is not possible. For this purpose, we construct the component model for the two transistors of which characteristic curves represent the lot dispersion.

Table 2. Main parameters of the BFW11_Mod_a and BFW11_Mod_b models

	BFW11_Mod_a	BFW11_Mod_b
V_{T0} (V)	-1.0686	-2.3085
β (mA/V^2)	1.73071	1.09045
λ (V^{-1})	0.02591	0.02317

Let be BFW11_Mod_a the device for which we extracted from measured curves the following parameters: V_{T0} (V) = -1.0686, I_{DSS} (mA) = 1.976 and λ(V^{-1}) = 0.02591. The other transistor named BFW11_Mod_b is characterized by the parameter values: V_{T0} (V) = -2.3085, I_{DSS} (mA) = 5.8112 and λ(V^{-1}) = 0.02317. The user models characterizing the lot dispersion are constructed and saved with the same names as the devices. The main parameters of the two models are summarized in Table 2. As for previous case, the rest of the model parameters have the same values as they of BFW11 model in Master Database of simulator.

Now, we consider the effects of five circuit parameters on the same DC outputs and performance attribute as in previous case. Among these, we have two component parameters with symmetrical tolerances, i.e. R_2 and R_3, and three device parameters with asymmetrical tolerances, i.e. V_{T0}, β and λ.

The nominal value and tolerance of these five parameters are as follows:

$p_1 = R_2$, p_{10} (Ω) = 620, ε_1 (Ω) = 31; $p_2 = R_3$, p_{20} (kΩ) = 3.9, ε_2 (Ω) = 195; $p_3 = V_{T0}$, p_{30} (V) = -2, ε_{p3} (V) = 0.9314, ε_{n3} (V) = 0.3085; p_4 = β, p_{40} (mA/V^2) = 1.24685, ε_{p4} (mA/V^2) = 0.48386, ε_{n4} (mA/V^2) = 0.1564; p_5 = λ, p_{50} (V^{-1}) = 0.0246045, ε_{p5} (V^{-1}) = 0.001311, ε_{n5} (V^{-1}) = 0.001429.

The nominal values p_{30}, p_{40} and p_{50} correspond to the model parameter values of BFW11_mod device. Their asymmetrical tolerances associated to these nominal values, i.e. ε_{p3}, ε_{n3}, ε_{p4}, ε_{n4}, ε_{p5}, ε_{n5}, represent the differences between the values of the homonym parameters of BFW11_Mod model and BFW11_Mod_a model, respectively BFW11_Mod_b model.

According to the proposed procedure, the polytope with averaged nominal point has 2^5 vertices corresponding to the five considered parameters of circuit. The hypothesis of the constant temperature introduces some constraints concerning the combination of tolerances assigned to the model parameters of JFET. This means that the mean values of tolerances associated to the two model parameters will be simultaneously added or subtracted from the averaged nominal values for all three parameters. Consequently, only 2^3 vertices of polytope rest to be tested.

Next, we have to calculate the averaged nominal values and mean tolerances of the parameters according to (7) and (8). These algebraic calculations yield the following data:

p^0_{m1} = p_{10} (Ω) = 620, ε_{m1} = ε_1 (Ω) = 31; p^0_{m2} = p_{20} (kΩ) = 3.9, ε_{m2} = ε_2 (Ω) = 195; p^0_{m3} (V) = -1.68855, ε_{m3} (V) = 0.61995; p^0_{m4} (mA/V^2) = 1.41058, ε_{m4} (mA/V^2) = 0.32013; p^0_{m5} (V^{-1}) = 0.024545, ε_{m5} (V^{-1}) = 0.00137.

Now, applying (9) we can write the vertices of the polytope with averaged nominal point as follows:

$$P_m^1 = \begin{bmatrix} 589 \\ 3705 \\ -1.0686 \\ 1.73071 \\ 0.02591 \end{bmatrix}; P_m^2 = \begin{bmatrix} 651 \\ 3705 \\ -1.0686 \\ 1.73071 \\ 0.02591 \end{bmatrix}; P_m^3 = \begin{bmatrix} 589 \\ 4095 \\ -1.0686 \\ 1.73071 \\ 0.02591 \end{bmatrix}$$

$$P_m^4 = \begin{bmatrix} 651 \\ 4095 \\ -1.0686 \\ 1.73071 \\ 0.02591 \end{bmatrix}; P_m^5 = \begin{bmatrix} 589 \\ 3705 \\ -2.3085 \\ 1.09045 \\ 0.02317 \end{bmatrix}; P_m^6 = \begin{bmatrix} 651 \\ 3705 \\ -2.3085 \\ 1.09045 \\ 0.02317 \end{bmatrix}$$

$$P_m^7 = \begin{bmatrix} 589 \\ 4095 \\ -2.3085 \\ 1.09045 \\ 0.02317 \end{bmatrix}; P_m^8 = \begin{bmatrix} 651 \\ 4095 \\ -2.3085 \\ 1.09045 \\ 0.02317 \end{bmatrix}.$$

Firstly, using the circuit simulator the monotonicity of DC outputs and voltage gain of the amplifier with respect to the changes in the three parameter values of the JFET model was checked. This checking made separately for each model parameter needs other six user models of active device derived from BFW11_Mod model. For instance, to check up the monotonicity of DC outputs and performance attribute with respect to threshold voltage, one model has V_{T0} (V) = - 1.0686, β (mA/V^2) = 1.24685 and λ (V^{-1}) = 0.0246, and other model has V_{T0} (V) = - 2.3085, β (mA/V^2) = 1.24685 and λ (V^{-1}) = 0.0246. The rest of parameters have their nominal values. Simulating the two new circuits one obtains the necessary data to calculate the DC outputs and voltage gain sensitivities over the parameter range. The results of these analyses and sensitivity calculations show that the DC outputs and voltage gain of the circuit are monotonic with respect to model parameters of JFET.

Next, to find out the DC worst case outputs of the circuit, we have to run eight times the DC Operating Point Analysis and AC Analysis from the circuit simulator for the eight specified vertices. Each polytope vertex means a particular circuit concerning the active device, i.e. either BFW11_Mod_a or BFW11_Mod_b, and extreme values of the two resistances. The simulation results concerning the DC circuit outputs are shown in Table 3 while those of the voltage gain are shown in Fig. 4.

The minimum and maximum values of each band (bolded in Table 3) represent the results of the worst case analysis based on the polytope vertex test. The parameter value dispersion of active device highlighted by the differences of the band bounds of each DC outputs of the circuits in Table 1 and 3 has a critical impact on meeting the design specifications.

Table 3. The results of the DC worst case analysis based on the polytope vertex test.

Polytope vertices	DC circuit outputs		
	Y_1(V)	Y_2(V)	Y_3(mA)
P^1	9.14932	0.45318	0.76941
P^2	**9.31214**	0.47228	0.72546
P^3	8.8569	**0.45208**	0.76754
P^4	9.03572	0.47124	**0.72387**
P^5	5.36171	1.05532	**1.79171**
P^6	5.75153	**1.09791**	1.6865
P^7	**4.69983**	1.05001	1.7827
P^8	5.12496	1.09296	1.67889

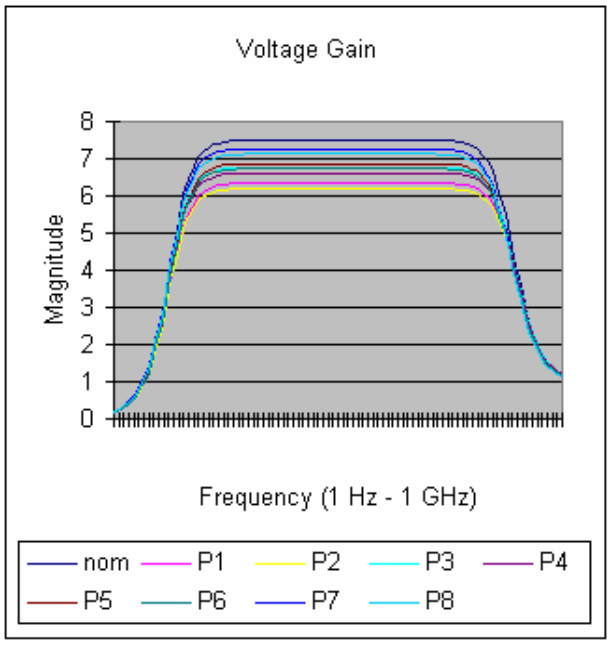

Fig. 4. Magnitude-frequency plots of voltage gain obtained by the proposed procedure.

The results of the worst case analysis performed with the proposed technique and experimental setup concerning the voltage gain at f = 39.8 kHz are also given in Fig. 5.

The results obtained by the proposed procedure are nearly the same as the experimental results. This means that the proposed procedure can be an alternative means to perform the worst case analysis of an analog circuit.

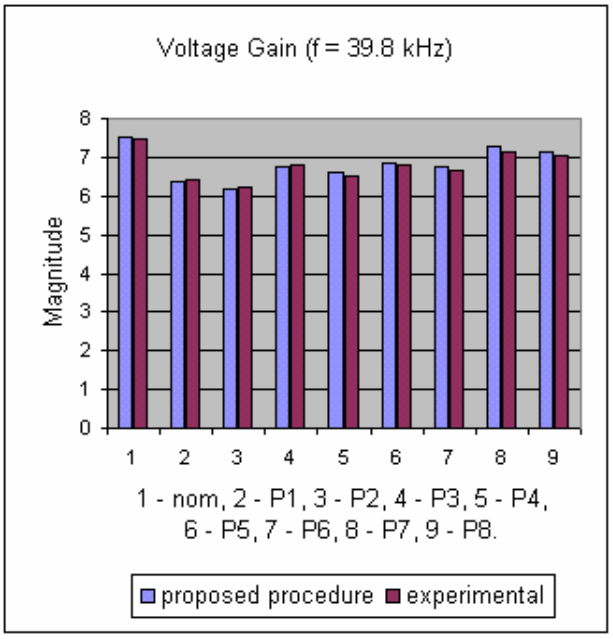

Fig. 5. Magnitudes of voltage gain at f = 39.8 kHz as they are obtained by measurement and proposed procedure.

5 Conclusion

In this paper, a procedure to perform the worst case analysis of an analog circuit with symmetrical and/or asymmetrical tolerance is presented. The worst case values of the circuit outputs or performance attributes are obtained by performing DC or AC or transient analysis for the extreme values of parameters given by the vertices of a polytope. The number of vertices increases with the number of circuit parameters taken into account. When the worst case analysis is performed in conjunction with a circuit simulator for a large number of parameters such a procedure becomes heavy. Each polytope vertex requires the modification and resimulation of the circuit. This drawback disappears when the procedure is applied in conjunction with a computational environment.

Likewise EVA, our proposed approach to worst-case circuit analysis is the easiest technique to use and yields the most readily obtainable estimates worst-case circuit performance. The proposed procedure is different to extreme value analysis (EVA), because it is not based on the sensitivity analysis to compute the extreme values of circuit outputs and/or performance attributes. Also, our proposed approach yields an in-depth understanding of a design due to the format of the required inputs that consists of the worst-case part variation limits for all components.

References:

[1] W. M. Smith, *Worst Case Circuit Analysis Handbooks* (Volumes 1–5), Design and Evaluation Inc., 1989.

[2] W. M. Smith, Worst-case circuit analysis - an overview (electronic parts/circuits tolerance analysis), *Proceedings of International Symposium on Product Quality and Integrity*, pp. 326 – 334, 1996.

[3] B. Vinnakota, *Analog and Mixed-Signal Test*, Prentice Hall, 1998.

[4] R. R. Boyd, *Tolerance Analysis of Electronic Circuit Using Mathcad*, CRC Press LLC, 2000.

[5] http:// www.designandevaluation.com

[6] W. K. Al-Assadi and P. Chandrasekhar, Issues in Testing Analog Devices, *Proc. of the 12th NASA Symposium on VLSI Design,* 2005.

[7] A. Brockschmidt, R. Carpenter, and F. Shi, Guidelines and examples for performing worst case analysis, *Proceedings of the IEEE Applied Power Electronics Conference and Exposition*, APEC'99, Vol. 2, pp. 930-936, 1999.

[8] M. W. Tian and C.-J.R. Shi, Worst-case analysis of linear analog circuits using sensitivity bands, *IEEE Transactions on Circuits and Systems: Fundamental Theory and Applications,* vol. 47, no. 8, 2000, pp. 1138-1145.

[9] M. Worsman and M.W.T. Wong, Non-linear analog circuit fault diagnosis with large change sensitivity, *International Journal of Circuit Theory and Applications,*No. 28, 2000, pp. 281-303.

[10] C. Marcantonio and A. Fort,Soft Fault Detection and Isolation in Analog Circuits: Some Results and a Comparison Between a Fuzzy Approach and Radial Basis Function Networks, *IEEE Transactions on Instrumentation and Measurement*, Vol. 51, No. 2, 2002, pp. 196-202

[11] S.-J. Chang, C.-L. Lee, and J. E. Chen, Structure-based specification-Constrained Test frequency generation for Linear Analog Circuits, *Journal of Information Science and Engineering*, Vol. 19, 2003, pp. 637-651.

[12] V. C. Prasad and N. C. S. Babu, Selection of test nodes for analog fault diagnosis in dictionary approach. *IEEE Transactions on Instrumentation and Measurement*, Vol. 49, 2000, pp. 1289-1297.

[13] J. W. Bandler, Worst Case Network Tolerance Optimization, *IEEE Transactions on Microwave Theory,* Vol. MTT-23, Aug. 1975, pp. 630-641.