A CMOS Gm-C State-Space 1MHz Low-Pass Active Filter

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Abstract: - In this paper are presented a CMOS Gm-C state-space active filter for high frequencies, in the 1μm CMOS process, synthesised using the intermediate transfer function method. The Gm transconductor has a good linearity (1% relative error for $2V_{p-p}$ input signals with a 5V power supply) and high DC gain (≥40dB), combined with a large band to avoid errors in the filter characteristic. By using the intermediate transfer functions method, the active filter performances - as sensitivity and dynamic range (noise) - are optimised. The 1 MHz low-pass filter has the dynamic range grater than 70db and the total harmonic distortion lower than –60 dB.

Key-Words: - synthesis, active filters, intermediate transfer function synthesis method

1 Introduction

Monolithic filters can be implemented using several circuit techniques: AO-RC [1], [2], MOSFET-C [3], switched-C [4], [5], Gm-C [6], [7], [8] and digital [9]. All these circuit techniques have advantages and disadvantages, so the different characteristics of each defines its application niches and the new technologies generally emphasize the limits of these techniques in their applications areas. So, in the modern sub-micron technology the Gm-C filters can be operated over the entire VHF/UHF range [10], [11].

Generally the Gm-C integrators are very fast, because an open-loop transconductance amplifier drives the capacitive load. However, unfortunately, they are not very linear. Linearisation techniques exist, but often they affect the transconductor bandwidth and a linearity-bandwidth compromise must be done. The noise is another problem of Gm-C integrators. In this case, in the synthesis process the dynamic range must be optimised. Taking into account all these advantages and disadvantages, the most natural applications for the Gm-C filters are those where speed is vital, and the amplitude of signal can be kept relatively low.

In addition to the shortcomings mentioned above, it is also well known that the active filters are very sensitive to the excess phase of the active elements. The excess phase is a result of the transconductor limitation:

(1) nonzero output conductance and
(2) also the parasitic poles and zeros.

The main techniques used to build a high DC gain integrator with a very large bandwidth is choosing a simple transconductor topology without internal node [12] and loading it with a negative resistance that compensates the output resistance. An internal node is a node in the circuit schematic that has no direct connection to either an input or an output terminal or a bias or supply terminal of the circuit [12].

Theoretically, by combining these two techniques in the design process of the transconductor, an integrator with infinite DC gain and very large bandwidth results. In reality, the DC gain is dictated by the mismatch of input transistors and the mismatch of positive and negative resistive loads.

In this paper is presented a 1 MHz band-pass filter with optimum dynamic range (imposed by technology) and low distortion.

In the following sections the intermediate transfer functions method, used for filter synthesis, is briefly reviewed and also the space-state description of Gm-C filters is presented.

In the third section the transconductor is described, briefly analysed and then the SPICE simulation results are presented for emphasising its performances.

In the fourth section the synthesised filter is presented and also the good performances of the filter are emphasised by SPICE simulation.

2 The Intermediate Transfer Functions Synthesis Method

The intermediate transfer function synthesis method was developed for the AO-RC filter [13] but can be adapted for the Gm-C filter. The method is concerned in the realisation of a given nth order transfer function with a structure with n resistively interconnected integrators. In conformity with this method the design process consists of two steps: first a set of intermediate transfer functions (IFs) is selected and then the set is used for synthesizing the circuit that realises the given transfer function. The major advantage of this method is that the performance evaluation and optimisation can be performed at the abstract level of transfer function generation and not at the circuit topology level.

The AO-C filter can be described by a state-variable formula [13]:

$$\begin{aligned} &s\cdot\mathbf{x}(s)=\mathbf{A}\cdot\mathbf{x}(s)+\mathbf{b}\cdot u(s)+\boldsymbol{\varepsilon}(s)\\ &y(s)=\mathbf{c}^{T}\cdot\mathbf{x}(s)+d\cdot u(s)\end{aligned} \tag{1}$$

where the vector $\mathbf{x}(s)$ represents the circuit state (integrators outputs), matrix $\mathbf{A}$ describes the interconnections between the n integrators, vector $\mathbf{b}$ contains the coefficients that multiply the input signal $u(s)$ in order to be applied to the integrator's inputs, vector $\mathbf{c}$ contains the coefficients required to form the output, scalar d is the coefficient of the feed through component from input to output, and $\boldsymbol{\varepsilon}(s)$ is the vector containing the noise component at the integrator inputs.

The dual sets of IFs, $\{f_i(s)\}$ and $\{g_i(s)\}$ are given by:

$$\begin{aligned} &f_i(s)\overset{\Delta}{=}\frac{x_i(s)}{u(s)};\ \mathbf{f}(s)=(s\cdot\mathbf{I}-\mathbf{A})^{-1}\cdot\mathbf{b}\\ &g_i(s)\overset{\Delta}{=}\frac{y(s)}{\varepsilon_i(s)};\ \mathbf{g}^{T}(s)=\mathbf{c}^{T}\cdot(s\cdot\mathbf{I}-\mathbf{A})^{-1}\end{aligned} \tag{2}$$

The first set, $\{f_i(s)\}$, contains the transfer function from the filter input to the integrator outputs, and the second set, $\{g_i(s)\}$, can be physically interpreted as the integrator's noise gains.

Given a transfer function $t(s)$, IF synthesis is based on choosing a set of linearly independent functions, $\{f_i(s)\}$, having identical denominator polynomials, $e(s)$, and arbitrary numerator polynomials of degree less than n. From this set we can obtain the $\{\mathbf{A}, \mathbf{b}, \mathbf{c}, d\}$ parameters using the following relationships:

$$\begin{aligned} &\mathbf{A}=\mathbf{F}\cdot\mathbf{E}\cdot\mathbf{F}^{-1},\ \mathbf{b}=\mathbf{F}\cdot\mathbf{1},\\ &\mathbf{c}^{T}=\mathbf{t}^{T}\cdot\mathbf{F}^{-1},\ d=t_{n+1},\\ &t(s)=\mathbf{t}^{T}\cdot\mathbf{v}(s)+t_{n+1}\end{aligned} \tag{3}$$

$$\begin{aligned} &\mathbf{f}(s)=\mathbf{F}\cdot\mathbf{v}(s),\\ &\mathbf{g}(s)=\mathbf{G}\cdot\mathbf{v}(s),\ v_i(s)=1/(s-e_i),\ i=\overline{1,n},\\ &\mathbf{G}^{T}=\mathbf{H}\cdot\mathbf{F}^{-1}\end{aligned} \tag{3}$$

where $\mathbf{t}$ is a vector containing the n residues of $t(s)$ at the poles, t_{n+1} is the residue at $s=\infty$, $\mathbf{F}$ is a matrix containing the residues of the f functions evaluated at the poles, $\mathbf{G}$ is a matrix of the residues of the g functions, e_i are the roots of $e(s)$, $\mathbf{E}$ is the diagonal matrix having the natural modes e_i as its elements, $\mathbf{1}=(1, 1, ...1)^{T}$ and $\mathbf{H}$ is a diagonal matrix formed from the residues of $t(s)$.

The sensitivities to the $\mathbf{A}$, $\mathbf{b}$, $\mathbf{c}$, d parameters, integrator gain γ_i and the operational amplifier gain $\mu_i(s)$ are:

$$\begin{aligned} &S_{a_{ij}}^{t(s)}=g_i(s)\cdot f_i(s)\cdot\frac{A_{ij}}{t(s)},\\ &S_{b_i}^{t(s)}=g_i(s)\cdot\frac{b_i}{t(s)},\ S_{c_i}^{t(s)}=f_i(s)\cdot\frac{c_i}{t(s)}\\ &S_{d}^{t(s)}=\frac{d}{t(s)},\ S_{\gamma_i(s)}^{t(s)}=f_i(s)\cdot g_i(s)\cdot\frac{s}{t(s)},\\ &S_{\mu_i(s)}^{t(s)}=S_{\gamma_i(s)}^{t(s)}\cdot S_{\mu_i(s)}^{\gamma_i(s)}\end{aligned} \tag{4}$$

The following sensitivity invariant can be demonstrated [13]:

$$\sum_i f_i(s)\cdot g_i(s)=-\frac{dt(s)}{ds} \tag{5}$$

and we obtain a classical sensitivity result:

$$\sum_i S_{\gamma_i(s)}^{t(s)}=-\frac{s}{t(s)}\cdot\frac{dt(s)}{ds} \tag{6}$$

Because the sum of the sensitivities is constant, the minimum is obtained when all sensitivities are equal and, so, the IFs for minimum sensitivity realisation are:

$$f_i(s)\cdot g_i(s)=-\frac{1}{n}\cdot\frac{dt(s)}{ds},\ \forall i=\overline{1,n} \tag{7}$$

Noise signals injected at integrator inputs can be modelled by $\boldsymbol{\varepsilon}(s)$, and if we assume that the noise signals have white spectra with equal densities N_i^2, the output noise will have a power spectrum given by:

$$P_{n0}(\omega)=N_i^2\cdot\sum_i\left|g_i(j\cdot\omega)\right|^2 \tag{8}$$

with a RMS level of:

$$\left\|P_{n0}(\omega)\right\|=N_i^2\cdot\sqrt{\sum_i\left\|g_i(j\cdot\omega)\right\|_2^2} \tag{9}$$

where $\left\|g_i(j\cdot\omega)\right\|_2^2=\sqrt{\int_{-\infty}^{\infty}\left|g_i(j\cdot\omega)\right|^2\cdot d\omega}$.

This description can be adapted to the Gm-C filter. The following relation gives the current through a single capacitor of a GM-C filter:

$$C_i \cdot \dot{v}_{C_i} = G_{m\,i1} \cdot v_1 + G_{m\,i2} \cdot v_2 + \ldots + G_{m\,in} \cdot v_n + G_{mbi} \cdot u + \varepsilon_i \quad (10)$$

where v_i, $i = 1 \div n$, is the voltage on capacitor i, u is the input voltage and ε_i is the total noise current through the capacitor.

By scaling the relation (10) with C_i we obtain:

$$\dot{v}_{C_i} = \frac{G_{m\,i1}}{C_i} \cdot v_1 + \frac{G_{m\,i2}}{C_i} \cdot v_2 + \ldots + \frac{G_{m\,in}}{C_i} \cdot v_n + \frac{G_{mbi}}{C_i} \cdot u + \frac{\varepsilon_i}{C_i} \quad (11)$$

Interconnecting *n* capacitors with transconductors can be conveniently described be the same state-variable formula (1):

$$\begin{aligned} s \cdot \mathbf{x}(s) &= \mathbf{A} \cdot \mathbf{x}(s) + \mathbf{b} \cdot u(s) + \boldsymbol{\varepsilon}_S(s) \\ y(s) &= \mathbf{c}^T \cdot \mathbf{x}(s) + d \cdot u(s) \end{aligned} \quad (12)$$

where the states x_i are represented by capacitor voltages, matrix element A_{ij} is implemented by a transconductor with input voltage x_j and output voltage on i^{th} capacitor x_i, vector element b_i is implemented by the transconductor from the input u to state *i*, c_i is the multiplication coefficient of state *i* required to form the output voltage y, d is the multiplication coefficient of input voltage u and ε_S can model the current noise at the capacitor *i*.

So the meaning of $\{f_i(s)\}$ IFs set is the same as in the OA-RC filter synthesis and the physical meaning of $\{g_i(s)\}$ IFs set is the noise gain to the capacitor *i* to output. We can conclude that all results obtained in the OA-RC filter synthesis can be applied to the Gm-C filter.

3 The Basic Transconductor

In this section we present the transconductor and then we will analytically analyse its behaviour and will verify it by SPICE simulations. The transconductor is presented in figure 1. It is based on very well known CMOS inverter cells. For increasing the linearity, a balanced version is used. For a good operation of the transconductor, the MOS transistors within inverters must operate in saturation. That means that when the input and output DC voltages are approximately half of V_{DD}, the swing around the DC output voltage can be at most $2 \cdot \min(|v_{Pn}|, |v_{Pp}|)$ in order to obtain a good linearity.

Firstly, the advantages of using a balanced version for increasing linearity and DC gain will be analysed. If the MOS transistors operate in strong inversion and in saturation, the output current of a single inverter can be written as:

$$\begin{aligned} I_0 &= I_{Dn} - I_{Dp} = \\ &= a_2 \cdot (V_C + v_i)^2 + a_1 \cdot (V_C + v_i) + a_0 \end{aligned} \quad (13)$$

where I_{Dn} and I_{Dp} are the drain currents of N and P channels MOS transistors in strong saturation

$$\begin{aligned} a_2 &= \frac{K_n}{2} \cdot \frac{W_n}{L_n} - \frac{K_p}{2} \cdot \frac{W_p}{L_p} \\ a_1 &= K_p \cdot \frac{W_p}{L_p} \cdot (V_{DD} + V_{Pp}) - K_n \cdot \frac{W_n}{L_n} \cdot V_{Pn} \\ a_0 &= \frac{K_n}{2} \cdot \frac{W_n}{L_n} \cdot V_{Pn}^2 - \frac{K_p}{2} \cdot \frac{W_p}{L_p} \cdot (V_{DD} + V_{Pp})^2 \end{aligned} \quad (14)$$

and V_C is the input voltage for which the output current is zero:

$$V_C = \frac{V_{DD} + V_{Pp} + \sqrt{\frac{K_n}{K_p} \cdot \frac{W_n / L_n}{W_p / L_p}} \cdot V_{Pn}}{1 + \sqrt{\frac{K_n}{K_p} \cdot \frac{W_n / L_n}{W_p / L_p}}} \quad (15)$$

The balanced transconductor contains two matched inverters and so the differential output current is given by de following expression:

$$\begin{aligned} I_{out} &= I_{01} - I_{02} = \\ &= (2 \cdot a_2 \cdot V_C + a_1) \cdot v_{id} = g_{md} \cdot v_{id} \end{aligned} \quad (16)$$

This expression shows that the V-I conversion of the differential transconductor is linear even with non-linear inverters. Normally the MOS transistors have no ideal square law behaviour:

$$\begin{aligned} I_{Dn} &= \frac{K_n}{2} \cdot \frac{W_n}{L_n} \cdot \frac{(V_{GS} - V_{Pn})^2}{1 + \theta_n \cdot (V_{GS} - V_{Pn})} = \\ &= \frac{K_n}{2} \cdot \frac{W_n / L_n}{1 + \theta_n \cdot V_{ONn}} \cdot \frac{(V_{ONn} + V_i)^2}{1 + \frac{\theta_n \cdot V_i}{1 + \theta_n \cdot V_{ONn}}} \\ I_{Dp} &= \frac{K_p}{2} \cdot \frac{W_n / L_n}{1 + \theta_p \cdot V_{ONp}} \cdot \frac{(V_{ONp} - V_i)^2}{1 - \frac{\theta_p \cdot V_i}{1 + \theta_p \cdot V_{ONp}}} \end{aligned} \quad (17)$$

with

$$V_{ONn} = V_C - V_{Pn};\ V_{ONp} = V_{DD} - V_C + V_{Pp} \quad (18)$$

If we note with

$$\Theta_n = \frac{\theta_n}{1 + \theta_n \cdot V_{ONn}};\ \Theta_p = \frac{\theta_p}{1 + \theta_p \cdot V_{ONp}} \quad (19)$$

and then we expand in Taylor series the drain currents and assuming $(\Theta_n \cdot V_i)^2 << 1$, $(\Theta_p \cdot V_i)^2 << 1$ the expression (17) becomes:

$$I_{Dn} \cong \frac{K_n}{2} \frac{W_n / L_n}{1 + \theta_n V_{ONn}} (V_{ONn} + V_i)^2 (1 - \Theta_n V_i) \quad (20)$$

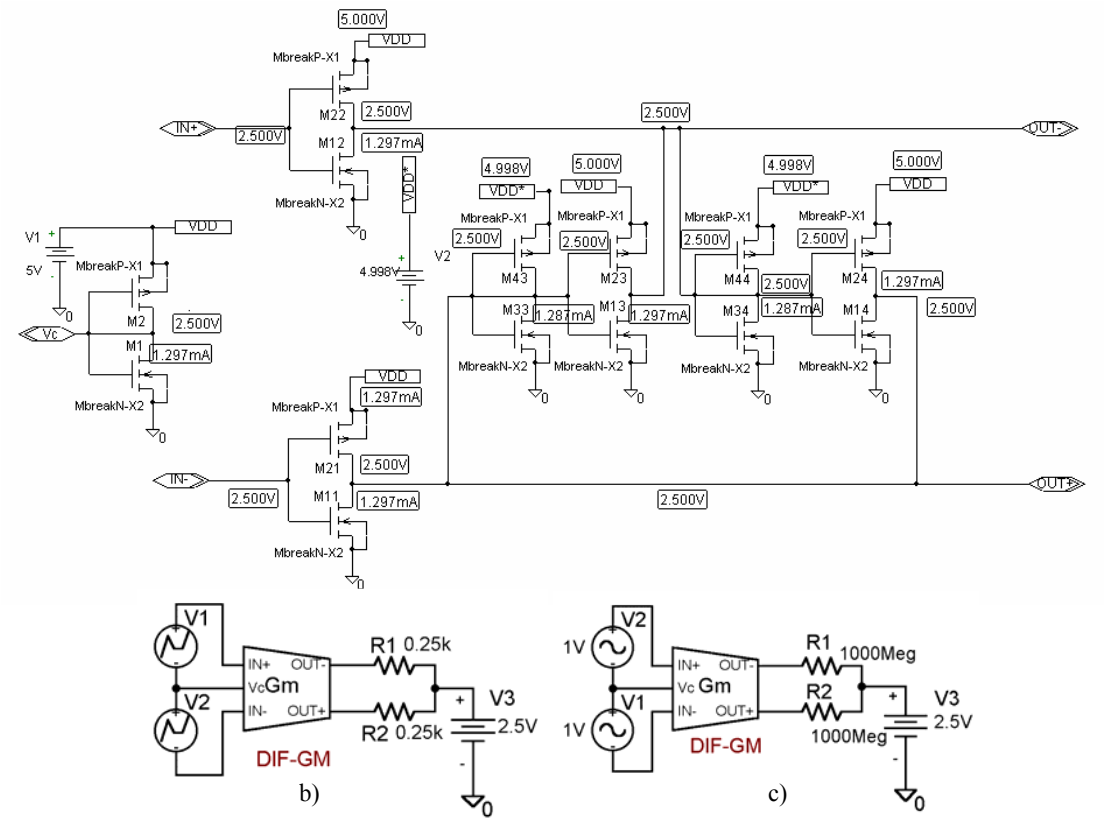


Figure 1. The transconductance element: a) the complete diagram dimensioned for Gm=2,2mA/V; b) the symbol of transconductor and simulation diagram used for emphasising the linearity of I-V conversion; c) the simulation diagram used for emphasizing the DC gain of the transconductor.

$$I_{Dp} \cong \frac{K_p}{2}\frac{W_p/L_p}{1+\theta_p V_{ONp}}\left(V_{ONp}-V_i\right)^2\left(1+\Theta_p V_i\right) \quad (20)$$

The output current of the differential transconductor is:

$$I_{out} = (I_{Dn1} - I_{Dn2}) + (I_{Dp2} - I_{Dp1}) =$$

$$= \left(\frac{K_n}{2}\cdot\frac{\Theta_n}{\theta_n}\cdot\frac{W_n}{L_n}\cdot\left(2+\Theta_n\cdot V_{ONn}\right)\cdot V_{ONn} + \right.$$

$$\left. + \frac{K_p}{2}\cdot\frac{\Theta_p}{\theta_p}\cdot\frac{W_p}{L_p}\cdot\left(2+\Theta_p\cdot V_{ONp}\right)\cdot V_{ONp}\right)\cdot V_{id} - \quad (21)$$

$$-\left(\frac{K_n}{8}\cdot\frac{\Theta_n^2}{\theta_n}\cdot\frac{W_n}{L_n}+\frac{K_p}{8}\cdot\frac{\Theta_p^2}{\theta_p}\cdot\frac{W_p}{L_p}\right)\cdot V_{id}^3$$

We can conclude that the harmonic distortions in a balanced transconductor are mainly third harmonic distortions. So that, for the short channel the device operates in strong inversion and saturation, the distortion being about 0.16% for a 1V-signal level. If the signal level is greater than 2V, the distortion level increases because it is very possible that the transistors do not operate in the saturation region for the entire swing signal. The SPICE simulations confirm these hypotheses.

In figure 2 is presented the dependence of output currents of the inverters and transconductor function on input signal level. The distortion level is 0.98% for 2V differential input voltage.

Four inverters control the common-mode level of the output voltages VOUT+ and VOUT-. Two of these inverters are shunted as resistance connected between the output nodes and the common-mode voltage level V_C. The effects of these output-connected inverters are described by the following equations:

$$\begin{aligned} g_{OUT+,d} &= 3/r_{0inv} + g_{m33} + g_{m43} - g_{m13} - g_{m23} \\ g_{OUT-,d} &= 3/r_{0inv} + g_{m34} + g_{m44} - g_{m14} - g_{m24} \\ g_{OUT+,cm} &= 3/r_{0inv} + g_{m33} + g_{m43} + g_{m13} + g_{m23} \\ g_{OUT-,cm} &= 3/r_{0inv} + g_{m34} + g_{m44} + g_{m14} + g_{m24} \end{aligned} \quad (22)$$

If the inverters are matched $g_{m33} = g_{m34} = g_{m3}$, $g_{m43} = g_{m44} = g_{m4}$, $g_{m13} = g_{m14} = g_{m1}$, $g_{m23} = g_{m24} = g_{m2}$, the output resistance is linear for differential signal and if $g_{m3} + g_{m4} < g_{m1} + g_{m2}$ its value can be very high, theoretically infinite if the difference between the terms of inequality become $-3/r_{0inv}$.

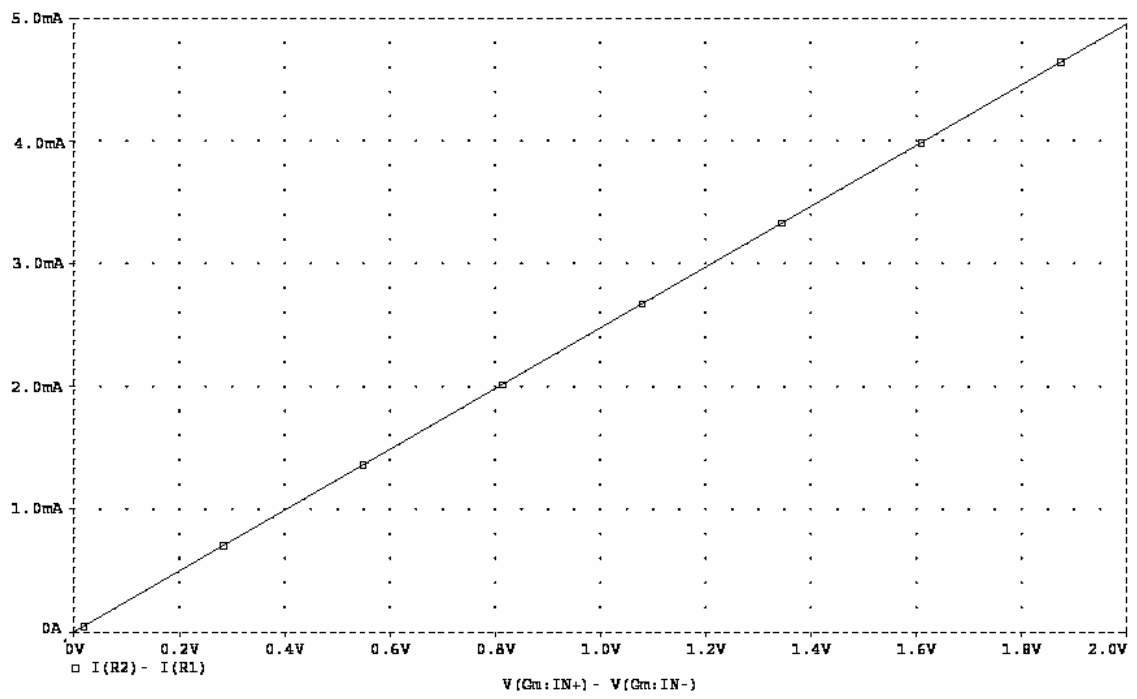


Figure 2. The V-I conversion of the transconductor.

For common-mode signals the output resistance is non-linear and has a low value. In this way the common-mode voltage level is controlled and its value is maintained V_C.

So, the DC gain of the transconductor for differential output signals is:

$$a_{0d} = g_{md} / g_{OUTd} \cong g_{md} / \Delta g_m \quad (23)$$

where Δg_m is the error due to mismatches. The following relation defines these mismatches:

$$g_{m3} + g_{m4} - g_{m1} - g_{m2} = -3 / r_{0inv} + \Delta g_m .$$

Using this technique, the DC gain becomes grater than 40dB. The tuning of DC gain can be done by means of V_{DD}. The amplitude-frequency characteristic obtained by SPICE simulation for the above-presented transconductor confirms that the DC gain is grater than 40dB (43dB). For simulation, SPICE parameters furnished by the American Microsystems Inc. for CMOS 1 μm technology were used.

4 The Filter

A third order filter with the following normalised transfer function:

$$t(s) = \frac{0.5}{s^3 + 2 \cdot s^2 + 2 \cdot s + 1} \quad (24)$$

has been implemented with the transconductor presented in the section above.

Because the structures that are synthesised using orthonormal and orthogonal intermediate transfer functions generally have a good dynamic range, good signal swing and low sensitivity, we chose these two types of IFs to be generated by the SSAF program [14].

The normalised topological elements, given by the SSAF program, are:

- for orthogonal intermediate functions

$$\mathbf{A} = \begin{bmatrix} 0 & 1 & 0 \\ -0,5 & 0 & 1 \\ 0 & -1,5 & -2 \end{bmatrix} \quad \mathbf{b} = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} \quad (25)$$

$$\mathbf{c}^{\mathrm{T}} = \begin{bmatrix} 0,5 & 0 & 0 \end{bmatrix} \quad \mathrm{d} = 0$$

- for orthonormal intermediate transfer functions

$$\mathbf{A} = \begin{bmatrix} 0 & 0,707 & 0 \\ -0,707 & 0 & 1,225 \\ 0 & -1,225 & -2 \end{bmatrix} \quad \mathbf{b} = \begin{bmatrix} 0 \\ 0 \\ 0,798 \end{bmatrix} \quad (26)$$

$$\mathbf{c}^{\mathrm{T}} = \begin{bmatrix} 0,724 & 0 & 0 \end{bmatrix} \quad \mathrm{d} = 0$$

Comparing the evaluated performances given by the SSAF program we chose to implement the transfer function by using the orthonormal IFs. In conformity with the SSAF program, this implementation will have the element sensitivities comparable with orthogonal realisation but will have a grater dynamic range and a maximal signal swing.

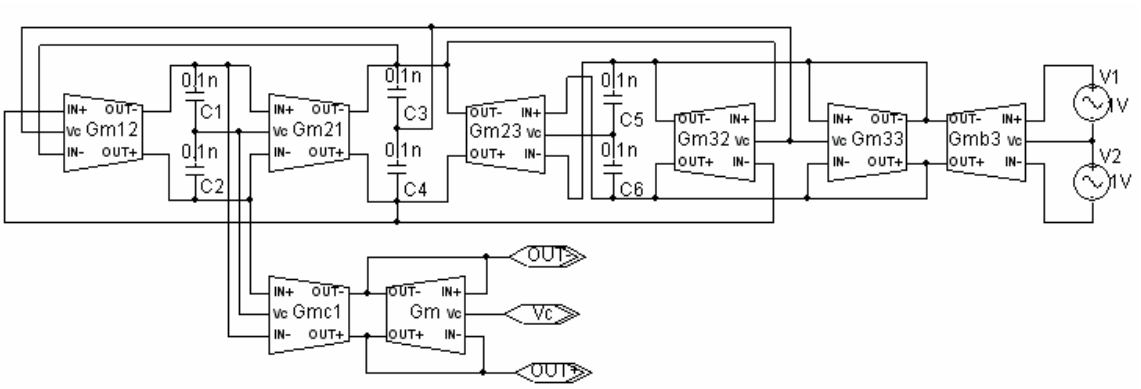
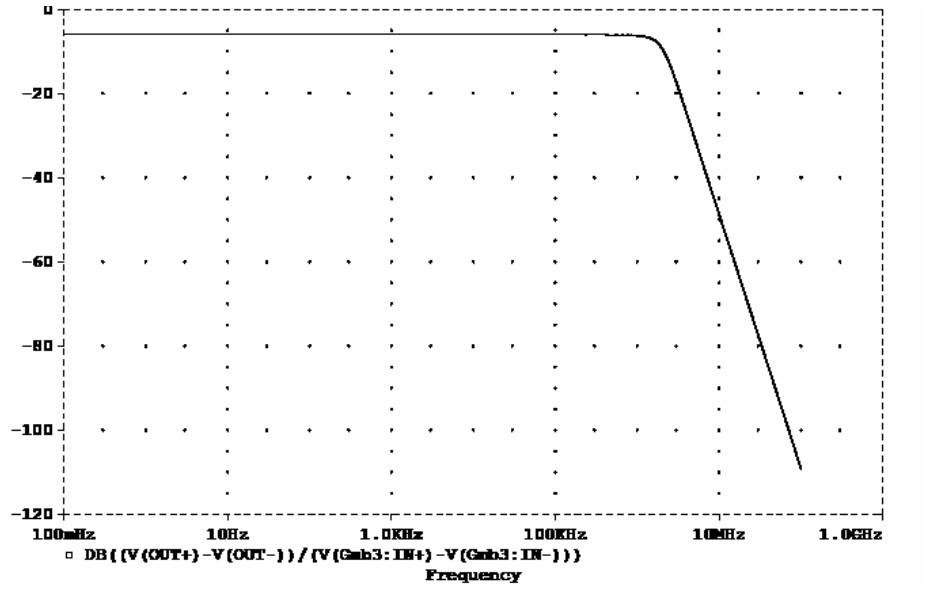
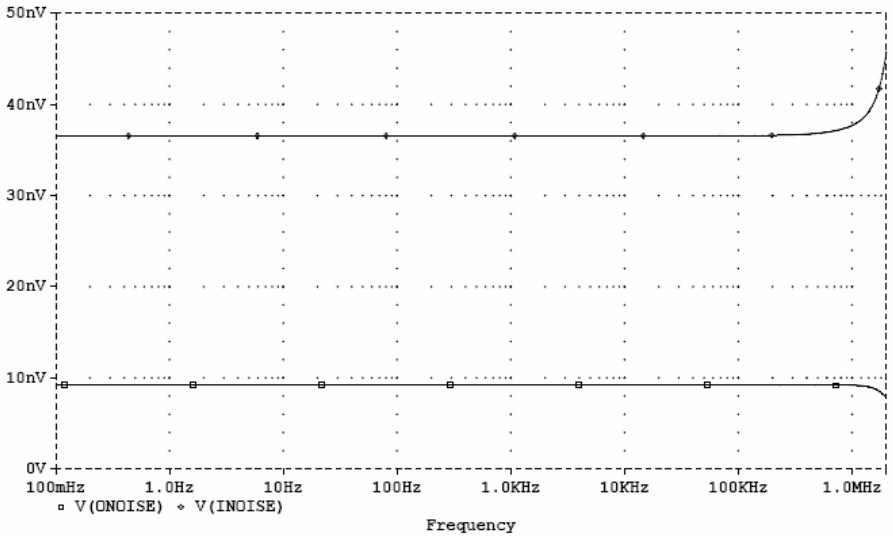


Figure 3. The structure of active 1MHz low-pass Gm-C filter



a)



b)

Figure 4. The main simulated performances of the low-pass active filter:
a) response of the filter; b) noise performances.

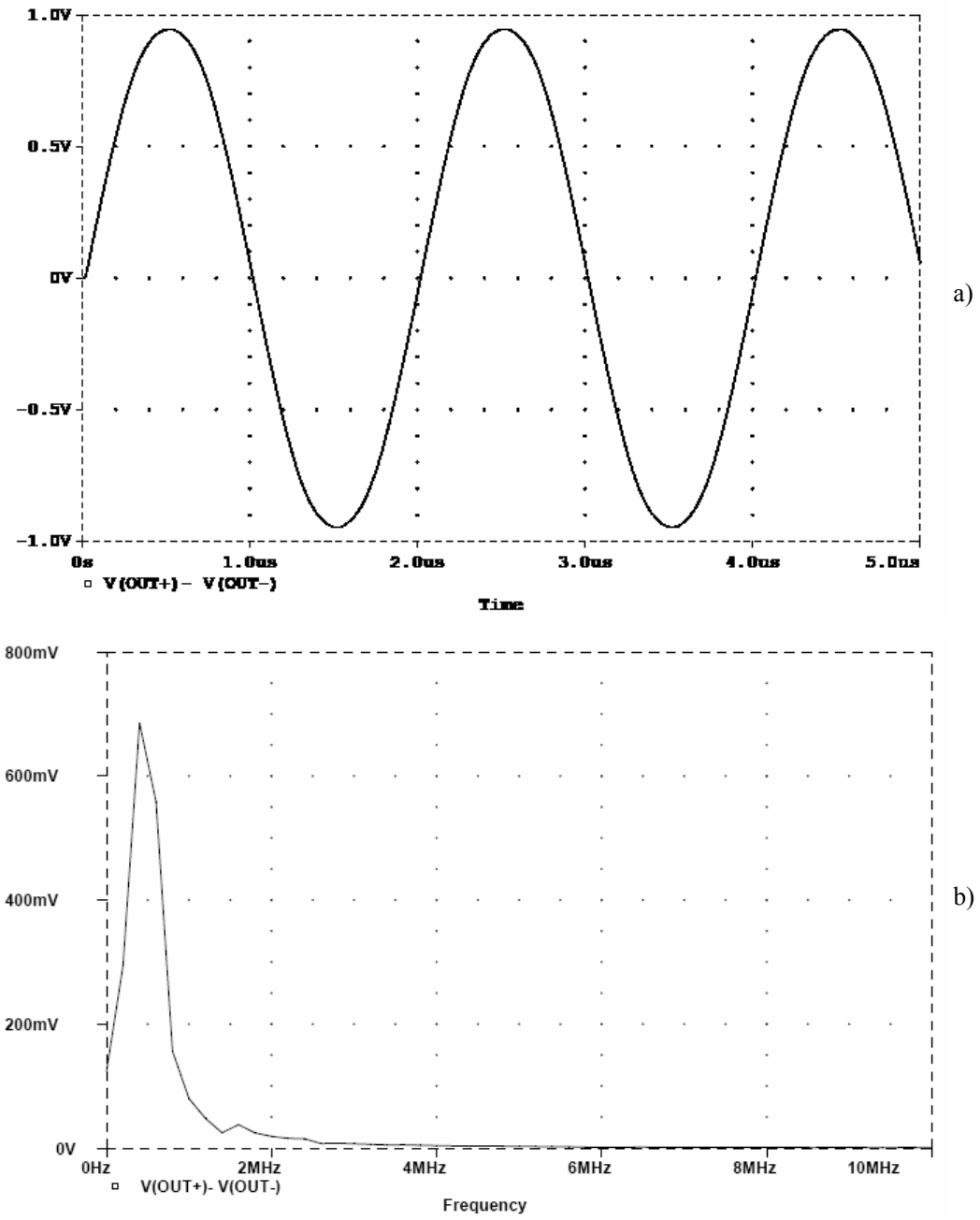


Figure 5. The simulated performances of the low-pass active filter at 500KHz input signal frequency: a) the output signal; b) the Fourier analysis result of the output signal.

The structure of active Gm-C filter is presented in figure 3. The required transconductance value was obtained via multiplying by $|a_{ij}|$ the W/L dimensional ratio of MOS transistors of the transconductor with g_{md}=1mA/V.

We have also made a fine tuning of channel dimensions of MOS transistors within inverters that are shunted as resistance connected between the output nodes and the common-mode voltage level V_C. The capacitor values were determined in order to obtain the desired 1MHz low-pass band.

The main simulated performances of the active filter are presented in figure 4. The simulated filter response is shown in figure 4.a. One can see that the filter response corresponds to the required transfer function.

The noise performances are presented in figure 4.b. The low noise level can be observed. The

dynamic range for the filter is grater than 80db.

For emphasising the output signal swing of the filter and transconductors and the distortions level, a transient analysis was made at a 500 kHz frequency. The simulations show that the output signal swings are approximately 1.5 V_{pp} and the total distortion is lower than –60dB (see figure 5 a and b). The total power consumption of the filter is 160mW.

Generally, to correct the frequency response of the integrated filter, which can vary due to technological process and temperature variations, a possibility to tune the cut-off frequency must exist. In integrated filters, an automatic tuning of cut-off frequency (f-tuning) is preferred. The f-control loop is usually a phase-locked loop [15], [16]. In many applications an automatic tuning of the quality factor is also made [17].

In our case the f-tuning of filter can be done by means of V_{DD}^{*}. With two Gm-C differential integrators connected in a loop, a voltage-controlled oscillator can be implemented. The command voltage for this VCO can be V_{DD}^{*}. This voltage will be copy to our filter and in this simple way the cut-off frequency will be kept to 1MHz.

5 Conclusion

In this paper a 1MHz low-pass Gm-C filter in CMOS process has been described. The filter was synthesised using the intermediate transfer functions method by using SSAF program created by us.

The presented full differential CMOS transconductor has a high DC gain (> 40dB) and a large bandwidth. That is why it is suitable to be used in high frequency filters. The transconductor also has a good linearity (<1%).

Using orthonormal intermediate transfer functions corresponding to an imposed transfer function, generated by the SSAF program, the low pass filter was synthesised. The filter response respects the transfer function, has a high dynamic range (>70dB), low noise and low total harmonic distortion.

The correction of the frequency response of the integrated filter can be made by means of V_{DD}^{*}.

6 Acknowledgement

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