A Low Complexity MIMO Channel Estimation Design and FPGA Implementation Using Orthogonal Matrix Triangularization

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Abstract:– The paper presents a low complexity channel estimation technique for multiple-input multiple-output (MIMO) wireless system that involves orthogonal matrix triangularization on training based least squares (LS) estimation to reduce a full rank matrix into a simpler form in order to eliminate matrix inversion. Complexity evaluation of the proposed approach is validated through MATLAB simulations in terms of mathematical operations, which shows that the method appreciably outperforms LS estimation at lower complexity and represents a good solution of MIMO channel estimation. The paper also provides design and implementation of a MIMO receiver on Xilinx Virtex™-4 XC4VLX60 FPGA that provides reconfigurability, resources by adopting the technique of parallelism. The system is developed based on modular structure which is simplifies system design, eases hardware update and facilitates testing the various modules in an independent manner.

Keywords:- MIMO, Channel estimation, Orthogonal matrix, FPGA, Least square

1. Introduction

Multiple-input multiple-output (MIMO) communication system, which plays an important role in improving wireless communications, is in the forefront of wireless research. The technique has recently emerged as one of the most significant technical breakthroughs in modern communication because of its ability to provide high efficiency and data rate [1]. Numerous researches on antenna technology are ongoing both in industry and academia to provide reliable communication systems [2-6]. However, multiple antenna system relies upon the knowledge of channel state information (CSI) at the receiver for data detection and decoding. Therefore, an accurate and robust estimation of wireless channel is of crucial importance for coherent data recovery.

A considerable number of channel estimation methods have already been studied by different researchers for MIMO system [7-12]. Least square (LS) is a training based estimation technique for which the channel coefficients are treated as deterministic but unknown constants [13]. In practice, LS estimation is more frequently used due to its acceptable performance, but this estimation involves matrix inversion which results in high computational complexity and hence undesirable for hardware implementation. To reduce the complexity, orthogonal matrix triangularization has been applied on MIMO systems in this paper. Orthogonal matrix triangularization, which reduces a full rank matrix into a simpler form, is a matrix factorization technique that is preferable over other matrix optimization techniques as it guarantees numerical stability by minimizing errors caused by machine roundoffs and clever implementation in highly parallel array architecture [14], [15]. Compared with the state of art algorithmic studies, research in hardware design and implementation of communication system remains relatively new and challenging topic. There are several alternative of implementing theoretical concepts of communication system on hardware, such as, DSP, ASIC, FPGA etc. Rao et al. put forward a classification scheme for different types of hardware implementation in [16]. FPGA combines the versatility of DSP and the performance of ASIC solutions. Moreover, FPGA solution is reconfigurable which result is reduced prototyping cost [17], [18]. The design and implementation of MIMO systems has become more and more attractive to researchers as has been observed in the past few years [19-22]. Different practical implementation aspects of real-time systems are presented in [23], [24], [25]. But these systems are designed based on sequential processing and hence resource is not properly utilized.

This paper presents a proficient channel estimation method for MIMO system by employing orthogonal matrix triangularization that minimizes computational complexity. This paper also focuses

on the FPGA design and implementation of the system that not only provides a faster and real-time solution but also ensures resource utilization by taking the advantage of parallel processing. The hardware is designed in modular structure which facilitates testing different part of the system independently and makes the hardware update easy.

The rest of the paper is organized as follows. In section 2, the low complexity MIMO channel estimation technique is introduced. Section 3 presents the FPGA design and implementation of the MIMO decoder. Section 4 describes the system development methodology. Section 5 comprises a number of experimentations validating the proposed method, showing its significant advantages over traditional LS estimation in complexity improvement. This section also shows the hardware implementation results of MIMO receiver. Finally section 6 highlights some of the distinct features of the proposed approach and draws the conclusion.

2. Low Complexity Channel Estimation

Space-time block coding (STBC) is a remarkable spatial and time diversity scheme that improves signal quality by using simple processing at the transmitter and linear decoding at the receiver [26], [27]. In an STBC scheme the symbols s_0 and s_1 are transmitted simultaneously from two transmit antennas Tx_1 and Tx_2 respectively, at symbol period *t*. At the next symbol period *t*+*T*, Tx_1 transmits symbol $-s_1^*$ and Tx_2 transmits symbol s_0^*. Figure 1 shows a multiple antenna systems with two transmit antennas and two receive antennas.

The received signal can be expressed as

$$\mathbf{R} = \mathbf{HS} + \mathbf{W} \tag{1}$$

where $\mathbf{W}$ is additive white Gaussian noise (AWGN), and $\mathbf{H}$ which can be denoted by the general term $\{h_{ji}\}$, is the channels between two transmit and two receive antennas. The received signals at time *t* are

$$\text{at Receiver 1: } r_1 = s_0 h_{11} + s_1 h_{21} + w_1 \tag{2}$$

$$\text{at Receiver 2: } r_3 = s_0 h_{12} + s_1 h_{22} + w_3 \tag{3}$$

The signals received at time *t*+*T* are

$$\text{at Receiver 1: } r_2 = -s_1^* h_{11} + s_0^* h_{21} + w_2 \tag{4}$$

$$\text{at Receiver 2: } r_4 = -s_1^* h_{12} + s_0^* h_{22} + w_4 \tag{5}$$

w_1, w_2, w_3 and w_4 are complex Gaussian random variables representing noise and interference. The transmitted symbols s_0 and s_1 can be estimated in a maximum likelihood fashion by first combining the received signals according to the following equations

$$\tilde{s}_0 = h_{11}^* r_1 + h_{21} r_2^* + h_{12}^* r_3 + h_{22} r_4^* \tag{6}$$

$$\tilde{s}_1 = h_{21}^* r_1 - h_{11} r_2^* + h_{22}^* r_3 - h_{12} r_4^* \tag{7}$$

and using a standard maximum likelihood detector to attempt to recover s_0 and s_1 from $\tilde{s}_0$ and $\tilde{s}_1$.

The receiver requires channel knowledge in order to recover the transmitted signal properly. In a training based channel estimation, where $\mathbf{x}$ is the transmitted training signal, the received symbols is expressed as

$$\mathbf{y} = \mathbf{Hx} + \mathbf{w} \tag{8}$$

where $\mathbf{w}$ is the noise response. The channel response $\mathbf{H}$ is assumed to be random and quasi-static within two transmission blocks. The LS approach solves the equation (8) by minimizing the cost function as,

$$J(\mathbf{H}) = (\mathbf{y} - \mathbf{Hx})^H (\mathbf{y} - \mathbf{Hx}) \tag{9}$$

The gradient of (9) is given below,

$$\frac{\partial J(\mathbf{H})}{\partial \mathbf{H}} = -2\mathbf{x}^H \mathbf{y} + 2\mathbf{x}^H \mathbf{x} \tag{10}$$

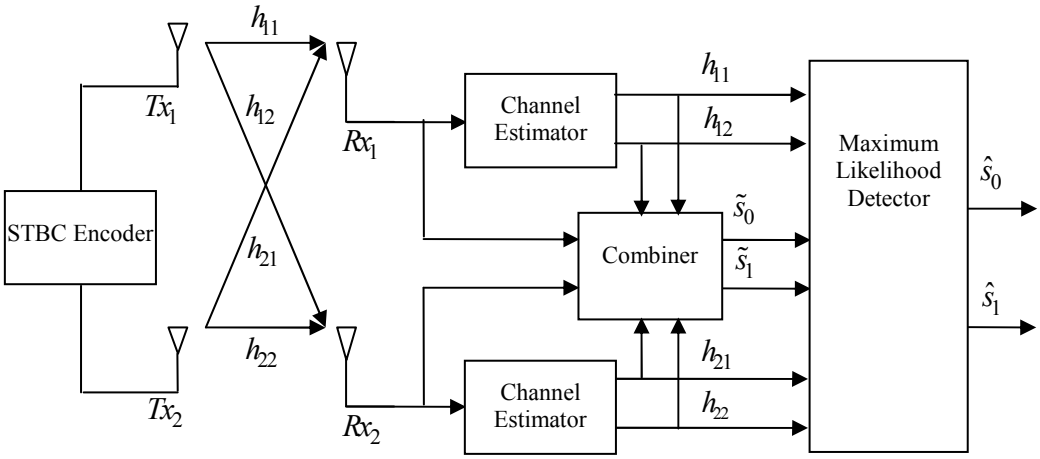

Figure 1. MIMO wireless System

Minimizing the gradient to zero yields the LS estimation $\hat{\mathbf{H}}$ of the channel response obtained by

$$\hat{\mathbf{H}} = (\mathbf{x}^H \mathbf{x})^{-1} \mathbf{x}^H \mathbf{y} \quad (11)$$

The inversion of $\mathbf{x}^H \mathbf{x}$ has a high complexity and will significantly increase when the number of transmit antennas increases. To avoid complexity because of matrix inversion, orthogonal matrix triangularization is applied on $\mathbf{x}$. In this approach, a series of reflection matrix is applied to the matrix, $\mathbf{x}$, column by column to annihilate the lower triangular elements. The reflection transformations are orthonormal matrices that is

$$\mathbf{A} = (\mathbf{I} + \beta \mathbf{v}\mathbf{v}^H) \quad (12)$$

where $\mathbf{v}$ is the Householder vector and $\beta = -2\|\mathbf{v}\|_2^2$. For the matrix $\mathbf{x}$, to annihilate the lower elements of the *k*-th column the $\mathbf{A}_k$ is constructed as shown in Figure 2.

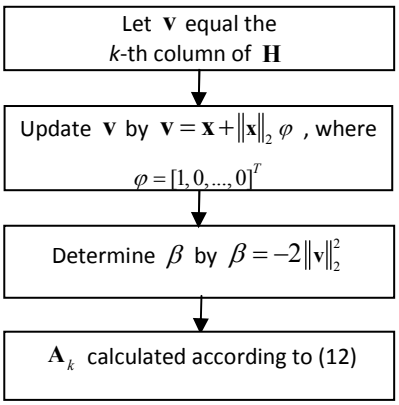

Figure 2. $\mathbf{A}_k$ Construction steps

The $\mathbf{A}_k$ formed from the above steps are pre-multiplied by $\mathbf{x}$ sequentially as follows

$$\mathbf{A}_n \ldots \mathbf{A}_1 \mathbf{H} = \begin{bmatrix} \mathbf{P} \\ \mathbf{0} \end{bmatrix} \quad (13)$$

where, $\mathbf{P}$ is an upper triangular matrix, $\mathbf{0}$ is a null matrix, and the sequence of reflection matrices form the complex transpose of the orthogonal matrix $\mathbf{Q}^H$, i.e. $\mathbf{Q}^H = \mathbf{A}_n \ldots \mathbf{A}_1$. Thus (13) is written as

$$\mathbf{x} = \mathbf{Q} \begin{bmatrix} \mathbf{P} \\ \mathbf{0} \end{bmatrix} \quad (14)$$

The error function for estimation (11) can be expressed as

$$\varepsilon = \mathbf{y} - \hat{\mathbf{H}}\mathbf{x}, \text{ if } \varepsilon = 0, \text{ then } \mathbf{y} = \hat{\mathbf{H}}\mathbf{x} \quad (15)$$

By combining (14) and (15) the received signal stands

$$\mathbf{y} = \hat{\mathbf{H}}\mathbf{x} = \hat{\mathbf{H}}\mathbf{Q} \begin{bmatrix} \mathbf{P} \\ \mathbf{0} \end{bmatrix} \quad (16)$$

The Hermitian of $\mathbf{Q} \begin{bmatrix} \mathbf{P} \\ \mathbf{0} \end{bmatrix}$ is multiplied to both sides of (16) to derive the proposed channel estimation

$$\hat{\mathbf{H}} = \mathbf{y}\mathbf{Q}^H \begin{bmatrix} \mathbf{P} \\ \mathbf{0} \end{bmatrix}^H \quad (17)$$

As $\mathbf{P}$ is an upper triangular matrix, $\hat{\mathbf{H}}$ can be solved through back-substitution. This approach proves itself an attractive solution of channel estimation that results in complexity reduction of the multiple antenna system.

3. FPGA Implementation

The hardware is designed in modular structure in order to simplify system design. This section illustrates the hardware design of a 2×2 antenna receiver. The main emphasis is led on the ability to extend the hardware in an easy way if the system requires hardware updates.

The receiver combines the received signals and the channel matrix obtained from the channel estimation module. Hardware design and implementation of the receiver is based on (6) and (7). However the complex values and their operations of the equations cannot be simply implemented using hardware description language. These are expanded to real and imaginary parts to simplify implementation.

$$\begin{aligned} &+\mathrm{Re}(h_{21}) \times \mathrm{Re}(r_3) + \mathrm{Im}(h_{21}) \times \mathrm{Im}(r_3) \\ &+\mathrm{Re}(h_{22}) \times \mathrm{Re}(r_4) + \mathrm{Im}(h_{22}) \times \mathrm{Im}(r_4) \end{aligned} \quad (18)$$

$$\begin{aligned} &-\mathrm{Re}(h_{12}) \times \mathrm{Im}(r_2) + \mathrm{Im}(h_{12}) \times \mathrm{Re}(r_2) \\ &+\mathrm{Re}(h_{21}) \times \mathrm{Im}(r_3) - \mathrm{Im}(h_{21}) \times \mathrm{Re}(r_3) \\ &-\mathrm{Re}(h_{22}) \times \mathrm{Im}(r_4) + \mathrm{Im}(h_{22}) \times \mathrm{Re}(r_4) \end{aligned} \quad (19)$$

$$-\mathrm{Re}(h_{11}) \times \mathrm{Re}(r_2) - \mathrm{Im}(h_{11}) \times \mathrm{Im}(r_2) + \mathrm{Re}(h_{22}) \times \mathrm{Re}(r_3) + \mathrm{Im}(h_{22}) \times \mathrm{Im}(r_3) - \mathrm{Re}(h_{21}) \times \mathrm{Re}(r_4) - \mathrm{Im}(h_{21}) \times \mathrm{Im}(r_4) \quad (20)$$

$$+\mathrm{Re}(h_{11}) \times \mathrm{Im}(r_2) - \mathrm{Im}(h_{11}) \times \mathrm{Re}(r_2) + \mathrm{Re}(h_{22}) \times \mathrm{Im}(r_3) - \mathrm{Im}(h_{22}) \times \mathrm{Re}(r_3) + \mathrm{Re}(h_{21}) \times \mathrm{Im}(r_4) - \mathrm{Im}(h_{21}) \times \mathrm{Re}(r_4) \quad (21)$$

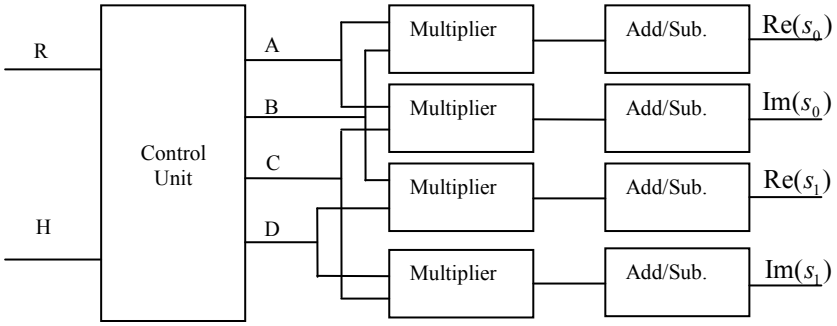

Figure 3. Block diagram of MIMO decoder

The equations use up most of the resources available on the FPGA of the hardware if these are directly converted into hardware language and synthesized. To solve the problem, a new design is considered as shown in Figure 3. The design has four functional multiplier units, and four associated add/subtract units with registers to accumulate the totals. There is also a control unit, implemented as a state machine, to multiplex inputs to different functional units, and also control whether add/subtract units add or subtract. The meaning of the A, B, C and D signal can be found by careful examination of (18) to (21). If the equations are investigated carefully, it can be noted that the apparently complex equations follow a pattern. In particular, there are four distinct sets of operands for the multiplication operations. These sets, labeled A, B, C and D, are shown in Table 1.

Table 1. Sets of operand outputs from control unit

Set	First use	Second use
A	Operand 1 in (18)	Operand 1 in (19)
B	Operand 2 in (18)	Operand 2 in (20)
C	Operand 2 in (19)	Operand 2 in (21)
D	Operand 2 in (20)	Operand 2 in (21)

To explain the meaning of Table 1, consider set A as an example. The first usage of A is listed as 'Operand 1 in equation (18)' and the second is 'Operand 1 in equation (19)'. Note, in particular, the first (left hand) operand of any multiplication in (18) is the same as the first operand of the corresponding multiplication in (19). Because these operands are always the same they are grouped together as set A. Table 1 similarly specifies the other sets.

The design calculates all the equations for the symbol estimates in parallel. There is one multiplier and one add/subtract unit for each equation being implemented. By exploiting these pairings the control unit is able to multiplex the required inputs through to all of the multiplier functional units using only four multiplexers instead of the eight that would otherwise be required.

4. System Development Methodology

Figure 4 presents a flow chart of the overall design process of FPGA implementation of the system. The system is first examined with high level simulation using MATLAB 7.0.

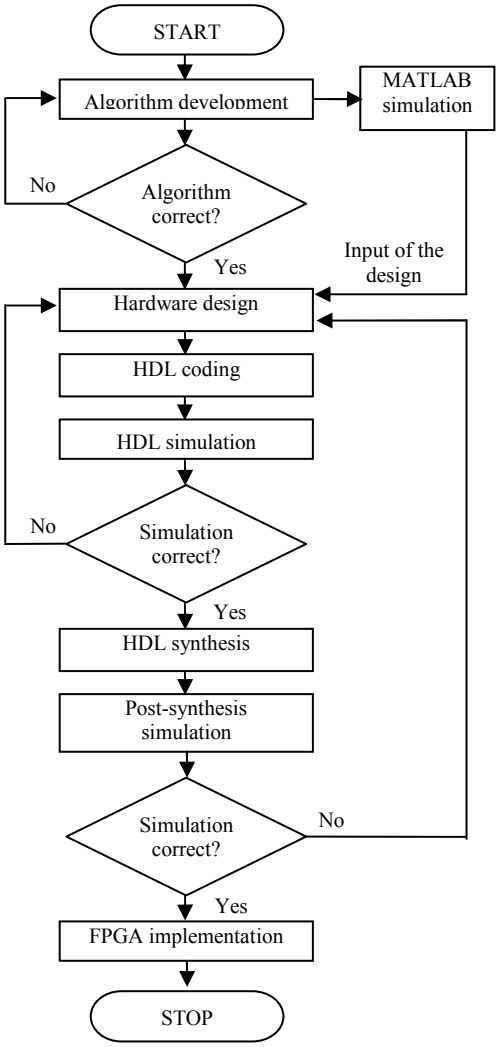

Figure 4. Flow chart of design methodology

Based on the results obtained from the simulation the specifications are matched with theoretical specifications to carry out the hardware design for MIMO system. The design is translated to hardware description language (HDL), and simulations are performed to confirm that the conceptualized design does function correctly. Functionality of the design has been verified through behavioral simulations. Then synthesis is performed to convert the high-level abstract description of the design to actual components at the gate and flip-flop level. The next step in the design flow is post-synthesis simulation. The earlier simulation at a higher level of abstraction does not take into account specific implementation of the hardware components that the design is using, but the post-synthesis simulation does. If post-synthesis simulation unveils problems, the design is further modified and timing requirements are met. Next, the process moves into specific realization of the design. Finally the design is implemented on FPGA.

5. Results and Discussion

a. Complexity Comparison

A new channel estimation method is proposed in this paper for MIMO communication system by employing orthogonal matrix triangularization which minimizes the computational complexity. The coding scheme of MIMO considered in this work is STBC which is an attractive approach for improving quality in wireless links. The channels are assumed to be static within a data block and vary independently among data blocks. The BER curve is obtained by transmitting 100,000 data block realizations for each SNR point and each data block length is set to 100. The channel is considered to have 16 paths where the amplitude of each path is independent and identically distributed (i.i.d.) according to the Rayleigh distribution with zero mean and unit variance. In this section, simulation results are presented that illustrate the complexity of the proposed technique. The performance limit for different antenna configuration is quantified in terms of BER over a range of SNR which is particularly attractive for wireless communications measurement. The comparison between different complexity plots are investigated by computer simulations using MATLAB 7.0.

The computational complexity of the LS estimation and the proposed estimation methods are measured and compared in terms of number of mathematical operations. For consistent comparison, the complex operations are converted to real operation equivalents. Table 2 summarizes the real equivalent operations for various complex operations. Each type of real operations has different levels of complexity when implemented in the hardware. Table 3 shows the number of floating point operations for each real operation.

Table 2. Number of real operations in every operations

Complex Operations	Number of Real Operations		
	Mult.	Div.	Add./Sub
Multiplication	4	2	0
Division	6	3	2
Add./Sub.	0	0	2

Table 3. Operation count for every real operation

Real Operations	Operation Counts
Multiplication/Addition/ Subtraction	1
Division	6
Square root	10

The complexity comparison between LS and the proposed channel estimation is depicted in terms of real operations in Figure 5. The impacts of varying antenna configurations on the estimation methods are studied. When the number of antennas increases, the size of unknown parameters also increases and as a result complexity increases in both estimation techniques. The complexity of the proposed method increases almost linearly with respect to the number of transmit antenna, whereas for LS method it increases exponentially at significantly higher rate. Thus the matrix triangularization channel estimation method is lower in complexity and proves itself a better choice for low complexity channel estimation.

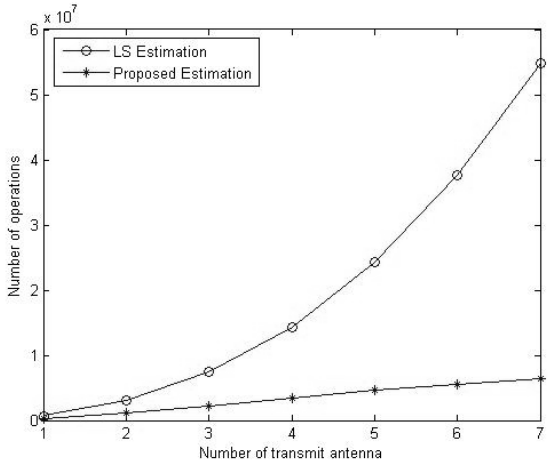

Figure 5. Complexity comparison between LS and the proposed channel estimation

b. FPGA Implementation

The FPGA implementation process starting from system specification is outlined in Figure 6. The system is first examined with a high level simulation using MATLAB. Different sub-blocks of the system are then translated for hardware implementation. The HDL used in this work is VHDL for its flexibility of coding styles and suitability for handling very large and complex designs. Xilinx ISE 10.1 and XST engine are used for VHDL synthesis and place-and-route, while Mentor ModelSim XE III 6.3c is used to run functional and post place-and-route simulations. After compilation, simulation and synthesis, configuration files are generated which are used to configure FPGA device. In every step the outputs are verified by comparing with MATLAB simulation result.

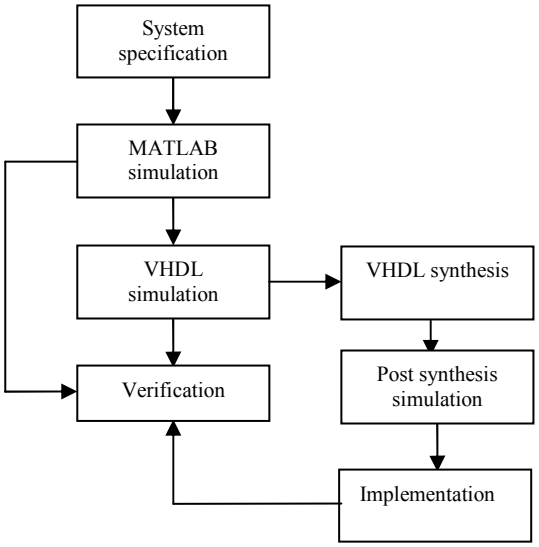

Figure 6. Design steps of FPGA implementation

The MIMO receiver is implemented on a Xilinx Virtex™-4 LX MB Development Kit. The board includs a Xilinx XC4VLX60 FPGA device, 64MB of DDR SDRAM, 4MB of Flash, 16-bit LVDS Transmit and Receive ports, programmable LVDS clock source, USB-RS232 Bridge, a 10/100 Ethernet PHY, 100 MHz clock source, RS-232 port, and additional user support circuitry to develop a complete system. The board also supports the P240 expansion module standard, allowing application specific expansion modules to be easily added. The FPGA in the board has a total of 59,904 logic elements available for system development. With all these features the device can be configured to implement very complex systems.

Figure 7 shows the picture of the experimental setup of the work. The task of the decoder at MIMO receiver is to combine the signals simultaneously received in all antennas to construct an improved signal, from which the transmitted signal can be

Figure 7. Experimental setup of FPGA implementation

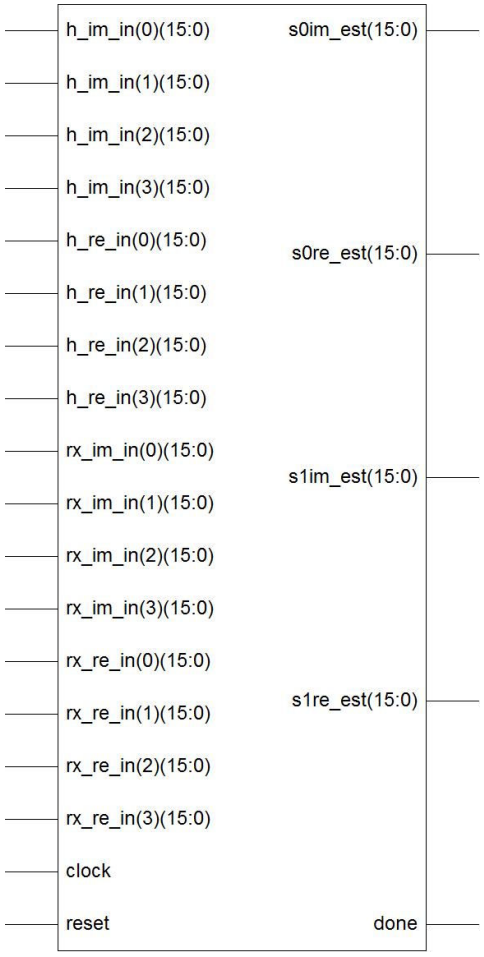

Figure 8. Schematic of MIMO decoder

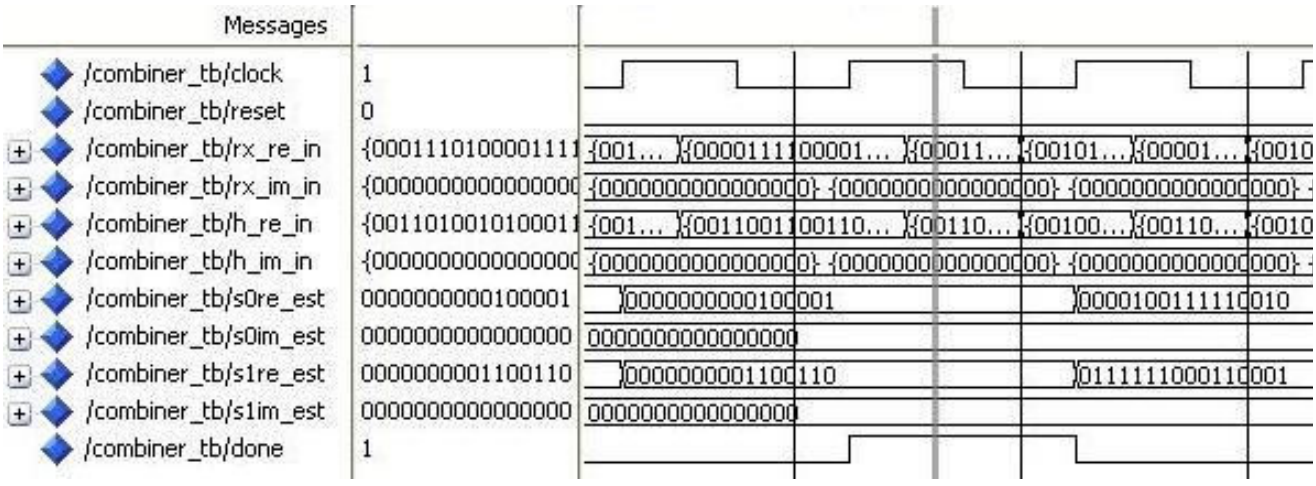

Figure 9. Simulation result of MIMO decoder

recovered. The decoder at the receiver takes the input of four 16 bit real and imaginary parts of the channel estimate and four 16 bit real and imaginary parts of the received signals. The design is a multi-cycle implementation; it takes multiple clock cycles to compute the results. The multipliers take one clock cycle to calculate a product and the add/subtract units also take one clock cycle. Therefore two symbol estimates (real and imaginary parts) are produced every 8 clock cycles. The 'done'

signal points the end of this 8 clock cycles. A 'reset' signal is also used to reset the decoder. Because of the pairing of the operands as mentioned in Table 1, the control logic is able to multiplex the required inputs through to all of the multiplier functional units using only four multiplexers instead of the eight that would otherwise be required. Figure 8 presents the schematic of the MIMO decoder and Figure 9 illustrates the simulation result of the decoder.

The decoder design is successfully synthesized using XST engine and then placed and routed on the targeted FPGA. Table 4 summarizes the device utilization summery of the implementation. It can be seen that only a small percentage of the available resources of the FPGA board is used for the design. This utilization should be considered as an upper bound as there exists a variety of possible optimizations not yet applied to the design.

Table 4. Device utilization summary

	Available Resources	Resource Used	Utilization %
Slices	26,624	393	1.47
Flip Flops	53,248	355	0.67
LUTs	53,248	472	0.89
Pins	448	323	72.09

6. Conclusion

A matrix factorization based MIMO channel estimation method is presented in this paper for complexity cutback. The technique is compared with training based LS estimation that proves extensive improvement in terms of complexity, and thus stands for a good way out of channel estimation problem. This paper also illustrates the design methodology and implementation of MIMO receiver, which involves Xilinx Virtex™-4 FPGA for fast parallel processing. More emphasis is led on the ability to extend the hardware in an easy way if the system requires hardware update. This litheness and resource utilization can thus be very efficient for embedded hardware realizations of next generations of wireless systems.

7. Acknowledgement

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8. References

[1] J. Mietzner, R. Schober, L. Lampe, W. H.Gerstacker and P. A. Hoeher, Multiple-Antenna Techniques for Wireless Communications – A Comprehensive Literature Survey, *IEEE Communications Surveys & Tutorials*, *vol. 11, no.2*, Second Quarter 2009, pp. 87-105.

[2] Mohammad Tariqul Islam, Ahmed Toaha Mobashsher and Norbahiah Misran, Small multi-band microstrip antenna for wireless applications, *IEICE Electronic Express*, vol 7, no. 21, 2010, pp. 1629-1634.

[3] Rezaul Azim, Mohammad Tariqul Islam Norbahiah Misran, A Planar Monopole Antenna for UWB Applications, *International Review of Electrical Engineering*, vol. 5, no. 4, 2010, pp. 1848-1852.

[4] Mohammad Tariqul Islam, Ahmed Toaha Mobashsher and Norbahiah Misran, Design of a microstrip patch antenna using a novel U-shaped feeding strip with unequal arm, *Electronics Letters*, vol. 46, no. 14, 2010, pp. 968-970.

[5] Mohammed Nazmus Shakib, Mohammad Tariqul Islam and Norbahiah Misran, Stacked Patch Antenna with Folded Patch Feed for Ultrawideband Application, *IET Microwave, Antenna and Propagation*, vol. 4, no. 10, 2010, pp. 1456-1461.

[6] Rezaul Azim, Mohammad Tariqul Islam and Norbahiah Misran, Printed Planar Antenna for Wideband Applications, *Journal of Infrared, Millimeter, and Terahertz Waves*, 31, 2010, pp. 969-978.

[7] H.M. Wang, X.Q. Gao, B. Jiang, X.H. You and W. Hong, Efficient MIMO channel estimationusing complementary sequences, *IET Communications, vol. 1*, Oct. 2007, pp. 962-969.

[8] G. Kang, M. Weckerle, E. Costa, and P. Zhang, "Time and frequency domain joint channel estimation in multi-branch Systems," Proceedings of the 5th WSEAS Int. Conf. on Applied Electromagnetics, Wireless and Optical Communications, Corfu, Greece, August 23-25, 2005, pp. 25-30.

[9] Z. Lu, T. Zhang, Z. Gong and Liejun Wang, "Challenge of channel estimations and its way out in MIMO OFDM systems for mobile wireless channels," Wseas Transactions on Communications, Issue 2, Volume 7, pp. 92-98, 2008

[10] B. Sobhani, "A new space-repetition code based on one bit feedback compared to alamouti space-time code," Proceedings of the 4th

WSEAS Int. Conference on Electromagnetics, Wireless and Optical Communications, Venice, Italy, November 20-22, 2006.

[11] X. Ma, L. Yang and G.B. Giannakis, Optimal training for MIMO frequency-selective fading channels, *IEEE Trans. Wireless Commun., vol. 4, no. 2*, March 2005, pp. 453–466.

[12] M. Biguesh and A.B. Gershman, Training-based MIMO channel estimation: A study of estimator tradeoffs and optimal training signals, *IEEE Transactions on Signal Processing, vol. 54, no. 3*, 2006, pp. 884-893.

[13] S. Sorrentino, D. Greco, L. Reggiani, Least squares channel estimation for IEEE 802.16e systems based on adaptive taps selection, *Proc. IEEE Vehicular Technology Conference, VTC Spring 2008,* May 2008, pp. 1524 – 1528.

[14] G.H. Golub and C.F. Van Loan, *Matrix Computations Third Edition* (John Hopkins University Press, Maryland, 1996).

[15] M. W. Numan, M. T. Islam, N. Misran, Performance and Complexity Improvement of Training Based Channel Estimation in MIMO Systems, *Progress In Electromagnetics Research C*, vol. 10, 2009, pp. 1-13.

[16] R. Rao, W. Zhu, S. Lang, C. Oberli, D. Browne, J. Bhatia, J. F. Frigon, J. Wang, P. Gupta, H. Lee, D. N. Liu, S. G. Wong, M. Fitz, B. Daneshrad, O. Takeshita, Mulit-Antenna Testbeds for Research and Education in Wireless Communications, *IEEE Communications Magazine, vol. 42, no. 12,* 2004, pp. 62-70.

[17] C. H. Roth Jr, L. K. John, *Digital Systems Design using VHDL Second Edition* (Thomson Learning, 2007).

[18] S. Karimi, P. Poure, S. Saadate, FPGA in the loop prototyping methodology for fully digital power electronics system control design, *International Review of Electrical Engineering, vol. 3, no. 2,* April 2008, pp. 281-288.

[19] S. Yu, T. H. Im, C. H. Park, J. Kim, and Y. S. Cho, An FPGA Implementation of MML-DFE for Spatially Multiplexed MIMO Systems, *IEEE Transactions on Circuits and Systems—II: Express Briefs, vol. 55, no. 7,* July 2008, pp. 705-709.

[20] A.J. -Pacheco, Á. F. -Herrero and J. C. -Quirós, Design and Implementation of a Hardware Module for MIMO Decoding in a 4G Wireless Receiver, *VLSI Design, vol. 2008,* 2008, Article ID 312614, pp. 1-8.

[21] S. Caban, C. Mehlfuhrer, R. Langwieser, A. L. Scholtz, M. Rupp, Vienna MIMO Testbed, *EURASIP Journal on Applied Signal Processing, vol. 2006,* 2006, pp. 1-13, Article ID 54868.

[22] H. Eslami, S. V. Tran, and A. M. Eltawil, Design and Implementation of a Scalable Channel Emulator for Wideband MIMO Systems, *IEEE Transactions on Vehicular Technology, vol. 58, no. 9,* 2009, pp. 4698-4709.

[23] T. Kaiser, A. Bourdoux, M. Rupp, U. Heute, Implementation Aspects and Testbeds for MIMO Systems, *EURASIP Journal on Applied Signal Processing, vol. 2006,* 2006, pp. 1-3, Article ID 69217.

[24] M. W. Numan, M. T. Islam, N. Misran and M. A. M. Ali, A Matrix Factorization Based Channel Estimation Technique for FPGA Implementation of Multiple Antenna System, *International Review of Electrical Engineering*, vol. 5, no. 4, 2010, pp. 1853-1861.

[25] M. W. Numan, M. T. Islam, N. Misran, FPGA-Based Hardware Realization for 4G MIMO Wireless Systems, *Informacije MIDEM Journal of Microelectronics, Electronic Components and Materials*, vol. 40, no. 3, 2010, pp. 191-199.

[26] S. Alamouti, A simple transmit diversity technique for wireless communications, *IEEE Journal on Selected Areas in Communications, vol. 16,* October 1998, pp. 1451-1458.

[27] Tarokh, V., Jafarkhani, H., &Calderbank, A.R. 1999. Space-time block codes from orthogonal designs. *IEEE Transactions on Information Theory*, 45:1456—1467.