Dynamic Characterization of the Power MOSFETs

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Abstract: - The paper proposes an easy extraction path of almost static and dynamic parameters of a power MOSFET based on a laboratory technique that requires only one test circuit. Hard switching the power MOSFET on a resistive load, the gate charge, the forward transconductance, the on-state resistance and the switching times, and the intrinsic capacitances are extracted from the waveforms of the gate voltage, drain voltage, and drain current. The extraction procedure for all these parameters of device is described step by step in the paper. A simple test allows students to evaluate the switching performance of a power MOSFET and to teach the difference between MOSFET technologies comparing the Figure of Merit (FOM) index of devices. This test can be repeated for many MOSFETs and IGBTs to compare their overall switching performance and to observe the device behavior for various operating conditions of the device under test (resistive or inductive loads and different supply voltages, and drive gate currents) and it can be used as an education tool in Power Electronics at its basic level.

Key-Words: - Power MOSFETs, Dynamic Characterization, Figure of Merit.

1 Introduction

Power MOSFETs are produced for different applications like programmable resistors, electronic loads, power amplifiers, linear and switching-mode regulators. Depending of application, the power MOSFETs must operate in saturation region or alternately in linear and blocked regions as on-off switches. Because of that the performance of MOSFET is expressed in term of forward transconductance, on-state resistance, dissipated power or gate charge and the tested device-parameters are different. Many of parameters are inter-related in their effect on MOSFET performance. The switching speed of a MOSFET is in correlation to the gate charge: smaller charge to turn it on means diminishing both the switching times and losses yielding a faster switch and higher efficiency of design will be obtained. To evaluate the performance of the MOSFET for a switching application, the Figure-Of-Merit (FOM) index, is being widely adopted as a prevalent criterion to select the best candidate for a switching application: the device with the lowest FOM index value should have the best performance and lead to the lowest loss for this device in the circuit. This explains why the gate charge and on-state resistance are very important parameter of the MOSFETs in applications as switched-mode power supplies [1]-[3].

The engineering educators are conscious of the fact that the engineering students' persistence is based on little experience or data [4]-[9]. Consequently, in an introductory electronics course as Electronic Devices, the laboratory exercise should be used for motivating students for attending more advanced electronics courses and beginning their research education.

Specific goals for parameter extraction are based on the complexity of the measurement circuit and the minimum number of experimental setup. This statement is true for any application engineer involved in the design process as well as for the students when they want to compare some MOSFETs or to more insight into the power MOSFET behavior. For a basic level model of the power MOSFET, an easy parameter extraction path is desired too before needing to abandon the use of simulation in the design process [10].

Usually, for a power MOSFET, the two important measurement setups are: the dc I_D-V_{GS} characteristics and gate-charge plot for resistive load

switching. To characterize a power MOSFET, an application engineer or a student should be able to complete all measurements and calculations within a minimum time [3].

This paper describes a simple laboratory exercise that allows students to characterize the behavior of a power MOSFET in switching applications and to understanding the FOM concept. This laboratory exercise presents a unique opportunity to examine the intersections between the engineering learning and research education for a junior student in electrical engineering [4].

An advantage of the test presented in this paper is the easy extraction of the dynamic parameters of a power MOSFET. Such simple exercise can be employed to compare device theory with the actual operation of an electronic device, using an effective visual format and promote student understanding of the link between theory and application [8], [9]. It has manifold objectives because the students can learn:

1. Evaluate the device performance and correctly select the devices from a specific application perspective.
2. Identify the knowledge and the sources of information needed to understand the problem.
3. Use the information contained in experimental results to verify the device characteristics given in data sheets.

The paper is organized as follows. Section 2 presents the extraction procedure of the dynamic parameters of interest for a switching application based on power MOSFETs and for evaluation of their switching performance, and the information contained by gate-charge characteristics. In Section 3, an application example of the described procedure and the experimental results are presented and discussed. In order to compare the dynamic performance of MOSFETs, three devices are characterized. Section 4 concludes the paper.

2 Dynamic Characterization of the Power MOSFETs

Dynamic characterization of a power MOSFET requires specific measurement circuits in order to determine the switching times, power losses and gate driving characteristics for specified operating conditions. All these characteristics that define the switching performance of a power MOSFET essentially depend on the internal parameters of the device such as gate threshold voltage ($V_{GS(th)}$), intrinsic capacitances (C_{gs}, C_{ds} and C_{ds}) and gate charge (Q_g) with its components (Q_{gs} and Q_{gd}), minimum gate voltage ($V_{GS(ON)}$) for specified conduction conditions, overdrive gate voltage (V_{GG}), drain-source resistance corresponding to full-conduction resistance ($r_{DS(ON)}$) and forward transconductance (g_{fs}).

For every MOSFET type, a parameter extraction path should be provided using only data sheet information. The parameter values will be less accurate because the data sheet describes the typical devices but the extraction time can be limited to minimum. Some data sheet gate-charge plots are improperly measured and are useless for parameter extraction. Conversely, some parameters, like the drain-source capacitance, are relatively unimportant and can be easily estimated from a data sheet without measurements.

2.1 Parameter Extraction from Switching Waveforms

The power MOSFET is a current-driven device during transitions due to the charging or discharging of capacitances. In actual applications, most drive circuits exhibit a first-order approximation to a constant current where the voltage compliance is determined by ground potential or the drive circuit power-supply voltage. This is one raison for which a circuit with the same topology as that used to obtain the gate-charge plot at manufacturers was implemented here. The duality of the abscissa scale (time and gate charge) was another raison for this choice. Using a bipolar gate-current supplied by the driving circuit for the test ($I_T = \pm 1$ mA), the gate and drain voltages versus gate-charge and time are simultaneously yield. Also, the drain current plot versus time is obtained with the same circuit. Excepting switching times, the extracted parameters are expressed in term of external electrical quantities.

Under constant current drive, the waveforms of Fig. 1 will scale in an direct manner with the gate charge in nanocoulombs corresponding to a test current (I_T) of 1 mA and with the actual time t* in nanoseconds corresponding to actual amplitude of the gate current (I_G). For the actual time t*, each division must be scaled down by the actual gate current in ampers: $x=1/I_G$ [A]. The piece-wise linear approximation of the gate-source and drain-source voltage plots versus gate charge or equivalently versus time because the horizontal scale represents the charge $Q_g=I_T \times t$ are shown in Fig. 1. So, how the desired switching times of power MOSFET are by order of tens of nanoseconds, the actual time

scale allows finding the gate current amplitude needed to drive the devices in specified conditions:

$$I_G = I_T \cdot (t / t^*). \quad (1)$$

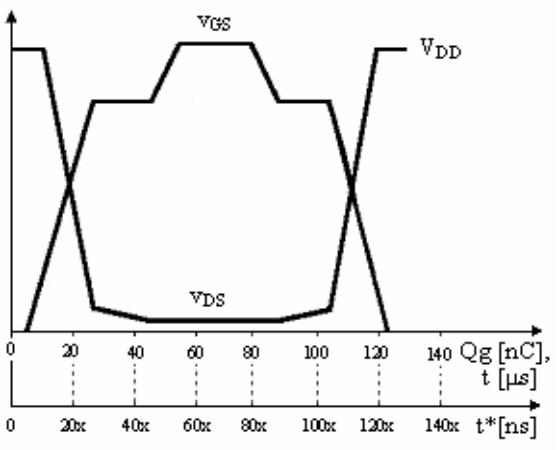

Fig. 1. The piece-wise linear approximation of gate and drain voltage plots versus charge gate and time [11].

Fig. 2 displays the gate and drain voltages, and drain current plots versus time of the tested MOSFET where the instants needed to extract the parameters of the MOSFET were noted as t_0, t_1, t_2, t_3 and t_4 for turn-on and t_5, t_6, t_7 and t_8 for turn-off.

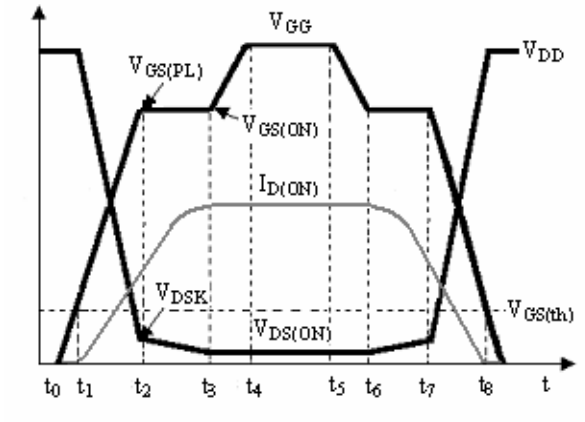

Fig. 2. The gate and drain voltages, and drain current plots versus time.

The following discussion relates the mean parameters of a power MOSFET to the waveforms in Fig. 1 and 2. The discussion begins with the instant t_0 when the positive gate-current is applied and the gate voltage equals zero. This condition corresponds to blocked behavior where the drain current is approximately equal to zero (I_{DSS}) and the drain voltage equals V_{DD}. First of all, the total gate charge Q_g, the gate-source charge Q_{gs} and the gate-drain charge Q_{gd} are directly extracted from the curve of gate-source voltage versus gate charge plot as shown in Fig. 1.

2.1.1 Forward transconductance and on-state resistance

The conduction parameters group the gate threshold voltage ($V_{GS(th)}$ or V_{TH}), the knee gate voltage ($V_{GS(ON)}$), the "dynamic Vsat" (V_{DSK}), the forward or large-signal transconductance (g_{fs}), and the drain-source resistance corresponding to full-conduction resistance or on-state resistance ($r_{DS(ON)}$). The gate threshold voltage can be estimated as the level of the gate voltage at the instant t_1 when the drain current starts to increase and the drain voltage starts to decrease, i.e. $V_{GS(th)} = v_{GS}(t_1)$. The right knee of the gate voltage is the gate voltage $V_{GS(ON)}$ that is $v_{GS}(t_3)$ at which the drain current reaches its maximum. The "dynamic Vsat" can be estimated as $v_{DS}(t_2)$.

Using only the curves of gate and drain voltages, the forward transconductance g_{fs} for the active region operating can be calculated as

$$g_{fs} = \frac{V_{DD} - v_{DS}(t_2)}{R_L\left[v_{GS}(t_2) - V_{GS(th)}\right]}. \quad (2)$$

Alternatively, the curves of gate voltage and drain current yield

$$g_{fs} = \frac{i_D(t_2)}{v_{GS}(t_2) - V_{GS(th)}}. \quad (3)$$

Many of the conduction parameters are inter-related in their effect on performance. For instance, the value of the drain-source resistance $r_{DS(ON)}$ determines the value of the common performance term named Figure of Merit of the device (FOM) as well as the power loss in the conduction state, $P_{D(ON)}$. The value of the parameter $r_{DS(ON)}$ is in the range of some milliohms and some ohms depending on the MOSFET technology, i.e. voltage range and the package [1].

The data sheet shows a typical and a maximum value of $r_{DS(ON)}$ for specified test conditions. Some times, the normalized values of $r_{DS(ON)}$ are given as function only of junction temperature and for a value pair of drain current and gate-source voltage. Other times, a curve family of $r_{DS(ON)}$ as function on I_D and V_{GS} (as family parameter) is offered by MOSFET manufacturers.

The actual value of this parameter can be extracted from the full-conduction region of the drain-voltage curve where the drain voltage has been reached its minimum $V_{DS(ON)}$. This condition corresponds to quasi-linear behavior of device where the drain current is approximately equal to

$I_{D(ON)}$ and the drain voltage equals $I_{D(ON)}$ times $r_{DS(ON)}$ that yields an alternatively path to determine this parameter. Using the switching waveforms of drain voltage and current, the drain-source resistance $r_{DS(ON)}$ can be calculated by means of the formula

$$r_{DS(ON)} = \frac{V_{DS(ON)}}{I_{D(ON)}} = \frac{R_L \cdot V_{DS(ON)}}{V_{DD} - V_{DS(ON)}}. \quad (4)$$

2.1.2 Gate charge and intrinsic capacitances

The most important dynamic characteristics of a power MOSFET are the gate charge and intrinsic capacitances (C_{gs}, C_{gd}, C_{ds}).

The gate-charge characteristic allows us to estimate the performance of MOSFETs and to design their drivers. The data sheet shows a typical gate-charge characteristic for two or more drain currents and a specified drain-source voltage or for two or three drain voltages and a specified drain current [16], [17]. The components of the gate charge and their correlation with the gate and drain voltage waveforms are shown in Fig. 3.

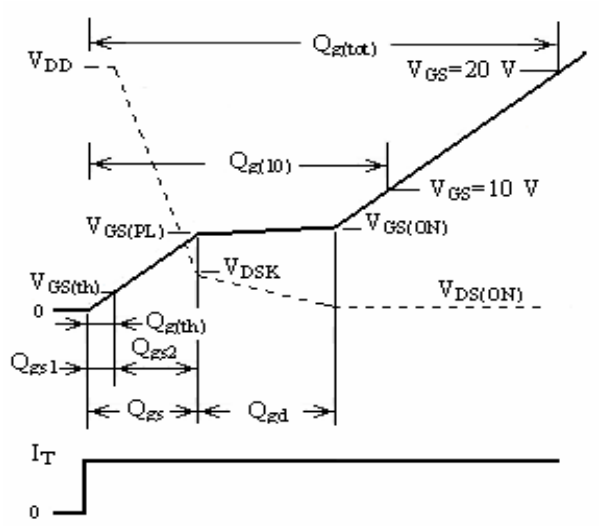

Fig. 3. The components of the gate charge [17].

Referring to Fig. 3, Q_{gs} is the charge from the origin to the first inflection in the curve, with its two components $Q_{g(th)}$ or Q_{gs1} and Q_{gs2}. The charge Q_{gd} or Q_{SW} (switching charge) is the charge from the first to second inflection in the curve (also known as the "Miller" charge), and $Q_{g(tot)}$ is the charge from the origin to the point on the curve at which V_{GS} equals a specified gate drive voltage. Generally, the data sheet indicates $Q_{g(tot)}$ as charge gate corresponding to the rated gate-source voltage (i.e. V_{GSmax}=20 V) and $Q_{g(th)}$ for the minimum value of gate threshold voltage.

The duality of the abscissa scale that is time and gate charge make from a right gate-charge characteristic a powerful tool to estimate the MOSFET performance, to proper design of driver, and to minimize the dissipation on the device. Such characteristics are obtained for a constant current drive of 1 mA for almost power MOSFETs. Fig. 2 highlights the correlation between gate-source voltage, components of the gate charge and switching times.

The charges Q_{gs} and Q_{gd} do not mean what their names seem to imply. Nevertheless they perform the useful function of identifying together the amount of charge necessary to bring the data-sheet-typical MOSFET into full conduction. Since, however, the data sheet values are for typical devices and do not account for the spread of values from MOSFET to MOSFET, proper gate drive design makes use of Q_g to bring about an overcharge condition in the gate.

The total gate charge Q_g and its components Q_{gs} and Q_{gd} can directly be extracted from the curve gate voltage versus gate charge given in Fig. 1 as follows:

$$Q_{gs1} = Q_g(t_1), \quad (5)$$

$$Q_{gs} = Q_g(t_2), \quad (6)$$

$$Q_{gd} = Q_{sw} = Q_g(t_3) - Q_g(t_2). \quad (7)$$

The necessary gate charge to drive the MOSFET into full conduction is the gate charge $Q_g(t_3)$. The overdrive condition means a total gate charge $Q_g(t_4)$. As Fig. 2 shows, a MOSFET must be driven by a fairly high voltage V_{GG}, on the order of 10 volts or on the order of 5 volts for L^2FETs, to ensure maximum saturated drain-current flow. This difference between V_{GG} and $V_{GS(ON)}$ shows that the device is overdriven. For this overdrive, a bigger charge must to be injected into gate than its minimum i.e. $Q_g(t_4)>Q_g(t_3)$. The curve gate voltage versus gate charge directly visualizes the minimum drive energy needed to drive into full conduction a given MOSFET and that one required in the overdrive case.

The intrinsic capacitances of MOSFET are given in data sheets as input capacitances (C_{iss}), output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}) for specified testing conditions and their dependence on drain-source voltage. The capacitance values of a power MOSFET are determined by the structure of the MOSFET technology and decrease over a range of increasing drain-source voltage, especially the output and reverse transfer capacitances. These capacitances are independent of temperature, so MOSFET switching speed is also insensitive to temperature (except for a minor effect related to the threshold voltage

changing with temperature).

The reverse transfer capacitance, often referred to as the "Miller" capacitance, is one of the major parameters affecting voltage rise and fall times during switching. It also affects the turn-off delay time. Gate charge values reflect charge stored on the inter-terminal capacitances described earlier. Gate charge is often used for designing gate drive circuitry since it takes into account the changes in capacitance with changes in voltage during a switching transient [10], [11].

The capacitances C_{gs} and C_{gd} with its two asymptotical values C_{gd1} at $V_{DS}=V_{DD}$ and C_{gd2} at $V_{DS(ON)}$ shown in Fig. 4 can be extracted using the gate and drain voltage plots given in Fig. 1. The inverse slope increasing from $v_{GS}=0$ V to $v_{GS}=V_{GS(th)}$ represents the input capacitance value denoted C_{in1},

$$C_{in1} = C_{gs} + C_{gd1}. \quad (8)$$

The inverse slope above the flat ''Miller effect'' region represents the input capacitance value denoted C_{in2} where

$$C_{in2} = C_{gs} + C_{gd2} \quad (9)$$

with

$$C_{gd2} = C_{gd1}\left(1 + g_{fs} \cdot R_L\right). \quad (10)$$

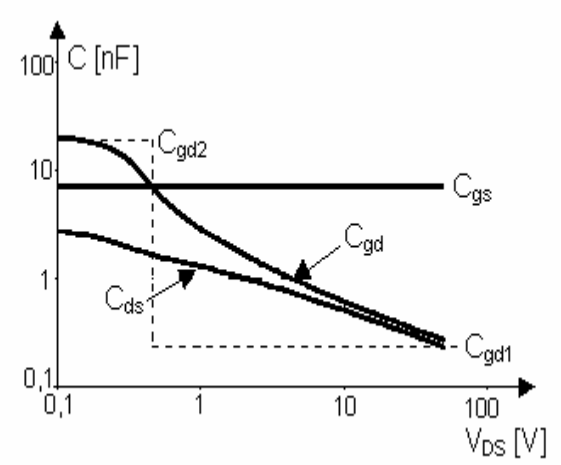

Fig. 4. The power MOSFET capacitances versus drain voltage.

Some power MOSFETs have a really plateau region where $v_{GS}(t_2)=v_{GS}(t_3)$ while others not. In the second case, the capacitance C_{in2} can be directly extracted from the gate-voltage plot. For both the cases, the capacitance C_{in2} can be extracted from the drain-voltage plot, which is correlated with the gate-charge plot as follows:

- At t_2, after the operating point traversed the active region, the drain voltage has been decreased until V_{DSK}. During active region traversing, the gate-drain capacitance increased from its minimum C_{gd1} to its maximum C_{gd2}.
- As v_{GS} progresses from $v_{GS}(t_2)$ to $v_{GS}(t_3)$, i_D reaches its maximum $I_{D(ON)}$ and v_{DS} reaches its minimum $V_{DS(ON)}$. So, the input capacitance C_{in2} can be estimated as

$$C_{in2} = \frac{Q_{gd}}{V_{DSK} - V_{DS(ON)}}. \quad (11)$$

Determining the forward transconductance g_{fs} and capacitances C_{in1} and C_{in2}, the intrinsic capacitances C_{gs} and C_{gd} with its asymptotical values C_{gd1} and C_{gd2} can be estimated.

2.1.3 Switching times

Under constant current drive and resistive load switching with load rated at maximum drain current, the curves of Fig. 1 and 2 directly visualize the switching time components during the turn-on and turn-off transitions. The switching times and their components are measured in the normal manner that is involving the 10% and 90% points of the drain voltage waveforms or the drain current waveforms as it is shown in Fig. 5.

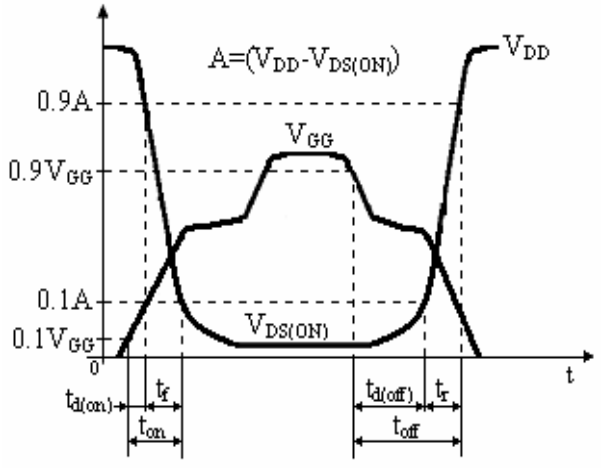

Fig. 5. The drain and gate voltage plot portions during turn-on and turn-off transitions and switching times of power MOSFET.

Now, the two mean components of power loss on the MOSFET namely the power loss in the conduction state (conduction losses), P_{ON}, and the power loss during switching forward and reverse transitions (switching losses), P_{SW}, can be estimated. For a switching pulse-width modulation (PWM) application where the power MOSFET will be switched on a resistive load at constant frequency f_S, the power losses can be estimated as

$$P_{ON} = f_S \cdot r_{DS(on)} \cdot I^2_{D(ON)} \cdot \left(t_p - t_{on}\right) \quad (12)$$

and

$$P_{SW} \cong (f_S / 6) \cdot V_{DD} \cdot I_{D(ON)} \cdot (t_r + t_f). \quad (13)$$

In (12), t_p denotes the duration of the driving current pulse.

2.2 Switching Performance

Using device data sheet values and measured gate-charge characteristics, many design parameters and components can be compared to achieve a design with the optimal combination of efficiency and cost [1], [2], [11]-[16]. In order to compare two or many power MOSFETs, the minimum drive energy can be used as well as so-called Figure-Of-Merit (FOM) of device.

The curve gate voltage versus gate charge directly vizualises the minimum drive energy needed to drive into full conduction a given MOSFET ($W_{drive,min}$), and that one required in the overdrive case ($W_{overdrive}$):

$$W_{drive,min} = Q_g(t_3) \cdot V_{GS(ON)} \quad (14)$$

and

$$W_{overdrive} = Q_g(t_4) \cdot V_{GG}. \quad (15)$$

The gate current amplitude needed to drive the devices in specified conditions can be found using (1). With these data, the gate driver can be easily designed or chosen.

The FOM index is a measure of a MOSFET's overall performance for switching. The product of the on-state resistance, $r_{DS(ON)}$, and total gate charge, $Q_{g(tot)}$, has been used as the figure of merit (FOM) for power MOSFETs for years:

$$FOM_1 = r_{DS(ON)} \cdot Q_{g(tot)}. \quad (16)$$

The FOM index represents how good one fabrication process is compared to another. For a given MOSFET technology, $r_{DS(on)}$ and $Q_{g(tot)}$ are opposite to each other. A MOSFET with a lower on-state resistance has a higher gate charge and vice versa; the lower the FOM index value, the better the MOSFET and two MOSFETs with the same value would perform the same in a given application [1].

The definition (16) is not consistently used. Both $r_{DS(ON)}$ and $Q_{g(tot)}$ are controlled by the gate-source voltage and they are also influenced by the junction temperature. Moreover, $r_{DS(ON)}$ is controlled by the drain current and $Q_{g(tot)}$ by drain-source voltage. A properly comparison of FOMs is only possible if made under the same conditions that depend on the circuit requirements [1]:

$$FOM_1(V_{GS}, V_{DS}, I_D) = r_{DS(ON)}(V_{GS}, I_D) \cdot Q_{g(tot)}(V_{GS}, V_{DS}, I_D). \quad (17)$$

So, an actually FOM index is one that corresponds to actually conditions imposed by MOSFET application and this value can be done only by the MOSFET parameters obtained through measurement or simulation. This is a raison that motivated the development of a simple test circuit and an extraction procedure of the parameters of interest of a power MOSFET. Shortly, using the information in switching waveforms of a power MOSFET on a resistive load, actually gate charge characteristic, on-state resistance, internal capacitances and switching times can be measured in specified conditions [11].

Requirements of more and more efficiently power supplies for actual computers demand advanced power MOSFETs with ultra-low on-state resistance and lower gate charge able to minimize the losses. In these circumstances, the older FOM_1 of switches proved to be inefficient to characterize the performance of the newer devices.

In [12], it was proposes the use of the more accurate FOM for power devices, which is the gate-drain charge times MOSFET on-resistance:

$$FOM_2 = r_{DS(ON)} \cdot Q_{gd}. \quad (18)$$

This definition of FOM index is widely accepted and widely used too for power devices. As it was demonstrated, for a given constant new FOM_2, the power dissipation on the high side MOSFET will vary significantly. Using this new version of power MOSFET figure of merit and constant-power dissipation curves, designers can calculate the optimum combination of factors to select a device for a power supply application and minimize its dissipation [12].

In last ten years, new versions of FOM for power MOSFET have been proposed as response to the challenge providing more performance in VRM and in specially for DC-DC synchronous buck converter. For this converter type, two different types of MOSFETs are used. Thus the performance of the high side MOSFET is characterized differently of that of the low side MOSFET owing the different operating conditions of the two devices [13]. A new power semiconductor device figure of merit (FOM)-power density FOM-is proposed in [14], with consideration of power device conduction and switching losses, thermal characteristics, and package. In [15], an investigation of a new FOM based on a more accurate loss model, which includes the factor of Q_{gs2}, the gate-driving voltage and the packaging parasitics is presented. Concluding this part of discussion, different application requirements dictate the use of different products and better characterization of their performance. Nevertheless, regardless of which

figure of merit (older or newer) is used to select the switches for a switching application, the on-state resistance and gate charge characteristic of device must be known. The new lateral MOSEFT technology offers a 3× improvement over the state of the art trench MOSFETs that is a viable solution for the next-generation, multimegahertz, high-density dc/dc converters for future CPU cores and many other high-performance power management applications [3].

3 Test Setup and Experimental Results

This laboratory exercise aims to help the students to properly compare many candidates for an switching application MOSFETs using their most important dynamic parameters and switching performance expressed in term of FOM index denoted as FOM_1 and FOM_2. First of all, the most important characteristics and parameters of MOSFETs to be compared are extracted from data sheets. Then gate-charge characteristic and switching waveforms are measured and captured. To make possible a comparison of switching performance and different technologies, the test has to be repeated for several samples that operate in the same conditions.

The block-diagram of the test setup is shown in Fig. 6. The current-generator block consists of a pulse generator and a comparator with two paralleled OTAs. The pulse generator is set for 1.2 ms pulse duration and approximately 12 ms repetition rate (about 0.1 duty cycle) to capture the quasi-plateau region of the gate voltage plot. The supply voltages of the OTA comparator are set to clamp the gate voltage at ± 10 V [11].

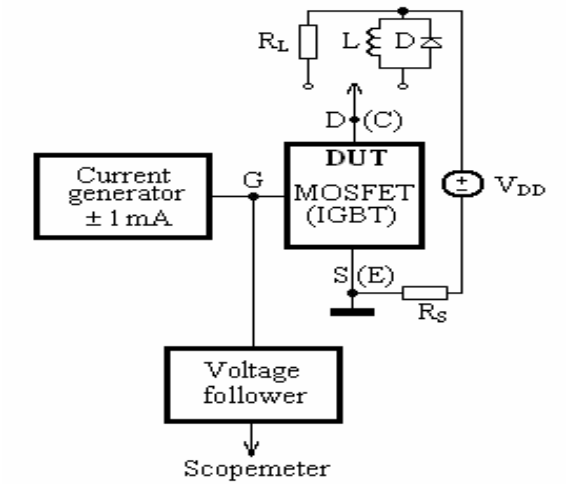

Fig. 6. Block-diagram of the test setup.

The scopemeter allows capturing all the waveforms necessary to be processed. The drain voltage and the drain current are directly displayed. The resistance R_S of 1 ohm acts as drain current sensor. Only for the gate voltage waveform is used a unity gain follower built with a high input impedance operational amplifier. With minor arrangements, the testing parameters as gate-current amplitude, maximum gate-source and drain-source voltages, and full-conduction drain current can be set at desired values.

In order to illustrate the exposed procedure to extract the dynamic parameters of the power MOSFETs, three samples of 100V single N-Channel HEXFET Power MOSFET in a TO-220AB package namely IRF510 (Id=5.6 A, $r_{DS(ON)}$=0.54 Ohm) and IRF530 (Id=14 A, $r_{DS(ON)}$=0.16 Ohm) were tested for $I_T = \pm 1$ mA ($I_{T(on)}=I_{T(off)}$), V_{DD}=20V, V_{GG}= 10 V and $I_D \cong 1$ A (resistive load). In this part of the paper, the most important results obtained by testing these devices are presented and discussed.

The graphs in Fig. 7, 8 and 9 represent the gate-source and drain-source voltage plots versus time in microseconds or equivalently gate charge in nanocoulombs during turn-on transition while those in Fig. 10, 11 and 12 are the homonym curves during turn-off transition of the same samples.

The gate charge and its components for the three MOSFET samples extracted from the gate voltage waveforms in Fig. 7, 8 and 9, because the graph $v_{GS}=f(t)$ is directly transformed into the gate charge characteristic by grading the abscissa scale in nanocoulombs. All the gate threshold voltages measured during the experiment are in the range indicated by manufacturers for all samples. The gate voltage waveforms for IRF510 samples exhibit a quasi-flat plateau region due the little difference between $V_{GS(PL)}$ and $V_{GS(ON)}$.

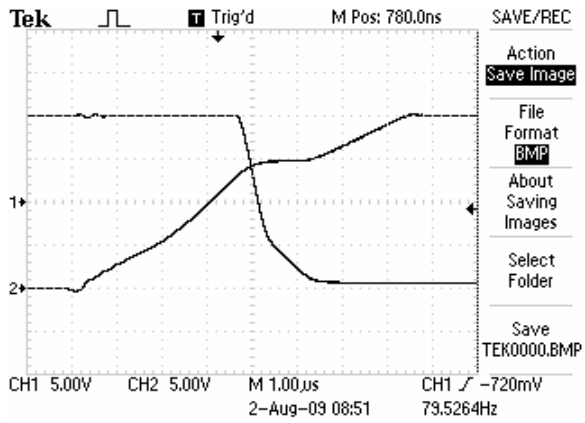

Fig. 7. Gate and drain voltage waveforms for IRF510(1) during turn-on transition.

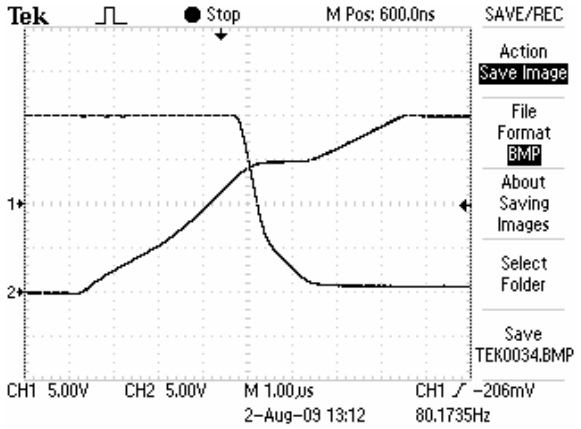

Fig. 8. The gate and drain voltage waveforms for IRF510(2) during turn-on transition.

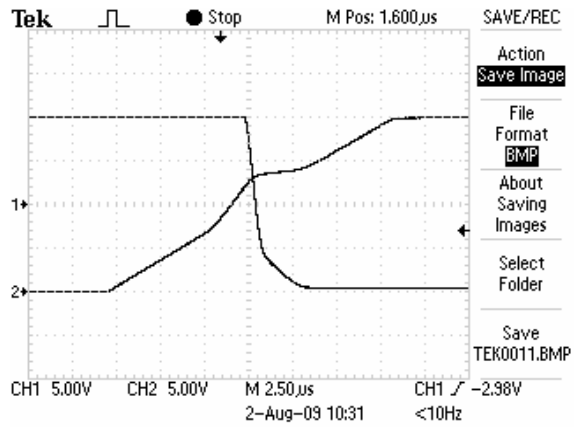

Fig. 9. The gate and drain voltage waveforms for IRF530 during turn-on transition.

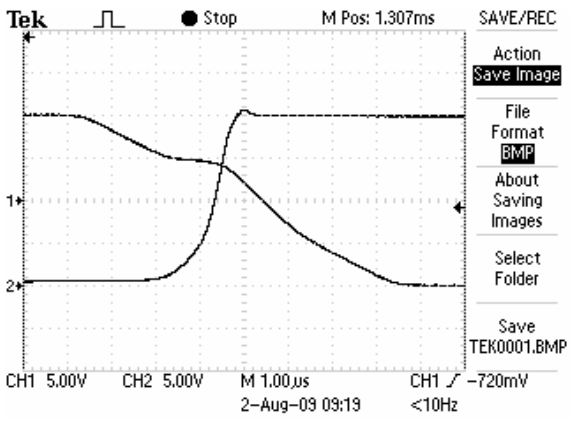

Fig. 10. Gate and drain voltage waveforms for IRF510(1) during turn-off transition.

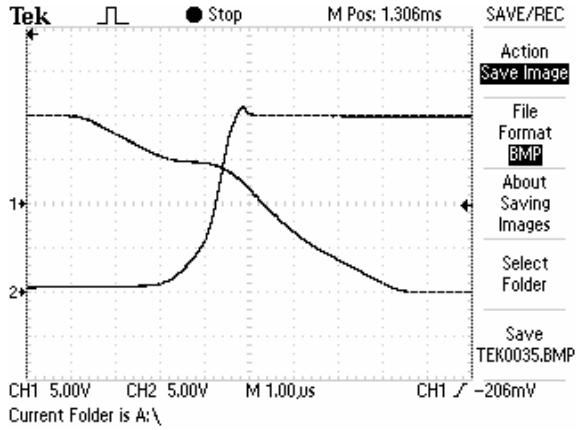

Fig. 11. Gate and drain voltage waveforms for IRF510(2) during turn-off transition.

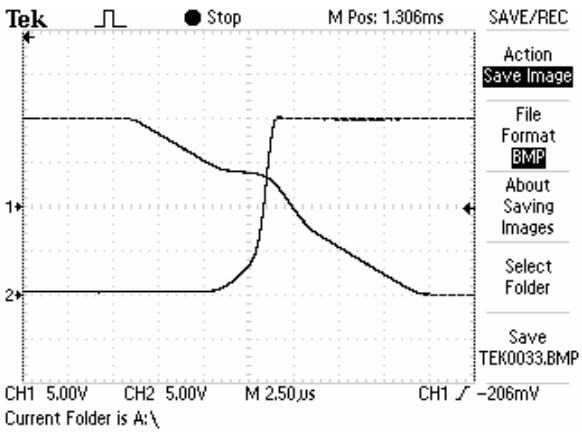

Fig. 12. Gate and drain voltage waveforms for IRF530 during turn-off transition.

The drain voltage waveforms captured during this laboratory exercise shown that a persistent "dynamic Vsat" exists even at slow switching speeds and the "dynamic Vsat" curves are symmetrical during the low-drain-voltage portion of the turn-on and turn-off portion.

The switching times and their components can be extracted from the gate and drain voltage waveforms or drain voltage and current waveforms during the turn-on and turn-off transitions. The drain voltage and current waveforms of IRF530 sample are given in Fig. 13 and 14 as example. These graphs as well as the homonym graphs of IRF510 samples highlight the well-known behavior of the device switched on a resistive load that is a simultaneous variation of the drain current and drain-source voltage during switching transitions.

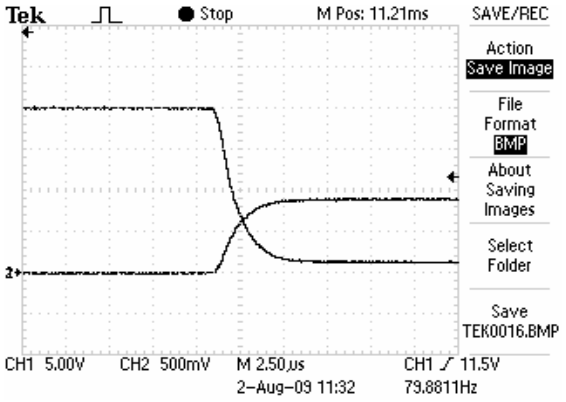

Fig. 14. Drain voltage and current waveforms for IRF530 during turn-on transition.

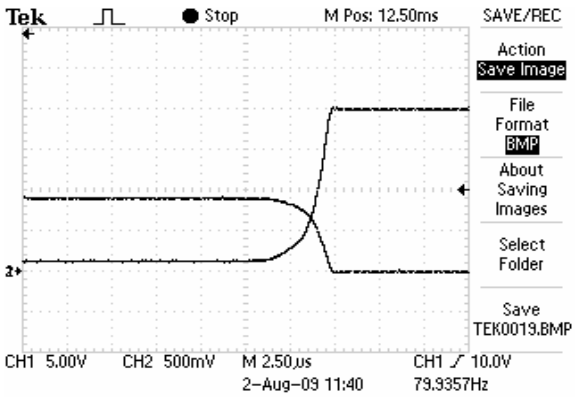

Fig. 15. Drain voltage and current waveforms for IRF530 during turn-off transition.

The aggregation of the most important experimental results obtained by testing the three samples of power MOSFETs for $I_T = \pm 1$ mA, $V_{GS} = \pm 10$ V, $V_{DD} = 20$ V, and $I_D \cong 1$ A, in term of electrical quantities of interest and dynamic parameters, and switching performance extracted from the switching waveforms and is given in Table 1. The two samples of power MOSFET code IRF510 are denoted IRF510(1) and IRF510(2).

Now, the measured values of the dynamic parameters can be compared with those extracted from data sheets. Taking into account the testing conditions for the samples considered here, the comparison result shows little differences between them. Also, it can be seen in experiment that the MOSFET with a lower on-state resistance has a higher gate charge and vice versa. In this test, the MOSFET code IRF530 could be considered the better MOSFET owing its lower the FOM index value in both versions FOM_1 and FOM_2.

Although the devices have been driven from a current generator whose $I_{T(ON)}=I_{T(OFF)}$, the rise and fall times are slowly different. With an actual current drive I_G of 1 A, the switching times will be scaled down by thousand times.

Table 1. Electrical quantities of interest and dynamic parameters and switching performance of tested devices.

Parameter	IRF510(1)	IRF510(2)	IRF530
$V_{GS(th)}$ [V]	3	2.8	2
$V_{GS(PL)}$ [V]	4.6	4.8	3.5
$V_{GS(ON)}$ [V]	4.8	5	4
V_{DSK} [V]	5.2	5.4	4.4
$V_{DS(ON)}$ [V]	0.43	0.42	0.109
$r_{DS(ON)}$ [Ω]	0.452	0.446	0.189
$Q_{g(tot)}$ [nC] (V_{GS}=10 V)	4.5	4.35	9
Q_{gs1} [nC]	0.62	0.53	1
Q_{gs} [nC]	1.2	1.1	1.5
Q_{gd} [nC]	1.4	1.15	2
FOM_1 [Ω·nC]	2.03	1.94	1.7
FOM_2 [Ω·nC]	0.63	0.51	0.378
$t_{d(on)}$ [µs]	0.17	0.18	0.26
t_r [µs]	1.25	1.27	2.04
t_{on} [µs]	1.42	1.45	2.3
$t_{d(off)}$ [µs]	0.32	0.36	0.88
t_f [µs]	1.31	1.14	1.88
t_{off}[µs]	1.62	1.5	2.76

4 Conclusion

Theoretically, all the parameters and dynamic characteristics of the power MOSFET can be extracted and evaluate from the simulations of the test circuit given in Fig. 6 but only the on-state resistance value obtained as simulation result is very closed to the typical value given in data sheet and that measured regardless of the level of MOSFET model. This means that the simulated characteristics could be used to evaluate the switching performance of a power MOSFET only if an appropriate MOSFET model is available.

The laboratory exercise described in this paper presents a unique opportunity to examine the intersections between the engineering learning and research education for a junior student in electrical engineering. The differences between the parameter values of a device as power MOSFET given by various information sources demonstrate the importance of experimentally verification and

validation of a model and design solution and also can open a way to research for many students. Thus, the students teach to define the problem clearly and precisely, to generate criteria for evaluating the quality of a solution, and to identify all needs to be addressed by the design problem. Such learning experiences provide one of the most effective ways to actively engage the students in the learning process. The test presented in this paper can be repeated for many MOSFETs and IGBTs to compare their switching performance because both device types require the application of a positive gate voltage signal in order to turn-on the device.

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