# Using Circuit Simulators to Sensitivity-Factor Analysis in Analog Circuits

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*Abstract:* - In this paper, a procedure to calculate the sensitivity factors of the quiescent drain current of a field-effect transistor operating in the active region is presented. This one can be applied in conjunction with a general-purpose circuit simulator for bias circuits with bipolar junction transistors or field-effect transistors. We showed that the sensitivity factors of the quiescent drain current can be calculated by repeated simulations of the bias circuit modified according to the change of a parameter value. How to apply the proposed procedure is illustrated on the two common bias circuits for which comparatively studies are performed. Such a procedure based on a circuit simulator allows the students to verify and, if necessary, modify the bias circuit design on desired direction and rapidly test it.

*Key-Words:* - Sensitivity factor analysis, Bias circuits, FET.

## 1 Introduction

Student understanding of the link between theory and application has always been a critical objective in electronics education. During an introductory course on analog and digital electronics, software is one of the main teaching tools. The laboratory and home works are designed to be taken concurrently with the lecture course and to reinforce lecture concepts with practical application. Studies or small designs of simple circuits based on a circuit simulator allow students an in-depth understanding of the device and circuit operation, and link between transistor theory and application [1] – [5].

In the practical design of transistor circuits, the quiescent operating point Q is carefully established to ensure that the transistor will operate over a specified range, that linearity will be achieved and that maximum allowable power of device will not be exceeded. Once a design has been completed, it is necessary to check for quiescent point variations due to temperature changes and possible unit-to-unit parameter variations. These variations must be kept within acceptable limits as set by the specifications. Among the independent parameters which can cause a shift of the Q point of a field-effect transistor (FET) are the following: the wide variation in the transconductance parameter β and threshold voltage for a particular transistor type; variation in the afore mentioned parameters due to their dependence on temperature; variations in the supply voltages due to imperfect regulation; variations in the circuit resistances due to tolerance and/or temperature effects [6], [7].

Some of these parameters, e.g. temperature effects, are of importance for all designs while others, e.g. resistor tolerance and FET parameter variations, are more important when we are concerned with a production run of a number of identical amplifiers or large analog circuits.

## 2 Problem Formulation

In a FET, the threshold voltage and the transconductance parameter are functions of temperature. These parameters also vary somewhat from unit to unit as a result of differences in manufacturing process. This paper presents a way to find out the sensitivity factors of the drain current in bias circuits with FETs. In the next section, we discuss several methods to calculate the sensitivity factors of the drain current with rapport with two basic parameters of FET using a generalized bias circuit that controls the biasing variation in the devices and covers all types of *n*-channel devices (JFET, enhancement- and depletion-mode MOSFET). Although *n*-channel FETs are used throughout, the same technique can be used to bias the *p*-channel type.

### 2.1 Four-resistor bias circuit

We consider a bias circuit widely used to control the bias variation in the FETs based on the DC negative feedback on drain current, which schematic diagram is shown in Fig. 1. Such a voltage-divider biasing also known as four-resistor bias circuit is used to biasing both transistor types: BJTs and FETs. The symbol *n*-channel written inside of the circle means any FET with *n* channel, i.e. NJFET, enhancement-mode NMOSFET and depletion-mode NMOSFET. This bias configuration can ensure the bias for all *n*-channel FETs and contents even the

particular bias topologies used for JFET and depletion-mode MOSFET ($R_2 = \infty$). The resistance values and the supply voltage ensure a specified quiescent operating point in the active region for each device depending on its particular transfer characteristic curve. So, such a circuit must ensure a quiescent gate-to-source voltage $V_{GSQ}$ with polarity and value adequate to the FET type as follows:

- for a NJFET and depletion-mode NMOSFET operating into depletion mode, $V_{Th} < V_{GSQ} \leq 0$;
- for an enhancement-mode NMOSFET, $V_{th} < V_{GSQ} < V_{GSmax}$;
- for a depletion-mode NMOSFET operating into enhancement mode, $0 \leq V_{GSQ} < V_{GSmax}$.

The value of voltage $V_{GSQ}$ depends on the specified quiescent point of FET.

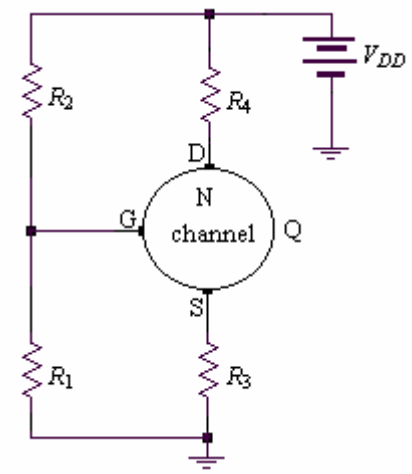


Fig. 1. The schematic diagram of four-resistor bias circuit.

### 2.1.1 Biasing the JFET

We consider the bias circuit in Fig. 1. In order that this topology to operate as a small-signal amplifier, we wish to bias this stage at a prescribed nominal value of quiescent drain-to-source voltage $V_{DSQ}$. The variation of the $Q$ point with JFET-parameter variation is to remain within prescribed limits. To accomplish this, we must bias the JFET to ensure that the variation of quiescent drain current falls within prescribed limits since changes in $I_{DQ}$ are reflected directly in $V_{DSQ}$.

The traditionally way to design such a circuit is based on the worst-case transfer characteristic curves of each particular JFET type utilizing a graphical procedure. These transfer curves are drawn assuming operation in the saturation or active region and show the worst-case variation of drain current as a function of gate-to-source voltage. For this operating mode, (1) or equivalently (2) applies:

$$I_D = I_{DSS}\left(1 - \left(V_{GS} / V_{th}\right)\right)^2, \quad (1)$$

$$I_D = \beta\left(V_{GS} - V_{th}\right)^2. \quad (2)$$

In the above equations, $I_{DSS}$ denotes the nominal saturation current and $\beta$ is the transconductance parameter: $\beta = I_{DSS}/(V_{th})^2$. The equivalent form (2) of the drain current (1) allows us to unify the description of all FET types in the active region. So, the worst-case transfer curves give us the worst-case values of the JFET parameters: $I_{DSSmin}$, respectively $\beta_{min}$ and $I_{DSSmax}$, respectively $\beta_{max}$, and $V_{thmin}$ and $V_{thmin}$. These worst-case values of the JFET parameters are provided also by the manufacturer for each particular FET type.

The bias circuit given in Fig. 2 is the Thevenin equivalent circuit of the generalized bias circuit in Fig. 1, where $V_{GG} = [R_1/(R_1+R_2)]V_{DD}$ and $R_G = (R_1R_2)/(R_1+R_2)$. Since no DC current can flow into the gate of the FET, no DC current flows in $R_G$ and the DC gate-to-source voltage is

$$V_{GS} = V_{GG} - I_D R_3, \quad (3a)$$

where

$$V_{GG} = [R_1/(R_1+R_2)]V_{DD}. \quad (3b)$$

The drain current is given by (1) or (2) and the drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D (R_3+R_4). \quad (4)$$

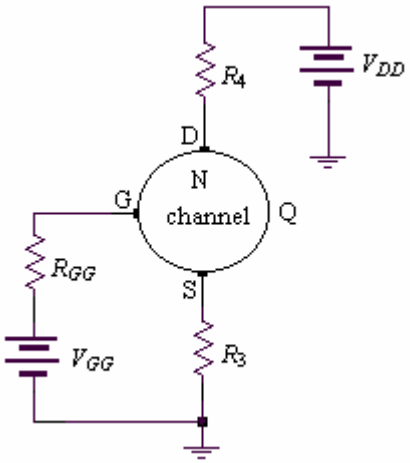


Fig. 2. The Thevenin equivalent circuit of the circuit given in Fig. 1.

The graphical design procedure of the stage is based on the worst-case transfer curves of a JFET and it is described in all electronics textbooks. Briefly, it is assumed that the nominal quiescent operating point ($I_{DQ}$ and $V_{DSQ}$) and supply voltage $V_{DD}$ are known. Also, the maximum allowable deviation from this nominal value

$\Delta I_{DQ}$ is specified. Two worst-case operating points can be fixed on the transfer characteristics: $Q_{max}$ corresponding to $I_{DQ,,max}$ and $V_{GS1}$ and $Q_{min}$ corresponding to $I_{DQ,min}$ and $V_{GS2}$. The straight line representing equation (3) must pass through the points $Q_{max}$ and $Q_{min}$. The intersection of this line and $V_{GS}$ axis yields $V_{GG}$, while the slope of line is -1/$R_3$. So,

$$R_3 = \left| V_{GS1}\text{-}V_{GS2} \right| / (I_{DQ,max}\text{-}I_{DQ,min}). \quad (5)$$

Then, the resistance $R_4$ is calculated:

$$R_4 = (V_{DD}\text{-}V_{DSQ})/I_{DQ}\text{-}R_3. \quad (6)$$

Choosing the current that flows through the resistors $R_1$ and $R_2$, and $V_{GG}$ being known, the last resistances are calculated and the design of the bias circuit is now complete.

### 2.1.2 Biasing the MOSFET

The bias circuit in Fig. 1 works in the same fashion with JFET or MOSFET. The worst-case values of MOSFET parameters are given as $k_{max} = \beta_{max}$, $k_{min} = \beta_{min}$, and $V_{thmax}$ and $V_{thmin}$. When the MOSFET is operating in the active region, the worst-case equations of the drain current are:

$$I_D = \beta_{max} (V_{GS}\text{-}V_{th,min})^2. \quad (7)$$

$$I_D = \beta_{min} (V_{GS}\text{-}V_{th,max})^2. \quad (8)$$

Equation (7) yields the largest $I_D$ for a given value of $V_{GS}$, while (8) produces the smallest $I_D$. The design of the bias circuit is similar with that of JFET.

### 2.1.3 Drain current expression

Combining (2) and (3), we obtain a second-degree equation in unknown $I_D$:

$$aI_D^2 + bI_D + c = 0 \quad (9)$$

where:

$$a = \beta R_3^2;\ b = 2\beta R_3^2 (V_{th} - V_{GG}) - 1;\ c = \beta\left(V_{GG}^2 + V_{th}^2\right).$$

Equation (9) has two solutions

$$I_{D1,2} = \frac{1}{2\beta R_3^2} \times \left[ \begin{array}{l} 1 + 2\beta R_3 (V_{GG} - V_{th}) \\ \pm \sqrt{1 + 4\beta R_3 (V_{GG} - V_{th}) - 8\beta^2 R_3^2 V_{GG} V_{th}} \end{array} \right], \quad (10)$$

if the following inequality is accomplished:

$$1 + 4\beta R_3 (V_{GG} - V_{th}) - 8\beta^2 R_3^2 V_{GG} V_{th} \rangle 0. \quad (11)$$

Among these two above solutions only one accepted solution is the quiescent drain current $I_{DQ}$ namely that for which

$$V_{GG} - I_{DQ} R_3 \rangle V_{th}, \quad (12)$$

for all types of *n*-channel FET.

Now, we suppose that the worst-case of the FET parameters are known. The design problem of the bias circuit knows some aspects such as the following:

1. The nominal quiescent operating point and the maximum variation of drain current being specified or for a given performance specification such as the gain of the small-signal amplifier, it must find out the values of the resistances $R_1$, $R_2$, $R_3$ and $R_4$.
2. For given resistances $R_1$, $R_2$, $R_3$ and $R_4$, it must find out the maximum possible variation of $I_{DQ}$ and $V_{DSQ}$ taking into account the wide spread of the parameter values of FET and/or the temperature variations or voltage supply deviations.

The solution of the former formulation of design problem can be found using either a graphical or an analytical procedure.

We consider the nominal quiescent operating point given by $I_{DQ}$, $V_{DSQ}$, and the maximum variation of drain current specified as $I_{DQmax}$ and $I_{DQmin}$. Firstly, we calculate the gate-to-source voltages corresponding to the variation limits of drain current:

$$V_{GS1} = V_{thmin} + (I_{DQmax}/\beta_{max})^{1/2}, \quad (13)$$

$$V_{GS2} = V_{thmax} + (I_{DQmin}/\beta_{min})^{1/2}. \quad (14)$$

Next, the Thevenin voltage $V_{GG}$ and the resistance $R_3$ can be calculated:

$$V_{GG} = (V_{GS1} I_{DQmin}\text{-}V_{GS2} I_{DQmax})/(I_{DQmin}\text{-}I_{DQmax}), \quad (15)$$

$$R_3 = \left| (V_{GS1}\text{-}V_{GS2}) \right| / (I_{DQ,max}\text{-}I_{DQ,min}). \quad (16)$$

Then, the resistance $R_4$ is found:

$$R_4 = (V_{DD}\text{-}V_{DSQ})/I_{DQ}\text{-}R_3. \quad (17)$$

Choosing the current that flows through the resistors $R_1$ and $R_2$, the last resistances are calculated and the design of the bias circuit is now complete.

The second aspect of design problem is related to so-called stability-factor analysis often used in engineering practice.

## 3 Sensitivity-Factor Analysis

In the circuit in Fig. 1, any increase in drain current causes an increase in the source voltage, and therefore the gate-to-source voltage becomes more negative. This tends to reduce the current, thereby reducing the current increase which started the cycle. This sequence of events describes a negative feedback and resistor $R_2$ is responsible of stabilizing influence of the bias circuit.

Briefly stated, the problem of the stability-factor analysis is as follows: Given a physical variable (in our case, $I_{DQ}$), what change will it undergo when the variables on which it depends (in our case, $V_{th}$, β, $V_{DD}$ etc.) change by prescribed (usually small) amounts? This type of analysis goes under various names, e.g., sensitivity analysis, variability analysis, and stability/sensitivity factor analysis. All these methods are based on assumption that, for small changes, the variable of interest is a linear function of the other variables and can be expressed in the form of a total differential. For our case, we write the quiescent drain current

$$I_{DQ} = I_{DQ}(\beta, V_{th}, V_{DD}). \tag{18}$$

Then the total differential is

$$dI_{DQ} = \frac{\partial I_{DQ}}{\partial \beta} d\beta + \frac{\partial I_{DQ}}{\partial V_{th}} dV_{th} + \frac{\partial I_{DQ}}{\partial V_{DD}} dV_{DD}. \tag{19}$$

Formally, likewise for a BJT, if the changes in the independent variables β, $V_{th}$, and $V_{DD}$ are small, we could define here three sensitivity factors of $I_{DQ}$ as follows:

$$S_{\beta} = \frac{\Delta I_{DQ}}{\Delta \beta} \cong \frac{\partial I_{DQ}}{\partial \beta}; \tag{20a}$$

$$S_{V_{th}} = \frac{\Delta I_{DQ}}{\Delta V_{th}} \cong \frac{\partial I_{DQ}}{\partial V_{th}}; \tag{20b}$$

$$S_{V_{DD}} = \frac{\Delta I_{DQ}}{\Delta V_{DD}} \cong \frac{\partial I_{DQ}}{\partial V_{DD}}. \tag{20c}$$

Now, we can write that the total change $\Delta I_{DQ}$ in the quiescent drain current is proportional to the changes in each of the independent variables and to their sensitivity factors:

$$\Delta I_{DQ} = S_{\beta} \Delta \beta + S_{V_{th}} \Delta V_{th} + S_{V_{DD}} \Delta V_{DD}. \tag{21}$$

Unlike the quiescent collector current of a BJT, $I_{DQ}$ is a strongly nonlinear function on all three variables, i.e. β, $V_{th}$ and $V_{DD}$, as shows the equation (10). Moreover, large changes of the independent variables are involved. Consequently, the procedure that applies to BJT to calculate the sensitivity factors cannot be applied to a bias circuit of a FET. However, in such a case, for given variation limits of β, $V_{th}$ and $V_{DD}$, the total change in the quiescent drain current must be obtained directly, i.e.

$$\begin{aligned} \Delta I_{DQ} = {} & I_{DQ}(\beta_{max}, V_{th\,min}, V_{DD\,max}) \\ & - I_{DQ}(\beta_{min}, V_{th\,max}, V_{DD\,min}) \end{aligned}. \tag{22}$$

In (22), the independent variables are chosen to maximize $\Delta I_{DQ}$ in order to provide a worst-case condition. Using (22) in conjunction with (4), the total change in the quiescent drain-to-source voltage results:

$$\Delta V_{DSQ} = \Delta V_{DD} - \Delta I_{DQ}(R_3 + R_4). \tag{23}$$

Such a procedure can be easily implemented by help of a computational package as Mathematica, MathCAD, MatLab, etc.

To find out each sensitivity factor of the quiescent drain current, we can employ a circuit simulator to calculate the actual increment of the quiescent drain current caused by the variation of only one independent variable. This procedure will by described in the following.

Suppose a given bias circuit as that in Fig. 1. The circuit consists of a JFET_N sample, for which the $\beta_0$ and $V_{th0}$ were measured at ambient temperature T=27°C. Let be $V_{DD}$ the nominal voltage value of the supply. Let be JFET_N_e0 the simplified user model constructed utilizing only two parameter model of JFET, i.e. $\beta_0$ and $V_{th0}$, the rest of model parameter have the same values for all user models. Three other user models named in order JFET_N_b1 with the parameters $\beta_1$ and $V_{th0}$, JFET_N_t1 with the parameters $\beta_0$ and $V_{th1}$, and JFET_N_e with the parameters $\beta_1$ and $V_{th1}$, respectively, will be constructed too.

The three actual increments of the quiescent drain current corresponding to the three independent variables are denoted and calculated as follows:

- For a change in the transconductance parameter value, $\Delta\beta=\beta_1-\beta_0$,

$$\Delta I_{D,\beta} = I_{DQ}(\beta_1, V_{th0}, V_{DD}) - I_{DQ}(\beta_0, V_{th0}, V_{DD}). \tag{24a}$$

- For a change in the threshold voltage, $\Delta V_{th} = V_{th1} - V_{th0}$,

$$\Delta I_{D,Vth} = I_{DQ}(\beta_0, V_{th1}, V_{DD}) - I_{DQ}(\beta_0, V_{th0}, V_{DD}). \tag{24b}$$

- For a change in the supply voltage, $\Delta V_{DD} = V_{DD1} - V_{DD}$,

$$\Delta I_{D,VDD} = I_{DQ}(\beta_0, V_{th0}, V_{DD1}) - I_{DQ}(\beta_0, V_{th0}, V_{DD}). \tag{24c}$$

If the variations of all three circuit parameters are considered to be simultaneous, then the total change in quiescent drain current will be

$$\Delta I_{DQ} = I_{DQ}(\beta_1, V_{th1}, V_{DD1}) - I_{DQ}(\beta_0, V_{th0}, V_{DD}). \quad (25)$$

The proposed procedure can be applied and tested in conjunction with any general-purpose circuit simulator, because only the DC Operating Point Analysis is used. Four simulations of the bias circuit for a DC operating point analysis are needed to calculate the three actual increments of the quiescent drain current as follows: $s_0$ = nominal simulation for JFET_N_e0 and $V_{DD}$; $s_1$ = simulation for JFET_N_b1 and $V_{DD}$; $s_2$ = a simulation for JFET_N_t1 and $V_{DD}$; $s_3$ = a simulation for JFET_N_e0 and $V_{DD1}$. An additional simulation, $s_4$, performed for the same circuit with JFET_N_e and $V_{DD1}$ allows us to verify the validity of the equation (21) comparing its result with that given by equation (25).

# 4 Case studies

The proposed procedure to calculate the sensitivity factors of the quiescent drain current of a FET will be illustrated on two bias circuit topologies with the same NJET. The former study group is based on the bias circuit with four resistors as that given in Fig. 1, and constructed with a NJFET type BF245A.

The four resistance values are calculated assuming that the basic device parameters, supply voltage and quiescent point have been specified. For instance, for a given BF245A transistor ($V_{th}$ = -1.7 V and $\beta$ = 1.2 mA/V$^2$), supply voltage $V_{DD}$ equal to 10 V, the following quiescent point is desired to be fixed: $I_{DQ}$ = 1,3 mA, $U_{DSQ}$ = 5 V.

The study is conducted as follows. Implementing the design procedure that was developed and illustrated in the classroom lecture, the resistance values shown on the circuit diagram in Fig. 3 are obtained. The first sensitivity-factor analysis is made on this bias circuit. Then, keeping the coordinates of the quiescent point of transistor, we increase the resistance value $R_3$ and calculate again the others resistances. It is obtained the new circuit design in Fig. 4 for which the sensitivity factor analysis is repeated. A third study can be made on the circuit in Fig. 4 where the resistance $R_4$ keeps its value of 3.3 kΩ and $R_3$ is increased as in the second case. The results of the three designs are compared in order to illustrate the effect of increasing the negative feedback on the quiescent point stability.

The second study group concerns the three-resistor bias circuit derived from that shown in Fig. 1. This topology is firstly analyzed for the same quiescent operating point as that established by the bias circuit in Fig. 3. Then, we increase the resistance value R3 for two different values of resistance $R_4$. The results of the three designs of three-resistor bias circuit are compared in order to illustrate the effect of increasing the negative feedback on the quiescent point stability. Finally, the two topology types namely four- and three-resistor bias circuits are compared for the same value of $R_3$, i.e., the same negative feedback degree, in order to highlight their effectiveness and choose the best bias circuit for an application.

In order to compare the analysis results, both example groups use the same JFET models. For the first simulation, $s_0$, the device model is BF245A_e$_0$ where $\beta_0$=1.2 mA/V$^2$ and $V_{th0}$ = -1.7 V. Then, we perform the second simulation of circuit, $s_1$, where the device model BF245A_b1 has the parameters $\beta_1$=1.5 mA/V$^2$ and $V_{th0}$ = -1.7 V. The third simulation, $s_2$, is performed for device model BF245A_t1 with $\beta_0$=1.2 mA/V$^2$ and $V_{th1}$ = -1.5 V. The fourth simulation, $s_3$, is performed for a device model BF245A_e$_0$ and $V_{DD1}$=12 V. Finally, the simulation $s_4$, is performed for a device model BF245A_e with $\beta_1$=1.5 mA/V$^2$ and $V_{th1}$ = -1.5 V, and $V_{DD1}$=12 V.

The following general notations are used to display the results obtained from simulations and after some algebra: $s_i$ for the simulations ($s_0$, $s_1$, $s_2$, $s_3$ and $s_4$), $\Delta p$ for the parameter variations ($\Delta\beta$, $\Delta V_{th}$, and $\Delta V_{DD}$) and $S_p$ for the sensitivity factors of $I_{DQ}$ ($S_\beta$, $S_{Vth}$, and $S_{VDD}$).

## 4.1 Four-resistor bias circuit

(1.a) For the bias circuit in Fig. 3, the simulation results are summarized in Table 1, from which the actual increments of the quiescent drain current can be calculated.

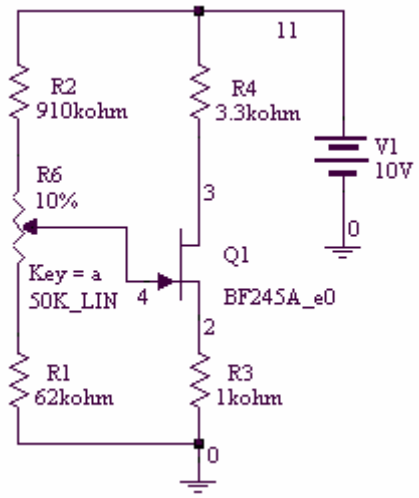


Fig.3. Four-resistor bias circuit ($R_3$ = 1 kΩ and $R_4$ = 3.3 kΩ).

Table 1. The simulation results for bias circuit in Fig. 3 ($R_3$ = 1 kΩ and $R_4$ = 3.3 kΩ).

| $s_i$ | $I_{DQ}$ (mA) | $\Delta I_{DQ}$ (mA) | $\Delta p$ | $S_p$ |
|---|---|---|---|---|
| $s_0$ | 1.31 | | | |
| $s_1$ | 1.39 | -0.08 | $\Delta\beta$ = -0.3mA/V$^2$ | +0.26 V$^2$ |
| $s_2$ | 1.16 | +0.14 | $\Delta V_{th}$ = -0.2V | - 0.7 mA/V |
| $s_3$ | 1.4 | -0.09 | $\Delta V_{DD}$ = -2 V | - 0.045 mA/V |
| $s_4$ | 1.34 | -0.03 | $\Delta\beta$ = 0.3mA/V$^2$<br>$\Delta V_{th}$ = 0.2 V<br>$\Delta V_{DD}$ = -2 V | |

(1.b) Keeping $I_{DQ}$ = 1.31 mA, $V_{GSQ}$ = - 0.655 V, and $V_{DSQ} \cong$ 5 V, we increase the value of resistance $R_3$ from 1 kΩ to 1.5 kΩ. Now, we calculate the necessary values of the resistances $R_1$, $R_2$, and $R_4$. The resistive network in Fig. 4 assures aforementioned coordinates of the initial quiescent point of transistor.

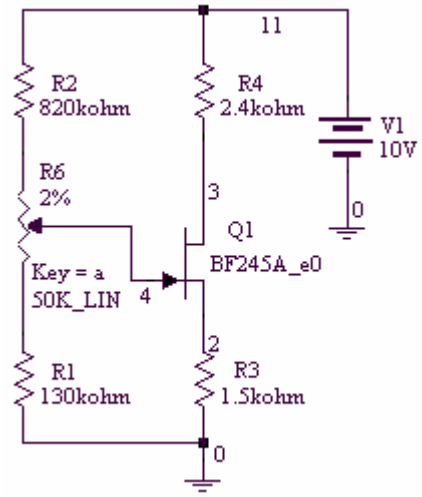


Fig.4. Four-resistor bias circuit ($R_3$ = 1.5 kΩ and $R_4$ = 2.4 kΩ).

All the simulations in above example were repeated for the bias circuit in Fig. 4, using the same JFET models namely: BF245A_e$_0$ for the simulations $s_0$ and $s_4$, BF245A_b1 for the simulation $s_1$, BF245A_t1 for the simulation $s_2$, and BF245A_e for the simulation $s_4$. The obtained results are given in Table 2.

Table 2. The simulation results for bias circuit in Fig. 4 ($R_3$ = 1.5 kΩ and $R_4$ = 2.4 kΩ).

| $s_i$ | $I_{DQ}$ (mA) | $\Delta I_{DQ}$ (mA) | $\Delta p$ | $S_p$ |
|---|---|---|---|---|
| $s_0$ | 1.31 | | | |
| $s_1$ | 1.36 | -0.05 | $\Delta\beta$ = -0.3mA/V$^2$ | +0.16 V$^2$ |
| $s_2$ | 1.2 | +0.11 | $\Delta V_{th}$ = -0.2V | - 0.55 mA/V |
| $s_3$ | 1.44 | -0.13 | $\Delta V_{DD}$ = -2 V | + 0.065 mA/V |
| $s_4$ | 1.4 | -0.09 | $\Delta\beta$ = 0.3mA/V$^2$<br>$\Delta V_{th}$ = 0.2 V<br>$\Delta V_{DD}$ = -2 V | |

(1.c). The third study is performed for the following values of the resistances $R_3$ and $R_4$: $R_3$ = 1.5 kΩ and $R_4$ = 3.3 kΩ. Obviously, the quiescent operating point moves from its initial position toward a smaller drain-source voltage namely $V_{DSQ}$ = 3.7 V. As it was expected, almost all results of the simulations and analysis for this new design repeat those given in the Table 2, because the resistive network that fixes the drain current and the gate-source voltage is unchanged. Only the drain-source voltage is affected by modifying $R_4$ as it is shown in Table 3.

Table 3. The simulation and analysis results for bias circuit in Fig. 4 for $R_3$ = 1.5 kΩ and $R_4$ = 3.3 kΩ.

| $s_i$ | $I_{DQ}$ (mA) | $\Delta I_{DQ}$ (mA) | $V_{DSQ}$ (V) | $\Delta V_{DSQ}$ (V) |
|---|---|---|---|---|
| $s_0$ | 1.31 | | 3.7 | |
| $s_1$ | 1.36 | -0.05 | 3.43 | +0.27 |
| $s_2$ | 1.2 | +0.11 | 4.22 | - 0.522 |
| $s_3$ | 1.44 | -0.13 | 5.04 | -1.34 |
| $s_4$ | 1.4 | -0.09 | 5.26 | -1.56 |

An easy comparison of the three designs of the same bias circuit topology can be performed on basis of the result summary in the Table 4 in terms of total variations of the drain current and drain-source voltage. There, the total variations of the quiescent drain current and drain-source voltage are denoted as $\Delta I_{DQ,tot}$ and $\Delta V_{DSQ,tot}$. The shown results are obtained from the simulation $s_4$ that takes into account all parameter variations ($\Delta\beta$ = 0.3mA/V$^2$, $\Delta V_{th}$ = 0.2 V, and $\Delta V_{DD}$ = -2 V).

Table 4. Summary of the results of the three studies for four-resistor bias circuit.

| Study/Topology | | $\Delta\beta$ (mA/V$^2$) | $\Delta V_{th}$ (V) | $\Delta V_{DD}$ (V) |
|---|---|---|---|---|
| (1.a) | $S_p$ | +0.26 *) | -0.7 **) | -0.045 **) |
| $R_3$=1kΩ, | $\Delta I_{DQ}$ (mA) | -0.08 | +0.15 | -0.09 |
| $R_4$=3.3kΩ | $\Delta V_{DSQ}$ (V) | +0.3 | -0.54 | -1.65 |
| | $\Delta I_{DQ,tot}$ = -0.03mA; $\Delta V_{DSQ,tot}$ = -1.88V | | | |
| (1.b) | $S_p$ | +0.16 *) | -0.55 **) | +0.065 **) |
| $R_3$=1.5kΩ | $\Delta I_{DQ}$ (mA) | -0.05 | +0.11 | -0.13 |
| $R_4$=2.4kΩ | $\Delta V_{DSQ}$ (V) | +0.35 | -0.61 | -1.59 |
| | $\Delta I_{DQ,tot}$ = -0.09mA; $\Delta V_{DSQ,tot}$ = -1.64V | | | |
| (1.c) | $S_p$ | +0.16 *) | -0.55 **) | +0.065 **) |
| $R_3$=1.5kΩ | $\Delta I_{DQ}$ (mA) | -0.05 | +0.11 | -0.13 |
| $R_4$=3.3kΩ | $\Delta V_{DSQ}$ (V) | +0.35 | -0.61 | -1.59 |
| | $\Delta I_{DQ,tot}$ = -0.09mA; $\Delta V_{DSQ,tot}$ = -1.56V | | | |

In the Table 4, some units of measure were replaced with the superscripts *) and **) respectively that means ($V^2$) and (mA/V) respectively.

At first glance, one easily observes that increasing the negative feedback do not yields a better sensitivity of the quiescent operating point, because the gate voltage is kept constant. On the contrary, increasing the resistance value of resistor in series with the source of transistor causes the movement of the quiescent operating point and decreasing of the voltage gain of the amplifier as well as output voltage range.

## 4.2 Three-resistor bias circuit

(2.a) Keeping the given coordinates of the quiescent point of transistor namely $I_{DQ}$ = 1.31 mA, $V_{GSQ}$ = - 0.655 V, and $V_{DSQ} \cong$ 5 V, the three-resistor bias circuit in Fig. 5 was obtained. For this bias circuit, the simulation and analysis results are summarized in Table 5.

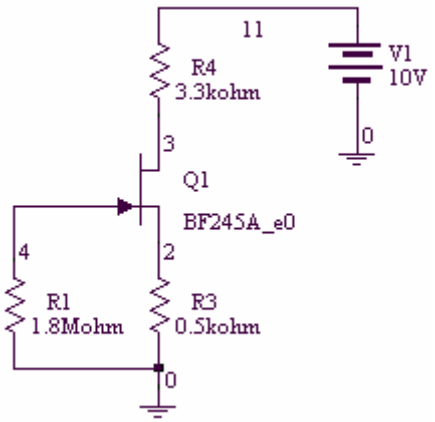


Fig.5. Three-resistor bias circuit ($R_3$ = 0.5 kΩ and $R_4$ = 3.3 kΩ).

Table 5. The simulation results for bias circuit in Fig. 5 ($R_3$ = 0.5 kΩ and $R_4$ = 3.3 kΩ).

| $s_i$ | $I_{DQ}$ (mA) | $\Delta I_{DQ}$ (mA) | $\Delta p$ | $S_p$ |
|---|---|---|---|---|
| $s_0$ | 1.31 | | | |
| $s_1$ | 1.44 | -0.13 | $\Delta\beta$= -0.3mA/V$^2$ | 0.43 V$^2$ |
| $s_2$ | 1.09 | +0.22 | $\Delta V_{th}$= -0.2V | -1.1mA/V |
| $s_3$ | 1.31 | 0 | $\Delta V_{DD}$ = -2 V | 0 |
| $s_4$ | 1.20 | +0.11 | $\Delta\beta$= -0.3mA/V$^2$<br>$\Delta V_{th}$= -0.2V<br>$\Delta V_{DD}$= -2 V | |

(2.b) In order to hightlight the effect of the negative feedback introduced by the resistor connected in series with the source of transistor on the circuit sensitivity factors, we double the resistance value $R_3$ and calculate again the others resistances. Firstly, we expect to a movement of the point Q and a better stability of the new point Q. The new design of the three-resistor bias circuit is shown in Fig. 6 and the mentioned modifications can be observed in the Table 6 that resumes the main analysis results.

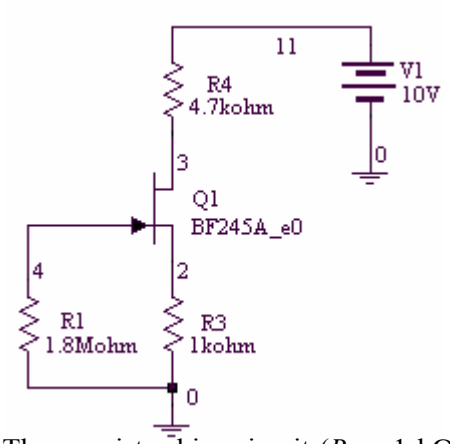


Fig.6. Three-resistor bias circuit ($R_3$ = 1 kΩ and $R_4$ = 4.7 kΩ).

Table 6. The simulation results for bias circuit in Fig. 6 ($R_3$ = 1 kΩ and $R_4$ = 4.7 kΩ).

| $s_i$ | $I_{DQ}$ (mA) | $\Delta I_{DQ}$ (mA) | $\Delta p$ | $S_p$ |
|---|---|---|---|---|
| $s_0$ | 0.855 | | | |
| $s_1$ | 0.917 | -0.06 | $\Delta\beta$= -0.3mA/V$^2$ | +0.2 V$^2$ |
| $s_2$ | 0.723 | +0.132 | $\Delta V_{th}$= -0.2V | -0.66mA/V |
| $s_3$ | 0.855 | 0 | $\Delta V_{DD}$ = -2 V | 0 |
| $s_4$ | 0.779 | +0.076 | $\Delta\beta$= -0.3mA/V$^2$<br>$\Delta V_{th}$= -0.2V<br>$\Delta V_{DD}$= -2 V | |

(2.c) We repeat the sensitivity factor analysis for the third design namely the schematic diagram in Fig. 6 where the resistance $R_4$ has a value of 3.3 kΩ. Again, as in the study (1.c), only the drain-source voltage modifies comparatively to its correspondent in previous case. The result summary of this analysis is presented in Table 7.

Table 7. The simulation results for bias circuit in Fig. 6 for $R_3$ = 1 kΩ and $R_4$ = 3.3 kΩ.

| $s_i$ | $I_{DQ}$ (mA) | $\Delta I_{DQ}$ (mA) | $V_{DSQ}$ (V) | $\Delta V_{DSQ}$ (V) |
|---|---|---|---|---|
| $s_0$ | 0.855 | | 6.32 | |
| $s_1$ | 0.917 | -0.06 | 6.05 | +0.267 |
| $s_2$ | 0.723 | +0.132 | 6.88 | - 0.568 |
| $s_3$ | 0.855 | 0 | 8.32 | -2.00 |
| $s_4$ | 0.779 | +0.076 | 8.65 | -2.33 |

To an easy comparison of the three studies concerning the different designs of the three-resistor bias circuit, the

main results are resumed in Table 8 in terms of total variations of the drain current and drain-source voltage. These results are obtained from the simulation $s_4$ that takes into account all parameter variations ($\Delta\beta$ = 0.3mA/V$^2$, $\Delta V_{th}$ = 0.2 V, and $\Delta V_{DD}$ = -2 V).

Table 8. Summary of the results of the three studies for three-resistor bias circuit.

| Study/Topology | | $\Delta\beta$ (mA/V$^2$) | $\Delta V_{th}$ (V) | $\Delta V_{DD}$ (V) |
|---|---|---|---|---|
| (2.a) $R_3$=0.5kΩ $R_4$=3.3kΩ | $S_p$ | +0.26 *) | -0.7 **) | -0.045 **) |
| | $\Delta I_{DQ}$ (mA) | -0.08 | +0.15 | -0.09 |
| | $\Delta V_{DSQ}$ (V) | +0.3 | -0.54 | -1.65 |
| | $\Delta I_{DQ,tot}$ = -0.11mA; $\Delta V_{DSQ,tot}$ = -2.39V | | | |
| (2.b) $R_3$=1kΩ, $R_4$=4.7kΩ | $S_p$ | +0.16 *) | -0.55 **) | +0.065 **) |
| | $\Delta I_{DQ}$ (mA) | -0.05 | +0.11 | -0.13 |
| | $\Delta V_{DSQ}$ (V) | +0.35 | -0.61 | -1.59 |
| | $\Delta I_{DQ,tot}$ = +0.076mA; $\Delta V_{DSQ,tot}$ = -2.43V | | | |
| (2.c) $R_3$=1kΩ, $R_4$=3.3kΩ | $S_p$ | +0.16 *) | -0.55 **) | +0.065 **) |
| | $\Delta I_{DQ}$ (mA) | -0.05 | +0.11 | -0.13 |
| | $\Delta V_{DSQ}$ (V) | +0.35 | -0.61 | -1.59 |
| | $\Delta I_{DQ,tot}$ = +0.076mA; $\Delta V_{DSQ,tot}$ = -2.33V | | | |

First remark refers to the null value of the sensitivity factor $S_{VDD}$, because $I_{DQ}$ is independent on $V_{DD}$ in a three-resistor bias circuit. Also, one again observes that increasing the negative feedback do not yields a significantly enhancement of the quiescent operating point stability, because the gate voltage is kept constant at zero. Generally, such a topology is more sensible to variations of the device parameters than its counterpart with voltage divider in gate. This behavioural difference appears by comparing the total variations of the drain current and drain-source voltage provided by the studies (1.a) and (2.c) that correspond to the same values of the resistances $R_3$ and $R_4$ in both topologies ($R_3$ = 1 kΩ and $R_4$ = 3.3 kΩ).

In almost all cases, once the bias circuit design has been completed, the student is instructed to verify the design of the bias circuit using a graphical load line approach [8]. Using a circuit simulator the design can rapidly be verified and then modified if is necessary.

Beside the partial variations of the drain current, the involved simulations provide the partial variations of the drain-source voltage, and gate-source voltage thus ensuring a complete evaluation of the effect of the variations of the parameter values on each coordinate of the quiescent operating point. The commonly used equations to describe the effect of such variations on the quiescent operating point can be easily verified by processing the simulation results.

Such studies can be developped for different topologies of bias circuits with BJTs or FETs even those with current mirrors in order to choose the best one for a given operating condition set or verify it before implementation.

# 5 Conclusion

The paper presents a procedure to calculate the sensitivity factors of the quiescent drain current of a FET operating in the active region using a general-purpose circuit simulator. This one can be applied to bias circuits with BJTs too. We demonstrated that the sensitivity factors of the quiescent drain current can be calculated by repeated simulations of the bias circuit. Each change of a circuit parameter involved in the sensitivity analysis modifies either the device model or the parameter values.

Such a procedure based on a circuit simulator allows the students to verify and, if necessary, modify the bias circuit design on desired direction and rapidly test it again.

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