# Matlab & Simulink Simulation with FPGA-Based Implementation Sliding Mode Control of a Permanent Magnet Synchronous Machine Drive

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*Abstract:* This paper starts with an overview of *FPGA* technology development, followed by a presentation of design methodologies, development tools and relevant *CAD* environments, including the use of portable hardware description languages and system level programming/design tools. In this paper, a new contribution for the *FPGA*-Based implementation of controls electrical. This approach is based on concept modularity and reusability.

In this paper is presents a detailed description of the structure by Indirect Sliding Mode of Permanent Magnet Synchronous Machine *PMSM*. Experimental results carried from a prototyping platform are given to illustrate the efficiency and the benefits of the proposed approach and the various stages of implementation of this structure in *FPGA*.

*Keywords:* Permanent Magnet Synchronous Machine (*PMSM*), *FPGA*, Indirect Sliding Mode Control, Power System Control, Systems Generator, Reusability, *PWM*.

## 1. Introduction

The Permanent magnet synchronous Motor is an electric actuator very robust and has a low moment of inertia compared to a DC machine.

This characteristic confers to him a dynamics characterized by weak constants of times what makes it possible to design controls in torque, of speed and in position with a better precision and very satisfactory dynamic performances[1, 2, 3].

Currently, two of the best techniques for controlling electrical machines have high performance for the Control of *PMSM*, namely the Direct Torque Control and the Space Vector Modulation Control. Invented by twentieth century, its operating principles are totally different but the goals are the same. its main objectives and control of torque and current to force the target to follow instructions given by the user with high accuracy and stability, but regardless of the variation of machine parameters and disturbances submitted by outside [4].

However, specific hardware technologies such as field programmable gate arrays (*FPGAs*) can also be considered as an appropriate solution in order to boost the performance of controllers. Indeed, these generic components combine low cost development (owing to their reprogrammability), use of convenient software tools, and more and more significant integration density [5-8]. *FPGA* technology is now considered by an increasing number of designers in various fields of application such as wired and wireless telecommunications [9], and image and signal processing [10, 11], where the always more demanding data throughputs take advantage of the ever increasing density of the chips. Still, more recently, other application fields are in growing demand, such as medical equipment [12], robotics [13]–[15], automotive [16], and space and aircraft embedded control systems [17]. For these embedded applications, reduction of the power consumption, thermal management and packaging, reliability, and protection against solar radiation are of prime importance and electrical control systems. This last domain, i.e. the studies of control of electrical machines, will be presented in this paper.

The principal advantages of the digital solutions are as follows:

- High flexibility of changing structures of control;

- Immunity against disturbances;
- No problems of variations of control parameters.

With technological advancement, increased integration of *FPGA* devices is increasing. Nowadays, the density of *FPGA* components can achieve the equivalent of *10* million logic gates with switching frequencies of around *500 MHz*. This allows the implementation of complex algorithms control in their entirety with a small period of time to load.

The inherent parallelism of *FPGA* components offers the possibility to run several algorithms in parallel control and configure them according to the defined criteria. Dynamic configuration between the algorithms control has as objective to select the appropriate algorithms depending on your point of operation. It may be useful also to ensure continuous operation in case of faults (sensors, switches ...).

This paper presents the realization of a platform for *Sliding Mode* control (*SMC*) of *PMSM* using *FPGA* based controller. This realization is especially aimed for future high performance applications. In this approach, not only the architecture corresponding to the control algorithm is studied, but also architecture and the *ADC* interface and *RS232 UART* architecture.

Considering the complexity of the diversity of the electric control devices of the machines, it is difficult to define with universal manner a general structure for such systems. However, by having a reflexion compared to the elements most commonly encountered in these systems, it is possible to define a general structure of an electric control device of machines which is show in *Fig.1*:

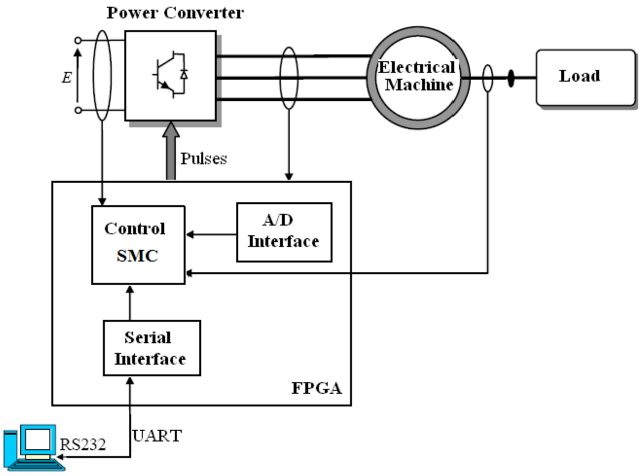



Fig.1: Architecture Sliding Mode Control

## 2. Principle of Variable Structure Systems

The principle of variable structure systems has been studied primarily in the Soviet Union. Subsequently, much research on power systems control field has been made elsewhere to complement the theoretical study and find some possible applications. The sliding mode control is a particular operating mode of variable structure system. Using this command has been limited longer due to oscillations to the phenomena of slip and limitations of the switching frequency of power switches.

There are different regulatory structures by sliding mode current in systems based on variable structure sliding mode control.

Consider the following controlled system (1):

$$\frac{dy}{dt} = h(x) + G(x)u \tag{1}$$

Where u is the input vector of dimension, m, y is the state function of dimension, *n*, *h* is the state function describing the system evolution over time and *G* is a matrix of dimension *n*m*. For the synthesis of a regulatory structure by sliding mode, it is necessary to define initially the switching function *S(y)* of dimension *m*. $S(y) = [S_1(y)....S_m(y)]^t$, where $S_i(y)$ is the $i^{th}$ switching function *S(y)*.

## 3. Modeling of the Synchronous Permanent magnet Machine

The motor considered in this paper is an interior PMSM which consists of a three phase stator windings and a PM rotor. The voltage equations in a synchronous reference frame can be derived as follows,

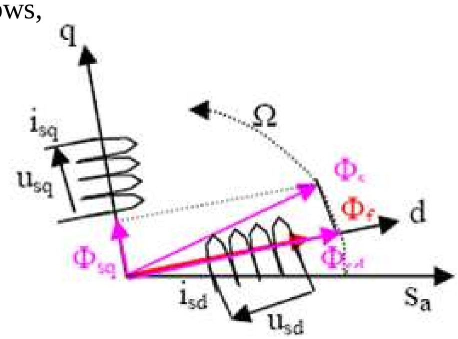



Fig.2: Scheme of the synchronous machine

$$u_{sd} = r_s.i_{sd} + \frac{d\Phi_{sd}}{dt} - \omega.\Phi_{sq} \tag{2}$$

$$u_{sq} = r_s.i_{sq} + \frac{d\Phi_{sq}}{dt} - \omega.\Phi_{sd} \qquad (3)$$

Where the direct and quadrate axis flux linkages are,

$$\Phi_{sd} = L_d.i_{sd} + \Phi_f \qquad (4)$$

$$\Phi_{sq} = L_q.i_{sq} \qquad (5)$$

The electromagnetic torque of the motor can be evaluated as follows,

$$Ce = \frac{3}{2} p\left[\phi_f.I_q + (L_d - L_q).I_d.I_q\right] \qquad (6)$$

The motor dynamics can be simply described by the equation (7).

$$Ce - C_r = J.\frac{d\Omega}{dt} + f.\Omega \qquad (7)$$

With:

$\Omega$: rotation's speed mechanical of the PMSM

$\omega$: rotation's speed electric.

$p$: Number of pairs of poles.

$J$ : Total moment of inertia brought back on the tree of the PMSM.

$f$ : Coefficient of viscous friction.

$C_r$: Resistive torque.

$f$: flux produced by the permanent magnet.

$\Phi_{sd}$: d axis stator magnetic flux,

$\Phi_{sq}$: q axis stator magnetic flux,

$L_{sd}$: d axis stator leakage inductance,

$L_{sq}$: q axis stator leakage inductance,

$r_s$: stator winding resistance,

$C_e$: electromagnetic torque,

# 4. The control law based on sliding mode control of the inverter development

The control law sliding mode must simultaneously satisfy the conditions of invariance and attractiveness. To do this the switching function *S (y)* must satisfies [5]:

- The invariance condition: $\begin{cases} S(y) = 0 \\ \dot{S}(y) = 0 \end{cases}$ (8)

- The attractiveness condition:

$$\begin{cases} \dot{S}_i(y) \prec 0 \quad si \quad S_i(y) \succ 0 \\ \dot{S}_i(y) \succ 0 \quad si \quad S_i(y) \prec 0 \end{cases} for(i = 0...m) \qquad (9)$$

These conditions lead to determining a new vector control:

$$u^* = u_{eq} + u_{att} \qquad (10)$$

The vector control given by equation (10) comprises two terms [7]:

- The first is the control vector specifying the equivalent control for the system to stay on the sliding surface.
- The second is the vector control that ensures the attractive control system outside the sliding surface. It also requires the system dynamics starting from an initial point until it reaches the sliding surface *(Fig.3)* [9].

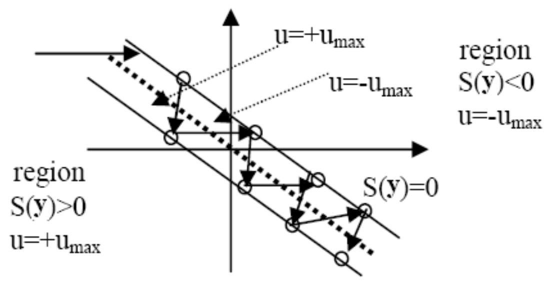



Fig.3: The state of Sliding Mode trajectory

# 5. Indirect control by PMSM sliding mode stator current

## 5.1. Synthesis of a-indirect control by sliding mode

The indirect control by sliding mode stator current vector of a permanent magnet synchronous machine ensures the calculation of direct and inverse components of the reference voltage vector expressed in the *d*-*q* plane. These components are then applied across the phases of the stator *PMSM* through an intermediate stage of the *PWM*. The development of such law control must satisfy simultaneously the conditions of invariance and attractiveness given by equations (8) and (9). The terms $-\omega_{dq}\Phi_{sq}$ and $\omega_{dq}\Phi_{sd}$ are considered as terms of electromotive forces induced on the axis d and q and the expressions of the derivatives of the switching function $\dot{S}_{isd}$ and $\dot{S}_{isq}$ are given by equations (11) and (12). Thus, the indirect control by sliding mode $d$ and $q$ components of stator current can be carried out by taking on each axis $d$ and $q$. Therefore, each component $V_{sd}^*$ and $V_{sq}^*$ is composed by two terms as shown in equation (10). The first term is the equivalent voltage vector which is active in steady state, while the second term is the voltage vector which is attractive assets in transition.

$$\begin{cases} V_{sd}^* = V_{sdeq} + V_{sdatt} \\ V_{sq}^* = V_{sqeq} + V_{sqatt} \end{cases} \tag{11}$$

For trajectories currents $i_{sd}$ and $i_{sq}$ remained on their sliding surfaces ($S_{isd}=0$ and $S_{isq}=0$), apply the voltage vectors $V_{sdeq}$ and $V_{sqeq}$ on the axis $d$ and axis $q$. These vectors can be calculated taking into account the following invariance conditions:

$$\begin{cases} S_{isd} = (i_{sd}^* - i_{sd}) = 0 \\ \dot{S}_{isd} = 0 \end{cases} \Rightarrow \begin{cases} i_{sd}^* = i_{sd} \\ \dfrac{S_{isd}}{dt} = -\dfrac{1}{L_d}(V_{sdeq} - r_s i_{sd} + \omega_{dq}\Phi_{sq}) = 0 \end{cases}$$

$$\Rightarrow V_{sdeq} = r_s i_{sd} - \omega_{dq}\Phi_{sq} = r_s i_{sd}^* - \omega_{dq}\Phi_{sq} \tag{12}$$

$$\begin{cases} S_{isq} = (i_{sq}^* - i_{sq}) = 0 \\ \dot{S}_{isq} = 0 \end{cases} \Rightarrow \begin{cases} i_{sq}^* = i_{sq} \\ \dfrac{S_{isq}}{dt} = -\dfrac{1}{L_q}(V_{sqeq} - r_s i_{sq} - \omega_{dq}\Phi_{sd}) = 0 \end{cases}$$

$$\Rightarrow V_{sqeq} = r_s i_{sq} + \omega_{dq}\Phi_{sd} = r_s i_{sq}^* + \omega_{dq}\Phi_{sd} \tag{13}$$

Considering the derived of switching functions and the control formulas, the new components $V_{sd}^*$ and $V_{sq}^*$ will be:

$$\begin{cases} V_{sd}^* = r_s i_{sd}^* - \omega_{dq}\Phi_{sq} - L_d \dfrac{S_{isd}}{dt} = V_{sdeq} + V_{sdatt} \\ V_{sq}^* = r_s i_{sq}^* + \omega_{dq}\Phi_{sd} - L_q \dfrac{S_{isq}}{dt} = V_{sqeq} + V_{sqatt} \end{cases} \tag{14}$$

From this attractive voltage vector system of reference voltage vector involves the switching function derivative $\dot{S}_{isd}$ and $\dot{S}_{isq}$. A structure of attractiveness is chosen at a constant speed and proportional action, which gives:

$$\begin{cases} V_{sdatt} = L_d(A_d \operatorname{sgn}(S_{isd}) + K_d S_{isd}) \\ V_{sqatt} = Lq(A_q \operatorname{sgn}(S_{isq}) + K_q S_{isq}) \end{cases} \tag{15}$$

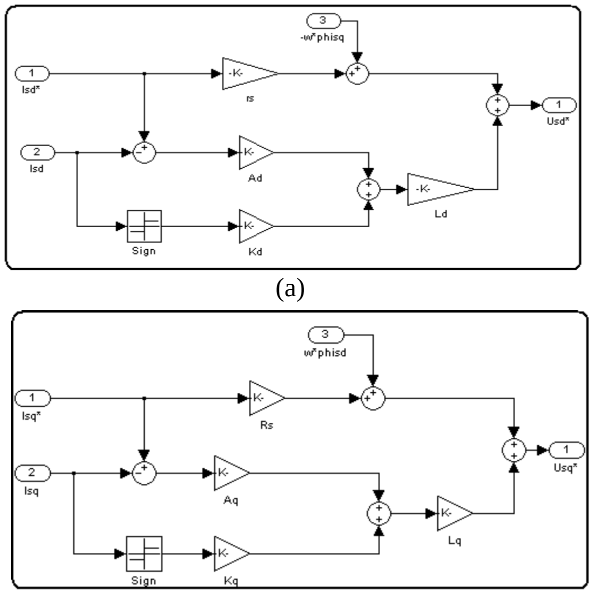
By applying the reference voltage vector given by the previous system, the result of the product of each of switching functions $\dot{S}_{isd}$ and $\dot{S}_{isq}$ its own derivative is given by the following system:

$$\begin{cases} S_{isd}\,\dot{S}_{isd} = -\dfrac{r_s}{L_d} S_{isd}^2 - A_d S_{isd} \operatorname{sgn}(S_{isd}) - K_d S_{isd}^2 \\ S_{isq}\,\dot{S}_{isq} = -\dfrac{r_s}{L_q} S_{isq}^2 - A_q S_{isq} \operatorname{sgn}(S_{isq}) - K_q S_{isq}^2 \end{cases} \tag{16}$$

In summary:

$$\begin{bmatrix} V_{sd}^* \\ V_{sq}^* \end{bmatrix} = r_s \begin{bmatrix} i_{sd}^* \\ i_{sq}^* \end{bmatrix} + \begin{bmatrix} -\omega_{dq}\Phi_{sq} \\ \omega_{dq}\Phi_{sd} \end{bmatrix} + \begin{bmatrix} L_d & 0 \\ 0 & L_q \end{bmatrix} \left( \begin{bmatrix} A_d & 0 \\ 0 & A_q \end{bmatrix} \begin{bmatrix} \operatorname{sgn}(S_{isd}) \\ \operatorname{sgn}(S_{isq}) \end{bmatrix} + \begin{bmatrix} K_d & 0 \\ 0 & K_q \end{bmatrix} \begin{bmatrix} S_{isd} \\ S_{isq} \end{bmatrix} \right) \tag{17}$$

The following figure shows the sliding mode correction block diagram, satisfying the attractiveness and invariance conditions:




(a)

(b)

Fig.4: Block diagram of the corrector indirect sliding mode (a) $i_{sd}$, (b) $i_{sq}$.

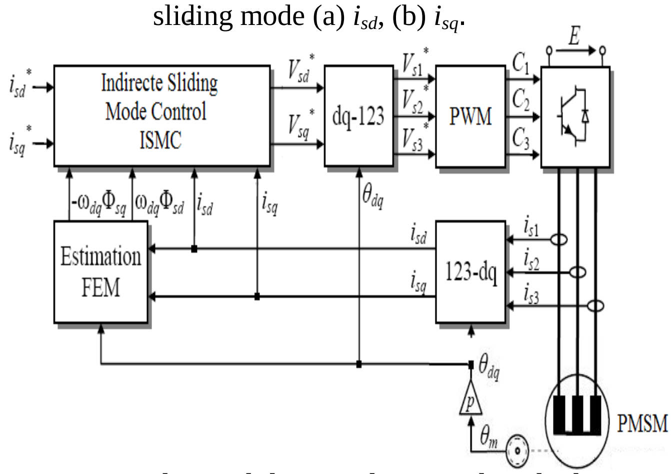
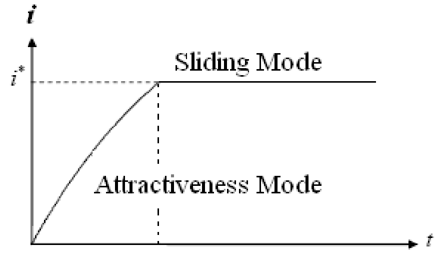
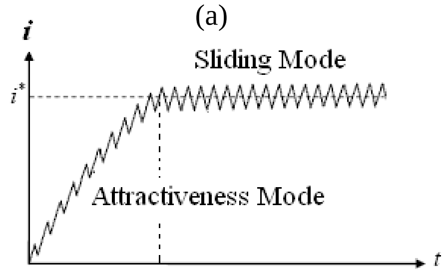



Fig. 5: Indirect Sliding Mode Control applied to a PMSM

For a given value of the reference current, the current i trajectory described by the system from *Fig.4* is shown in *Fig.6*. The trajectory obtained is characterized by two stages: the attractiveness mode and sliding mode.




(a)




(b)

Fig.6: Trajectory characterizing the indirect control mode by sliding (a) Continuous operation (b) Discrete operation

From this entire process, systems with variable structure controlled by an indirect sliding mode control have several properties:

- The system doesn't dependent only on the sign of the switching function, but also it depends on its value.
- The dynamics of the system controlled by such control depends essentially on the coefficients choice of the attraction mode matrices *K* and *A*.
- The theory of indirect sliding mode is appropriate to systems whose control is discontinuous.

## 5.2. Results of simulations

The *Fig. 7* shows the general structure of sliding mode control of the *PMSM* stator current in the *dq* reference. The $i_{sd}$ and $i_{sq}$ currents are subjected to the transformation of Concordia for components $i_{s\alpha}$ and $i_{s\beta}$ . Each component is controlled by a sliding mode corrector that provide the reference $U_{sd}$* and $U_{sq}$* dependant by the electromotive forces of voltages. The result is applied to the Pulse Width Modulation (*PWM*) component used for controlling the voltage inverter, which generates three-phase voltages $V_a$, $V_b$ and $V_c$ that are subject to a Park transformation. Finally, the $V_{sd}$ and $V_{sq}$ are applied directly in *PMSM*.

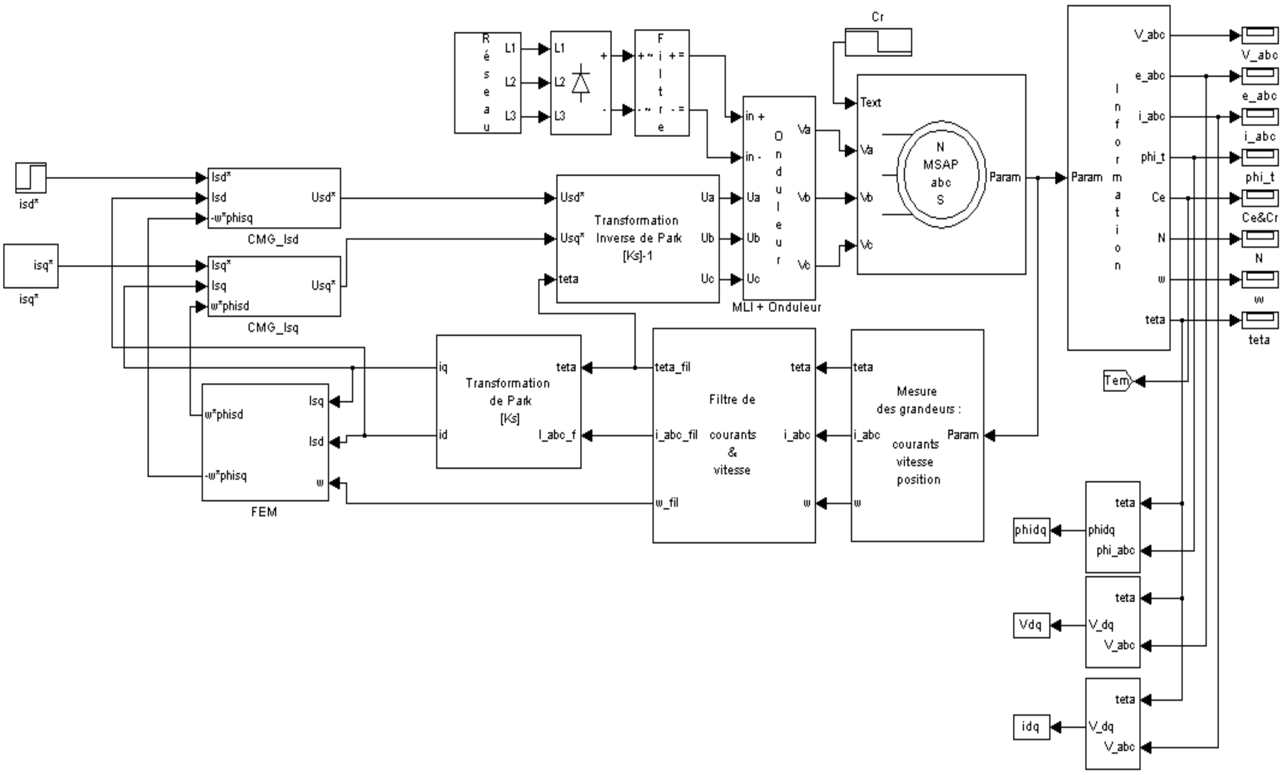



Fig. 7: Block diagram of indirect sliding mode control for *PMSM*

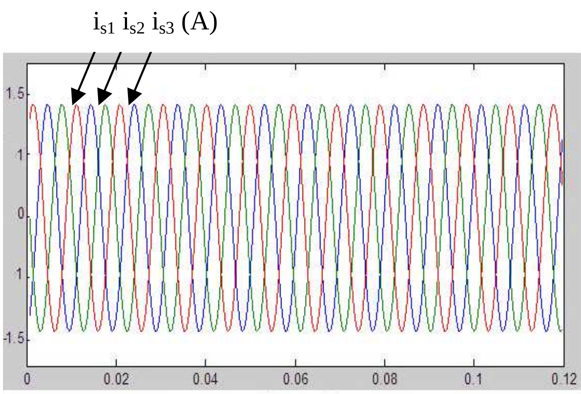



Fig.8: Stator current

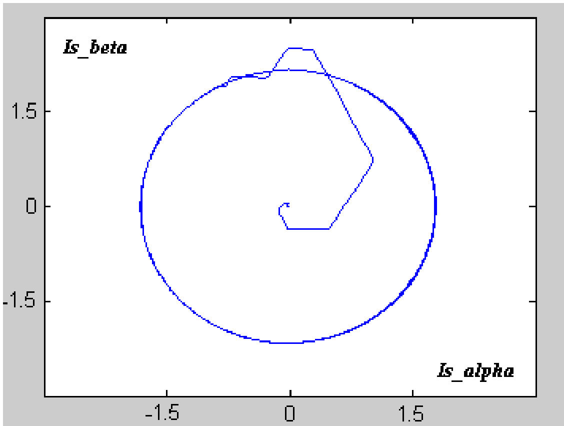



Fig.9: Instead of the current vector in the plane *(α β)*

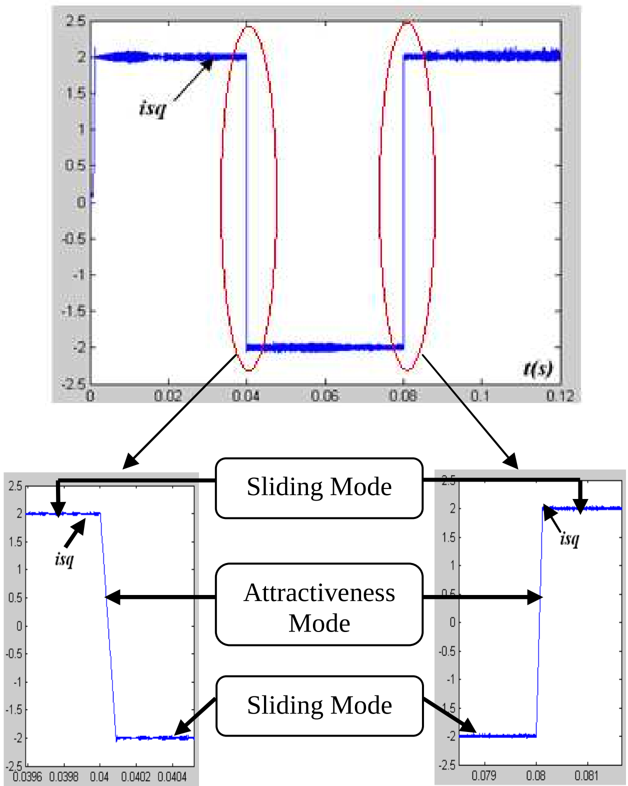



Fig.10: Quadratic Current $i_{sq}$

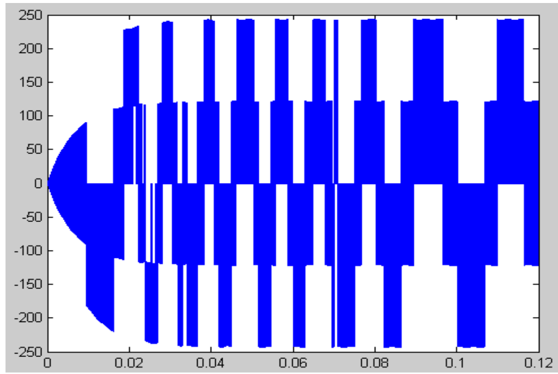


Fig.11: Voltage $V_{s1}$

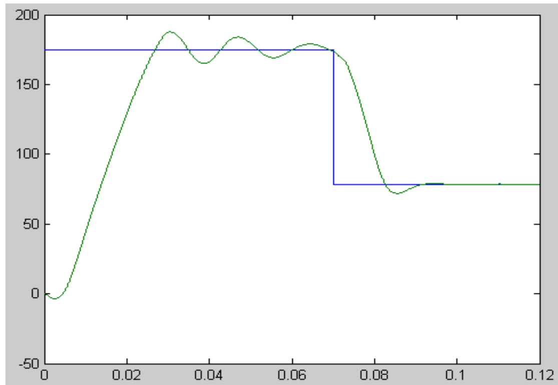


Fig.12: Speed Rotor

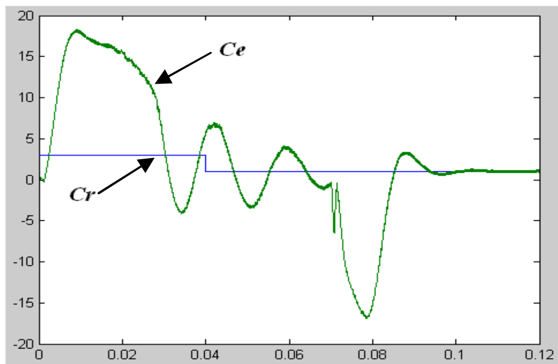



Fig.13: Torque electromagnetic

In the *Fig. 8* to *13* are show the simulation result of indirect control by sliding mode stator when the current is applied between $+I_{sn}$ and $-I_{sn}$ ($E=380V$, frequency $PWM=5\ KHz$, $K_d= K_q = A_d= A_q= 320$). It should be noted that the dynamics of the transient is lower than that obtained with other commands. However, the current has better quality control in steady state with fewer oscillations.
The choice of coefficients $A_d$, $A_q$, $K_d$ and $K_q$ was selected by follows criteria:

- The module reference voltage vector must not exceed the maximum amplitude that can generate voltage of the inverter.
- Coefficients chosen provide good robustness against parameter variations where the higher coefficients provide better control.

The coefficients should not cause strong current oscillations.

The chosen coefficients are the result of several simulations where the selection criteria is it a good factor.

These coefficients allow controlled quantities to follow their references to an error of about 99% on the PMSM parameters ($L_d$, $L_q$ and $r_s$).

# 6. Development of the design methodology

## 6.1. FPGA devices

There are several manufacturers of *FPGA* components such: *Actel*, *Xilinx* and *Altera*…etc. These manufacturers use different technologies for the implementation of *FPGAs*. These technologies are attractive because they provide reconfigurable structure that is the most interesting because they allow great flexibility in design.

Nowadays, *FPGAs* offer the possibility to use dedicated blocks such as *RAMs*, multipliers wired interfaces *PCI* and *CPU* cores.

The architecture designing was done using with *CAD* tools. The description is made graphically or via a hardware description language high level, also called *HDL* (Hardware Description Language). Is commonly used language *VHDL* and *Verilog*. These two languages are standardized and provide the description with different levels, and especially the advantage of being portable and compatible with all *FPGA* technologies previously introduced.

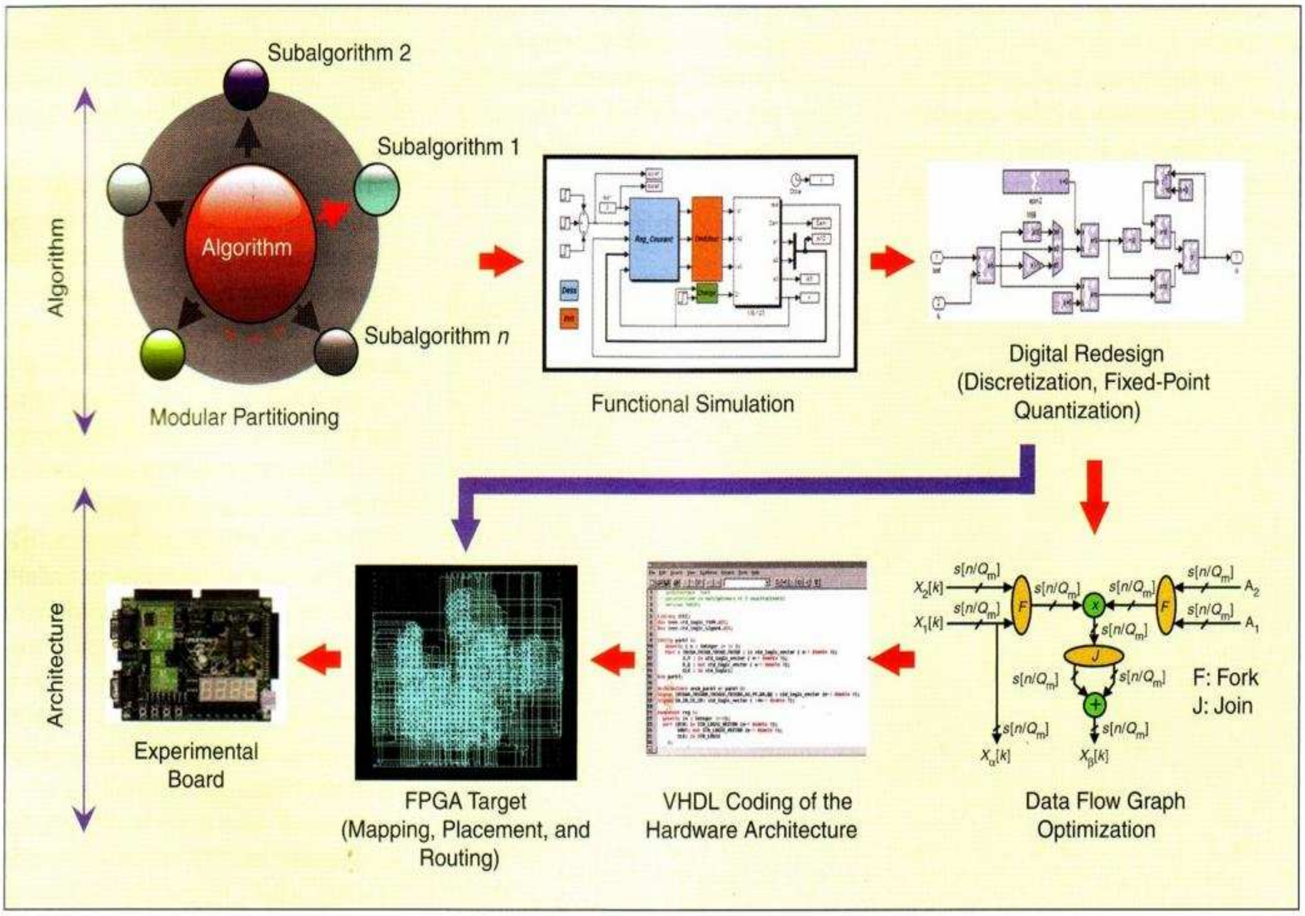



Fig.14: Programming *FPGA* devisee

The *Fig.14* summarizes the different steps of programming an *FPGA*. The synthesizer generated with *CAD* tools first one *Netlist* which describes the connectivity of the architecture. Then the placement-routing optimally place components and performs all the routing between different logic. These two steps are used to generate a configuration file to be downloaded into the memory of the *FPGA*. This file is called *bitstream*. It can be directly loaded into *FPGA* from a host computer.

In this paper an *FPGA XC3S500E Spartan3E* from Xilinx is used. This *FPGA* contains 400,000 logic gates and includes an internal oscillator which issuer a *50MHz* frequency clock. The map is composed from a matrix of 5376 slices linked together by programmable connections (*Fig.15*).

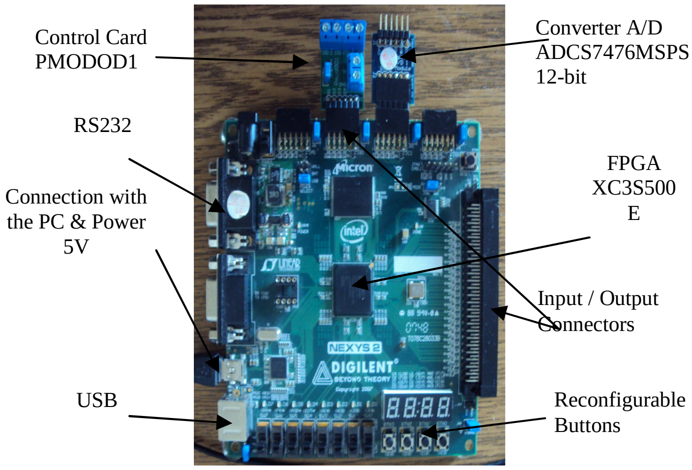



Fig.15: The *FPGA XC3S500E* Spartan

## 6.2. Simulation Procedure

The simulation procedures begin by checking the control algorithm functionality trough a functional model using *Simulink's* (System Generator for *Xilinx*) blocks. For this application, the functional model consists in a Simulink model of the Indirect Sliding mode Control algorithm associated with a voltage inverter and *PMSM* model. *Fig.16* gives a global view of the functional model.

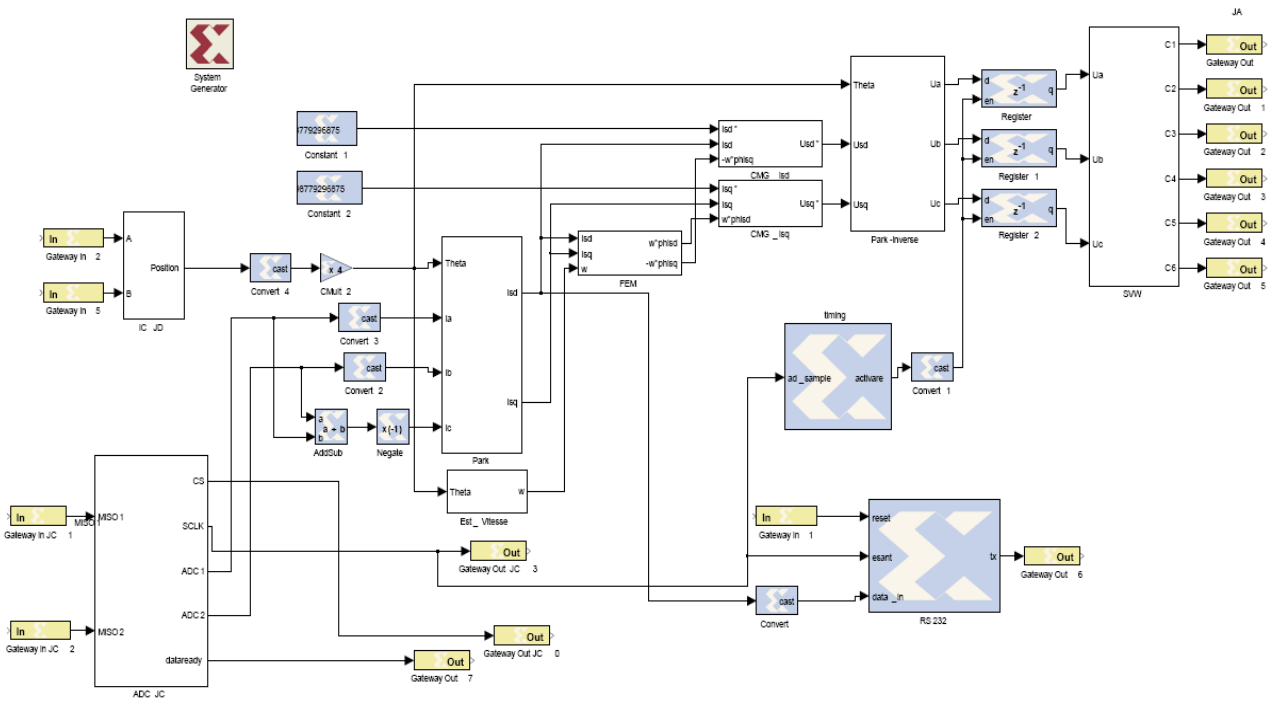



Fig.16: The schematic bloc of functional model

The description of the different modules is detailed below:

- The blocks of coordinate's transformation: the transformation of Park Inverse (*abc-to-dq*);
- The blocks of coordinate's transformation: the transformation of Park (*dq-to-abc*);
- The *PWM* block is the most important, because can provide control pulses to the *IGBT* voltage inverter in the power section from well-regulated voltages;
- Two blocks Sliding Mode Corrector for the regulation of currents $I_{sd}$ and $I_{sq}$ from the comparison of measured values and reference values of stator currents;

- The block for *FEM* calculation and speed estimator;
- The block encoder interface *IC* allows the adaptation between the F*PGA* and the acquisition board to iniquity the rotor position of the *PMSM*;
- The *ADC* interface allows the connection between the *FPGA* and the analog-digital converter (*ADCS7476MSPS 12-bit A / D*) that interfaces two Hall Effect transducers for the stator currents machine acquisition;
- Block "*Timing*" which controls the synchronization between blocks, which allows the refresh in the voltages reference $V_{10}$, $V_{20}$ and $V_{30}$ at the beginning of each sampling period;
- The *RS232* block provide the signal timing and recovery of signals viewed, created by another program on Matlab & Simulink to visualize the desired output signal.

## 7. Experimental Set-up

To implementing the control system by Sliding mode Control  is it used a *XC3S500E Spartan3E*, *ADC* (analog to digital convertor) interface (*Fig.17*).

The control unit architecture ensures a control module for an *A/D* interface, an encoder interface and the control Sliding module. The *A/D* interface module and encoder interface are activated simultaneously at the beginning of each sampling period. Then, after a delay conversion from analog to digital conversion $t_{ADC}$, the control unit activates the control module indirect sliding mode. This module is controlled by its own control unit. First times, the Park transformation module will calculate the components of $i_{sd}$ and $i_{sq}$ ($t_{abc-dq}$). Then, when the processing module *abc-dq* indicates the end of its calculation, the estimation module of the *FEM* is activated, has to calculate $-\omega_{dq}\Phi_{sq}$ and $\omega_{dq}\Phi_{sd}$ . It is running for $t_{FEM}$ time. Then the $SM\_I_{sd}$ and $SM\_I_{sq}$ modules are enabled computing in parallel the tensions $U_{sd}^*$ and $U_{sq}^*$ ($t_{SM\_dq}$). Thereafter, when the modules indicate the end of the calculation, inverse Park transformation module is activated and calculates the reference voltages $U_{sa}^*$, $U_{sb}^*$ and $U_{sc}^*$ ($t_{qd-abc}$). After the *PWM* module is enabled. Latter has a computational time equal to $t_{PWM}$ and can calculate and refresh the reference voltages $V_{10}$, $V_{20}$ and $V_{30}$ which will be compared to a triangular carrier signals that generate control signals $C_1$, $C_2$ and $C_3$.

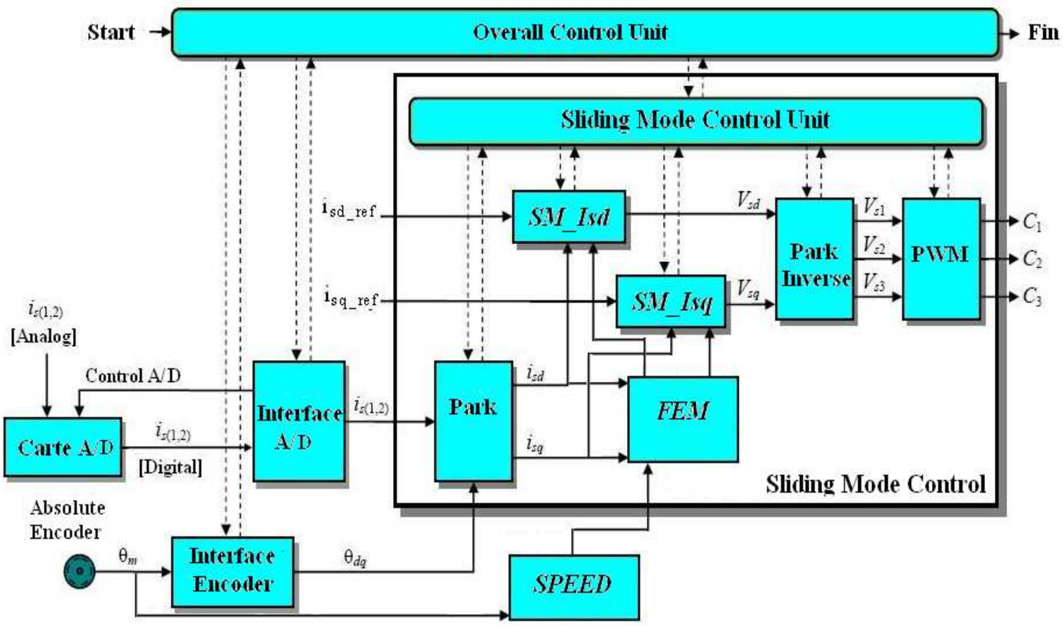



Fig.17: FPGA based hardware ISMC

The following table shows the performance of computing time and resource consumption, obtained during the control Sliding Mode architecture implementation. The resources consumed are obtained for a fixed point format *13/Q12*. The total computing time $t_{SMI}$, in command module is equal to *1.04µs*. By adding the analog to digital conversion time $t_{A/D}$, total time *Tex* architecture brought dives equals *3.48µs*.

| Module | Latency | Time Calculation |
|---|---|---|
| Interface A/D | 120 | $t_{A/D}$=2.4 µs |
| IC Interface | 2 | $t_{Cod}$=0.04 µs |
| Park | 16 | $t_{abc\text{-}dq}$=0.30 µs |
| FEM | 15 | $t_C$ = 0.24 µs |
| SM_$I_{sd}$ | 8 | $t_{SM\_dq}$ = 0.75 µs |
| Park-Inverse | 14 | tdq -abc=0.30 µs |
| SM_$I_{sq}$ | 18 | $t_{SM\_dq}$ = 0.75 µs |
| PWM | 5 | $t_{PWM}$ =0.014µs |
| $t_{SMI}$= $t_{abc\text{-}dq}$ + 2$t_{SM_dq}$ + $t_{dq\text{-}abc}$ + $t_{PWM}$ | | $t_{FOC}$= 1.04 µs |
| Run time $T_{ex}$=$T_{A/D}$ + $t_{SMI}$ | | $t_{ex}$ =3.48 µs |
| Resources Consumed | Number of Slices | 1344 de 5376 (25%) |
| | Wired Multipliers | 8de 16 (65%) |
| | Memory RAM | 7% |

Table1: FPGA Performance for ISMC

To test the controller, a prototyping platform for a Permanent magnet Synchronous Machine was assembled..

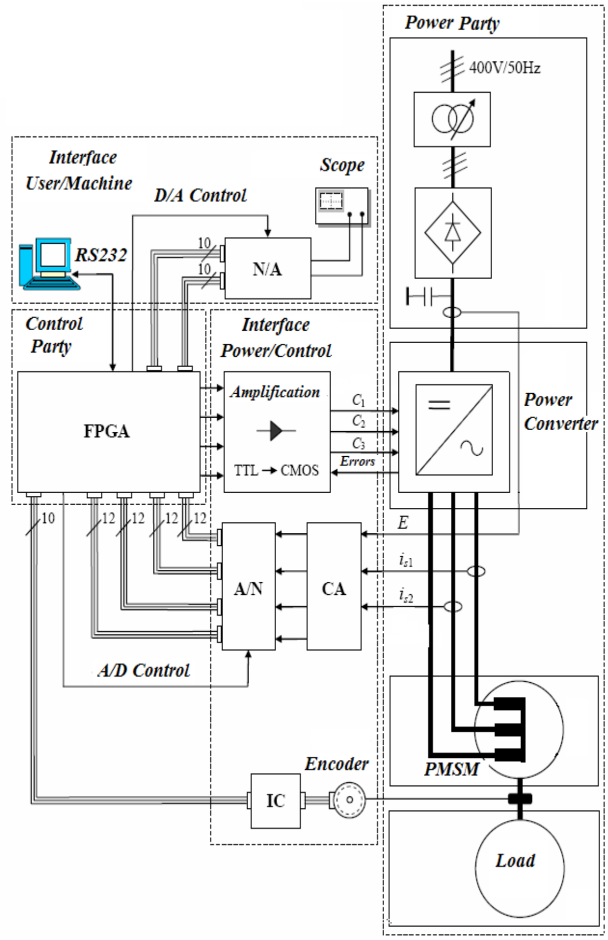



Fig.18: Experimental setup of the testbed

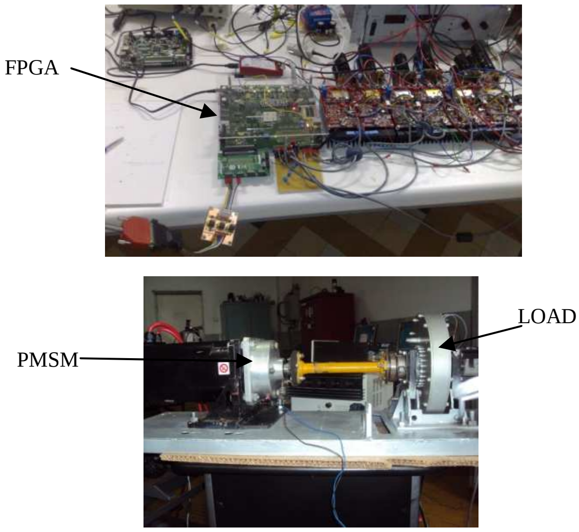



Fig.19: Prototyping platform control

The *Fig.20* show the experimental results obtained during the implementation of the Sliding Mode indirect control. It presents the control signals state for the switches of the inverter voltage in the area where there is the reference voltage vector. These results are similar to those presented in the theories. Furthermore, the control signals generated from the *FPGA* board will be filtered before being injected into the voltage inverter.

The above figures show that the phases are balanced and demonstrate the proper functioning of the *PWM*.

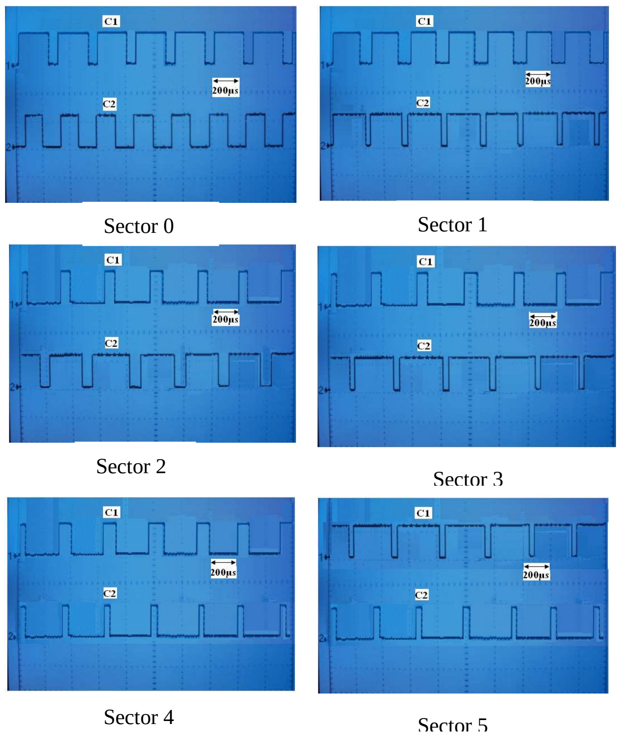



Fig.20: Switching states of control signals $C_1$ and $C_2$

The *Fig.20* shows that control system satisfy the basic requirements of the control strategy and validate therefore the good functionality of the system. In fact, It can be noted that:

- The switching frequency is limited to the sampling frequency of the control algorithm to guarantee safe operation of the semiconductor power devices.
- The switching frequency increases weakly when the stator current vector magnitude decreases.

The indirect sliding mode control is synthesized using the sliding mode theory. In this case, a reference voltage vector is applied to the machine. This voltage vector is composed by a vector voltage equivalent valid on the sliding surface and a vector attraction voltage valid outside the sliding surface (transient). The application of the vector reference voltage to *PMSM* requires an intermediate stage of pulse width modulation. The switching frequency is fixed equal to the frequency of the *PWM*.

The indirect control by sliding mode ensures better quality control currents in steady state with a considerable reduction of the oscillations.

The implementation of the indirect control by sliding mode on *FPGA* devices is characterized by a reduced operation time.

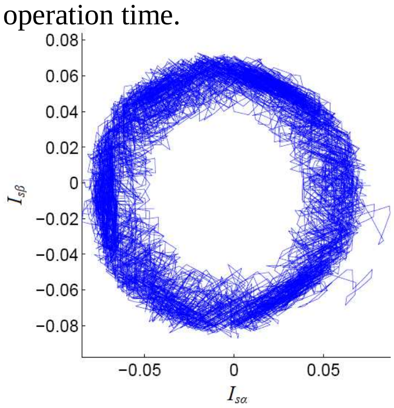



Fig.21: Stator current locus for *ISMC*

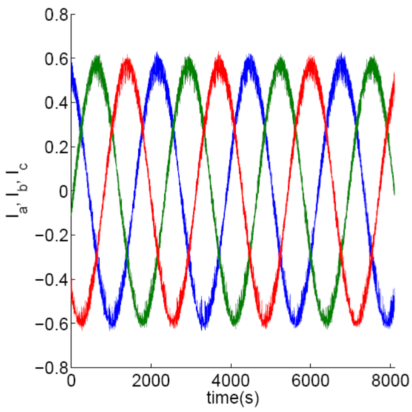



Fig.22: *abc*-axis current in the *PMSM*

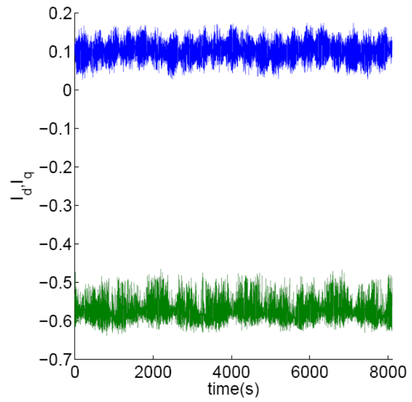



Fig.23: *d*-axis and *q*-axis current in the *PMSM*

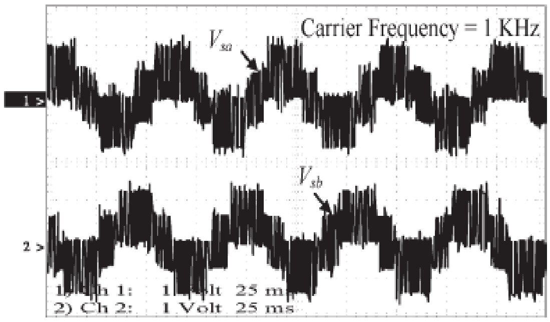



Fig.24: the *a*-axis and *b*-axis voltage stator

In figures 21, 22, 23 and 24 the experimental results of Indirect Sliding Mode PMSM with the FPGA platform are shown. Update frequency for this implementation is 20kHz. All results were extracted from the *FPGA* by the ChipScope tool of Xilinx.

This figures show that control system satisfies the basic requirements of the control strategy and validates therefore the good functionality of the system. In fact, It can be noted that:

- The switching frequency is limited to the sampling frequency of the control algorithm to guarantee safe operation of the semiconductor power devices.
- The switching frequency increases weakly when the stator current vector magnitude decreases.
- Implementing the *ISMC* control in *FPGA* has the drawbacks:
- The switching frequency is variable. It is limited to half the sampling frequency of the control algorithm and maximum at very low speed.
- The zero voltage vectors are not applied.

## 8. Conclusion

In the case of a Sliding mode controlled by current stator of permanent magnet synchronous machine, it is required the use of the PWM technique. This paper presents the implementation of Sliding Mode Control architecture on *FPGA* for Permanent Magnet Synchronous Machine (*PMSM*). The development of the corresponding design has rigorously followed an appropriate methodology which offers considerable advantages and allows the creation of a library for optimized reusable modules.

Among the advantages of this control structures, the switching frequency is fixed and there is compliance with the eight vector voltages that can provide the voltage inverter. However, it has disadvantages because the general structure of the control algorithm is complex to implement and parameters of the control algorithm depend on the sampling period.

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