Impact of MOSFET's performance on its threshold voltage and its influence on design of MOS inverters

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Abstract: The aim of this paper is to research the impact of physical parameters which characterize the MOSFET transistors structure on the threshold voltage values and its influence on critical voltage values which characterize digital circuits that contain the MOSFET transistors. The results obtained emphasize the impact of each single physical parameter on the total value of the threshold voltage. By adjusting the values of MOSFET physical parameters the accepted threshold voltage can be achieved. Since the threshold voltage will have influence on critical voltage values which characterise MOS inverters and delay times during transfer logic states between stages, it must be taken into consideration during design phase of logic gates that contain the MOSFET transistors.

Key words: Threshold Voltage, MOSFET Parameters, Enhancement-Type NMOS, Impurities, Doped Density, Short-Channel, Narrow-Channel, Voltage Level, Propagation Delay, Critical Values.

1 Introduction

The important value which characterizes the MOSFET transistors is the value of threshold voltage, which can be positive and negative according to the MOSFET type. This value can be controlled during the fabrication process of MOSFET transistors. The physical structure of n-channel enhancement-type MOSFET (or NMOS) is represented in Fig.1. Because the enhancement-type NMOS have advantage over other type of MOSFET transistors, in the following we will focus on this analysis. Terminals of MOSFET transistors are indicated with S (source), D (drain), G (gate) and B (body).

The value of the gate-to-source voltage V_{GS} needed to create (induced) the conducting channel (to cause surface inversion) is called the threshold voltage (V_{th} or V_t). The value of the threshold voltage is dependent from some physical parameters which characterize the MOSFET structure such as: the gate material, the thickness of oxide layer t_{ox}, substrate doping concentrations (density) N_A, oxide–interface fixed charge concentrations (density) N_{ox}, channel length L, channel width W and the bias voltage V_{SB} [1, 2, 5].

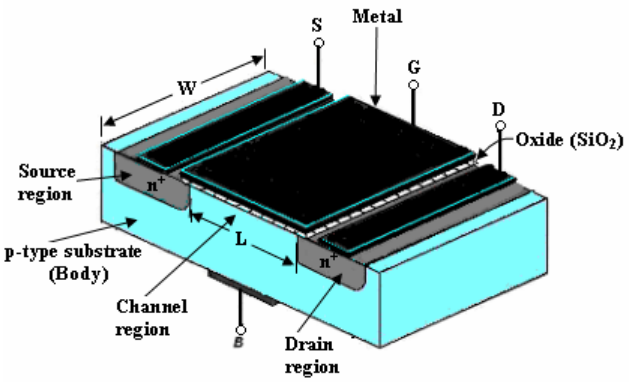


Fig. 1 The physical structure of an n-channel enhancement-type MOSFET in perspective view.

2 The threshold voltage on MOSFET-transistors

2.1 The threshold voltage of NMOS-transistors with long-channel

To calculate the threshold voltage we must consider physical parameters of MOSFET structure which have the impact in value of the threshold voltage by considering the various components of V_t (when V_{SB} =0V, the threshold voltage will indicate V_{t0}) [2]:

$$V_{t0} = \Phi_{GC} - 2\phi - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (1)$$

For nonzero substrate bias voltage ($V_{SB} > 0$), now the generalized form of threshold voltage will be [2]:

$$V_t = V_{t0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \quad (2)$$

where:
γ- is the body-effect parameter.
ϕ_F - the substrate Fermi potential.

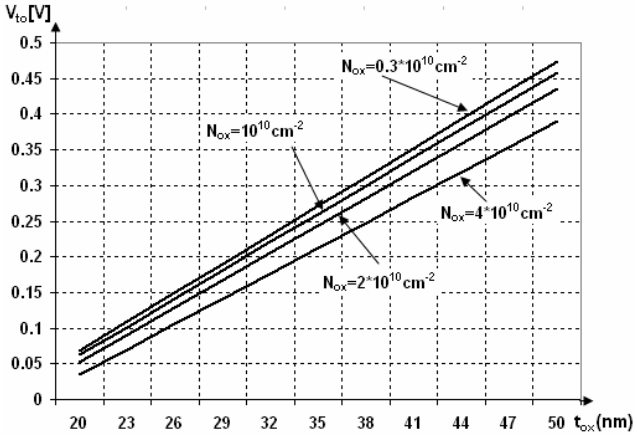


Fig. 2 The dependence of the threshold voltage V_{t0} on thickness of oxide layer t_{ox} for parametric values of oxide-interface fixed charge density N_{ox}, when N_A = 10^{16}cm^{-3}.

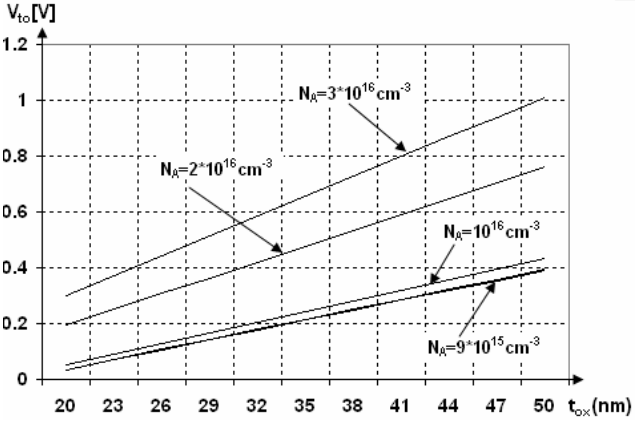


Fig. 3 The dependence of the threshold voltage V_{t0} on thickness of oxide layer t_{ox} for parametric values of substrate doping density N_A, when N_{ox} = 2*10^{10}cm^{-2}.

The influence of t_{ox}, N_A and N_{ox} in values of threshold voltage is shown in Fig.2 and Fig.3. For larger value of each parameter: $t_{ox,}$ or N_A the value of threshold voltage will increase. But, for larger value of N_{ox} the value of threshold voltage will decrease, which is not significant.

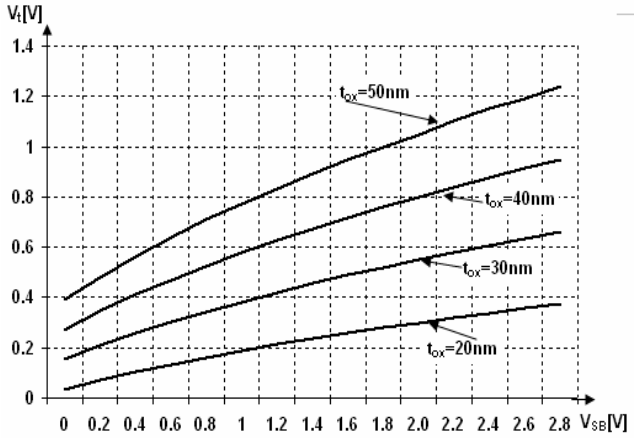


Fig.4 Variation of the threshold voltage V_t as a function of the source-to-substrate (V_{SB}) voltage for parametric values of thickness oxide layers t_{ox}, when N_A = 10^{16} cm^{-3} and N_{ox} = 4*10^{10} cm^{-2}.

Fig. 4 shows dependence of threshold voltage on the polarization voltage V_{SB}, which results in the higher values of the threshold voltage for higher value of V_{SB} compared with V_{t0} (as in case of integrated circuits).

The threshold voltage (V_t) can be adjusted by selective dopant ion implantation into the channel region of the MOSFET transistors during fabrication processes. For n-channel MOSFETs, the threshold voltage will increase by adding extra p-type impurities (acceptor ions) into the cannel region. The threshold voltage of the n-channel MOSFET can be decreased by implanting n-type impurities (dopant ions) into the channel regions. As result of the extra implanting of the type impurities, the threshold voltage will be shifted by a component (Δ_{tI}) which described:

$$\Delta V_{tI} = qN_I / C_{ox} \quad (3)$$

where:
N_I - is density of implanted impurities into the channel region [cm^{-2}].
Now the threshold voltage will be as:

$$V_{tI} = V_t \pm |\Delta V_{tI}| \quad (4)$$

The implanted impurities into the channel region will have an irrelevant effect on substrate Fermi potential.

Fig.5 shows the dependence of the threshold voltage V_{t0} on extra p-type impurities which is added into the channel region.

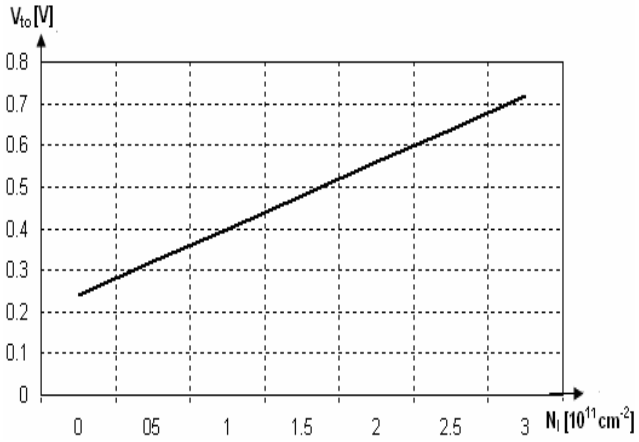


Fig.5 Variation of the threshold voltage V_t as a function of the concentration impurities N_I, when t_{ox}=35nm, N_A = 10^{16} cm^{-3} and N_{ox} = 4*10^{10} cm^{-2} and V_{SB} = 0V.

2.2 The threshold voltage of NMOS-transistors with short-channel

When NMOS is defined as a short-channel device the length of channel it will have impact on the threshold voltage. A short-channel will reduce the threshold voltage of ΔV_t compare with long-channel device [2, 5, 9].

$$V_{t0}\,(\text{short-channel}) = V_{t0} - \Delta V_{t0} \qquad (5)$$

The amount of threshold voltage reduction ΔV_{t0} can be found as [2, 5]:

$$\Delta V_{t0} = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{Si}N_A\left|-2\phi_f\right|}\,\frac{x_j}{2L}\left[\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)\right] \qquad (6)$$

x_j-junction depth of drain (source) region,
x_{dS}, x_{dD} represent the depth of depletion regions at source and drain as results of pn junction, respectively.

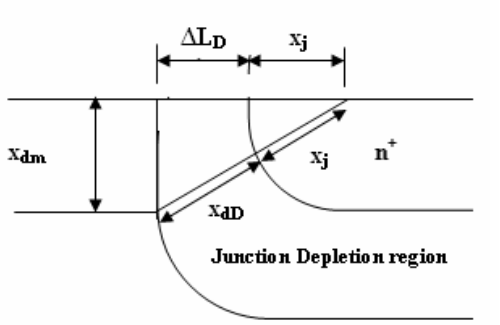


Fig.6 Simplified geometry of the MOSFET channel region. Close-up view of the drain diffusion edge.

Influence of the length channel L, the depth x_j of drain (source) regions and drain-to-source voltage (V_{DS}) on the voltage term $\Delta V_{t0,}$ are shown in Fig.7, Fig.8.

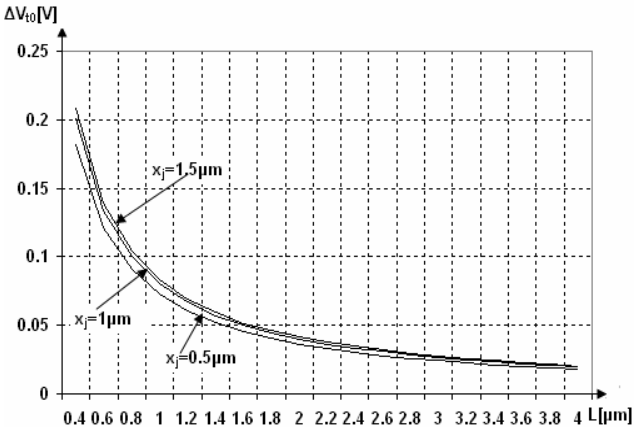


Fig.7 The dependence of the ΔV_{t0} on the length L for parametric values of depth x_j, when N_A = 10^{16} cm^{-3}, N_D = 10^{19} cm^{-3}, t_{ox} = 20 nm and V_{DS} = 0V.

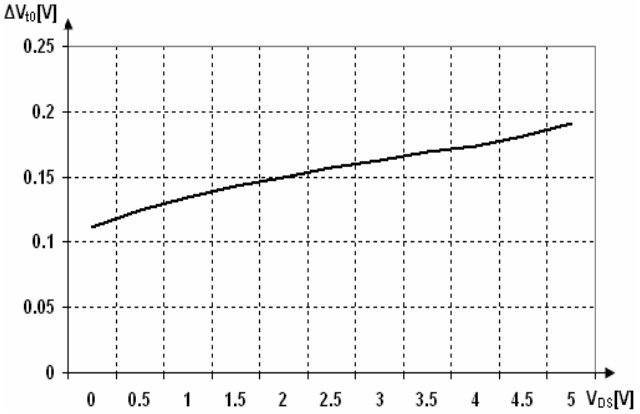


Fig.8 The dependence of ΔV_{t0} on V_{DS} voltage, when N_A = 10^{16} cm^{-3}, N_D = 10^{18} cm^{-3}, t_{ox} = 20 nm, x_j = 1 μm and L = 0.7 μm.

Obtained values are represented in Fig.7 and Fig.8. For $L \approx x_j$ the ΔV_{t0} will have influence in reduction of the threshold voltage V_{t0}. While if $L >> x_j$ the ΔV_{t0} is not significant, the NMOS is defined as long-channel device. The V_{DS} voltage will have significant influence in the term ΔV_{t0}, which results in larger value for higher value of V_{DS}.

2.3 The threshold voltage of NMOS with narrow-channel

When MOSFET transistor is defined as a narrow-channel device, the channel will have influence in the threshold voltage and results in higher value for ΔV_{t0} if compared with long-channel device [1, 2, 5].

$$V_{t0(\text{narrow-channel})} = V_{t0} + \Delta V_{t0} \quad (7)$$

The voltage term ΔV_{t0} can calculate with expression:

$$\Delta V_{t0} = \frac{1}{C_{ox}} \sqrt{2q\varepsilon_{Si} N_A \left| -2\phi_f \right|} \frac{\pi \cdot x_{dm}}{2W} \quad (8)$$

In Fig.9 is shown the dependence of voltage term ΔV_t on the channel width and we can say: when $W \approx x_{dm}$ the ΔV_t term will have influence in the increase of the total threshold voltage, while $W >> x_{dm}$ the ΔV_t term is not significant.

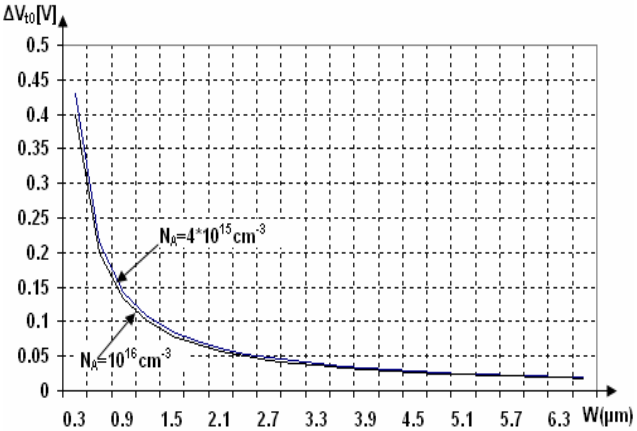


Fig.9 The dependence of ΔV_{t0} on channel width (W) for parametric values of N_A, when $N_D = 10^{18}$ cm^{-3} and $t_{ox} = 20$ nm.

Calculation of threshold voltage of a p-channel enhancement-p type MOSFET (PMOS) is same as in NMOS, but the voltage components will have reverse polarization, therefore the threshold voltage will be negative [3]. The PMOS transistors are slower then NMOS transistors for identical dimensions and in same applications use as loads.

The values obtained will help to determine the dimensions of MOS transistors and will have the approximate values of threshold voltage. The nominal value and the statistical range of the threshold voltage for any MOS process are ultimately determined by direct measurements.

3 Influence of threshold voltage on critical voltage values and delay times in MOS inverters and pass-transistor logic

In many applications such as MOS inverters, pass-transistor logic circuits, dynamic pass-transistor logic circuits, semiconductor memories and other applications, the NMOS and PMOS transistors are used in order to implement switches. The threshold voltage V_t will have influence on: maximum input voltage which can be interpreted as logic "0" (V_{IL}), minimum input voltage which can be interpreted as logic "1" (V_{IH}), minimum output voltage when the output level is logic "0" (V_{OL}), maximum output voltage when the output level is logic "1", static current (I_{stat}), linear resistance (r_{DS}) in triode region, finite output resistance on saturation (r_o), noise margin (NM) and propagation delay [2, 4].

3.1 Influence of threshold voltage on critical voltage values and delay times in pass-transistor logic

The MOS transistors in pass- transistor logic circuits used to transfer logic state between input and output nodes. During logic "1" transfer and "0" transfer the threshold voltage will have impact on level of output voltage and delay times. In Fig.10 is illustrated the logic "1" transfer with an NMOS.

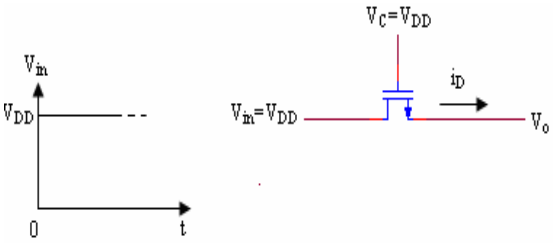


Fig.10 The logic "1" transfer with an NMOS.

After analysis we will have:

$$V_{OH}=V_{DD}-V_t \quad (9)$$

Fig. 11, Fig. 12 and Fig.13 shows the impact values of the threshold voltage in reduction level of output voltage (V_{OH}) which represents high logic level.

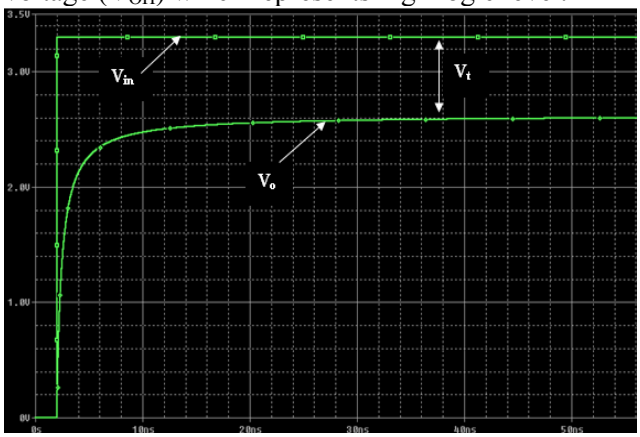


Fig.11 The reduction of high output voltage level (V_{OH}) by threshold voltage ("poor 1"), when V_{t0}=0.2V.

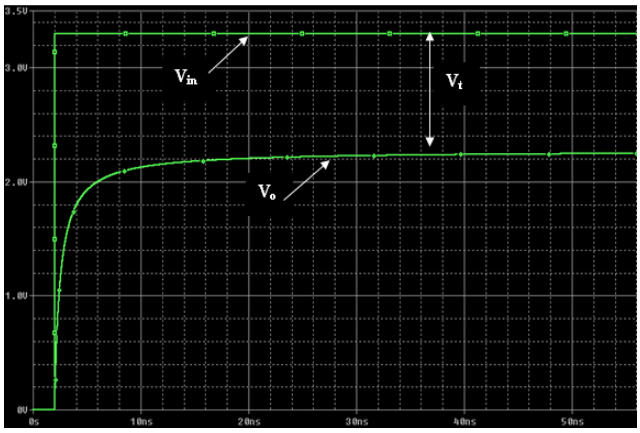


Fig.12 The reduction of high output voltage level by threshold voltage ("poor 1"), when V_{t0}=0.6V.

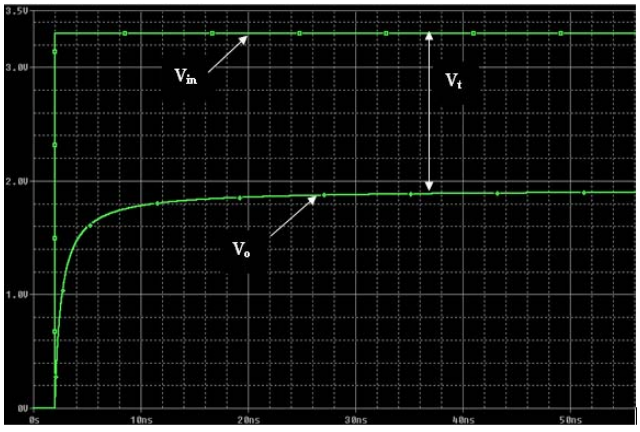


Fig.13 The reduction of high output voltage level by threshold voltage ("poor 1"), when V_{t0}=1V.

The fact that output voltage level will reduce based on threshold voltage, will have significant implication for circuit design. Thus the output voltage introduces the "poor 1". Hence, we can reduce the loss output voltage level by using a lower the threshold voltage for NMOS transistors, and we can eliminate the loss altogether by using NMOS transistors with zero-threshold voltage (V_t=0V). The zero-threshold voltage devices can be fabricated by using ion implantation (impurities) to control the values of the threshold voltage and are known as natural devices.

The threshold voltage will have influence on propagation delay (t_{PLH}) during logic "1" transfers, where for larger value of threshold voltage V_t the propagation delay (or time rise) will increase, because linear resistance in triode region and finite resistance in saturation region of channel region is dependent too from level of the threshold voltage. The amount of current which flows into channel during logic "1" transfer and time constants is dependent from these resistances.

For logic "0" transfer the threshold voltage will have no influence at output voltage which represent the low voltage level (it will be V_o=0V, or "good 0"), but will have influence in propagation delay (time falls), see Fig.14 and Fig 15. For lower value of the threshold voltage the value of propagation delay (t_{PHL}) will be lower.

The dependence of NMOS channel resistance on the threshold voltage for two regions will be as:

$$r_{DS} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_t)} \qquad (10)$$

r_{DS} - is resistance of channel in triode region.

k_n - is process transconductance parameter.

L- is length of channel region.

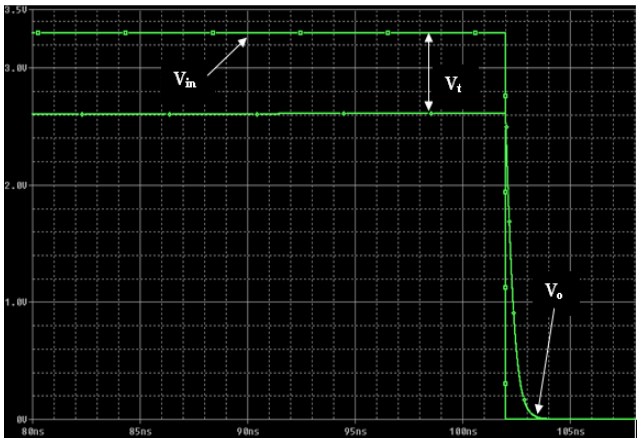
W- is width of channel region.

$$r_o = \frac{1}{\lambda \frac{k_n'}{2} \frac{W}{L}(V_{GS} - V_t)^2} \qquad (11)$$

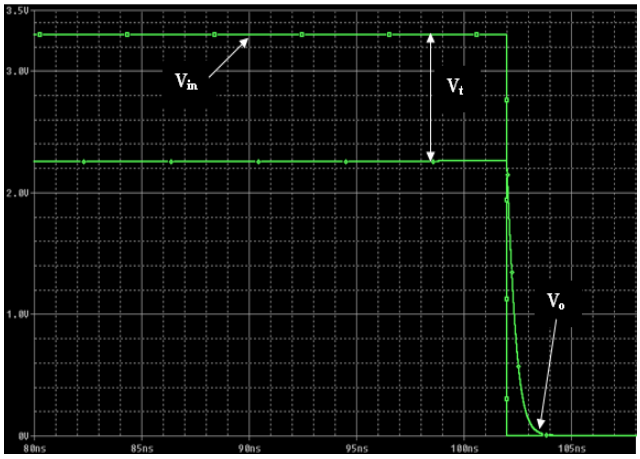
r_o - is resistance of channel in saturation region.

λ - is a process technology parameter.

The variation the NMOS channel resistance on values of the threshold voltage when the device is in triode region of operation is represented in Fig. 16.



Fg. 14 Waveform of output voltage V_o for logic "0" transfer with one pass-transistor, when V_{t0}=0.2V.



Fg. 15 Waveform of output voltage V_o for logic "0" transfer with one pass-transistor, when V_{t0}=0.6V.

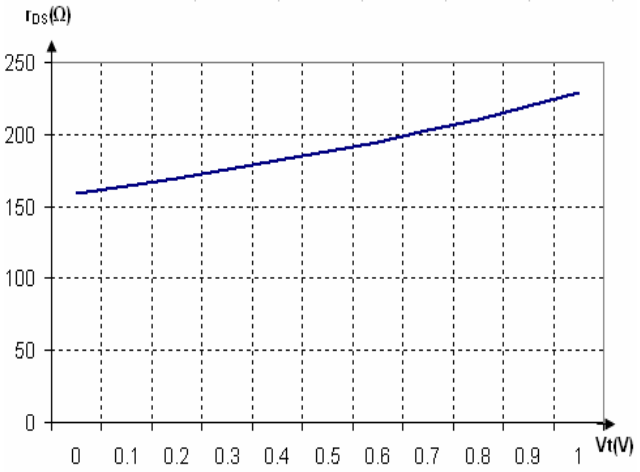


Fig.16 The variation of drain to source (channel) resistance of NMOS in triode region operation on values of the threshold voltage, when $k_n^{'} = 190\mu A/V^2$, $W/L=10$ and V_{GS}=3.3V.

For larger values of the threshold voltage will have larger values of resistance into channel (resistance of drain to source terminals) and resulting lower values of drain current.

The variation of NMOS channel resistance on values of the threshold voltage when the device is in saturation region of operation is represented in Fig. 17. Based on obtained values we will see that for larger values of the threshold voltage the resistance between source and drain (or channel) will have larger values. The values of channel resistance when NMOS device is in saturation region of operation are more larger then values of resistances when NMOS device is in triode region of operation for same values of the threshold voltage. These values will have influence on amount drain current, resulting in lower value for higher values of channel resistance. The drain current determines the charge and discharge time of the parasitic capacitances that are present in device and loads.

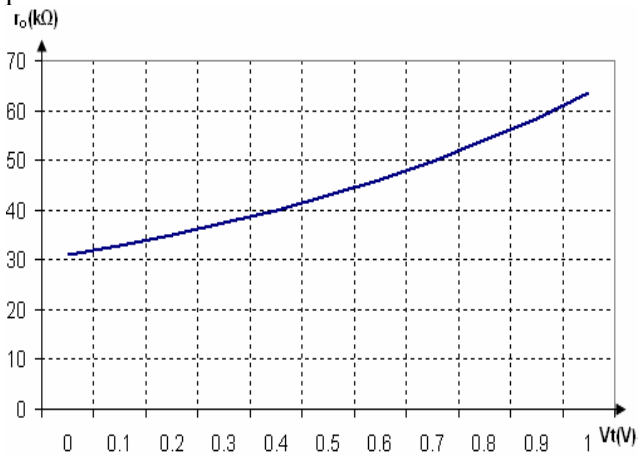


Fig.17 The variation of drain to source resistance of NMOS in saturation region operation on values of the threshold voltage, when $k_n^{'} = 190\mu A/V^2$, $W/L=10$, V_{GS}=3.3V and $\lambda = 0.0312$.

Now consider the following case in which will have three identical pass-transistors connected in series (in cascades) as in Fig. 18.

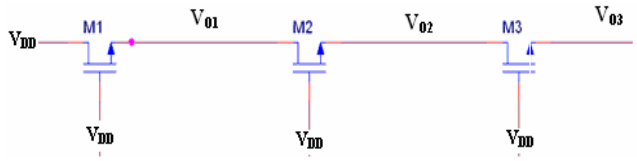


Fig. 18 Three identical pass-transistors connected in series.

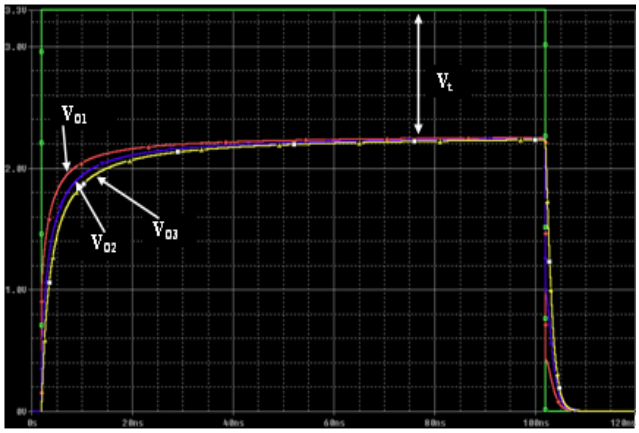


Fig. 19 Waveforms of outputs voltages when three pass-transistors connected in series, when V_{t0}=0.6V.

Output voltage of which internal node will reduce according to V_t (by itself threshold voltage of pass-transistors, independently of number the pass-transistors that are connection in series) and propagation voltage will increase from stage to stage. Now, we will consider different case in which the output of each pass-transistor drives the gate of another pass-transistor, as depicted in Fig.20.

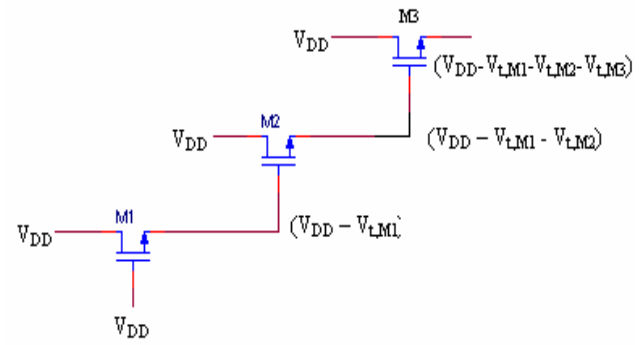


Fig. 20 The logic "1" transfers when one pass-transistor is driving another pass-transistor (node voltages during the "1" transfer).

After analysis, Fig.21 shows that the output voltage level will reduce by sum of the threshold voltage of each pass-transistor. It can be seen that, each stage in this case causes a significant loss of voltage level.

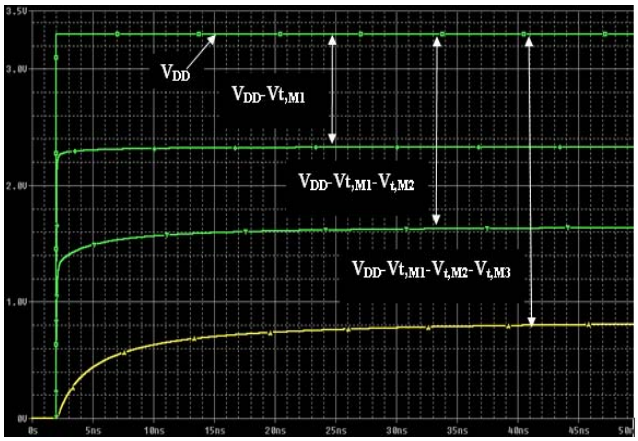


Fig.21 Waveform of outputs voltages V_o for logic "1" transfer, when each pass-transistor (NMOS) is driving another pass-transistor (NMOS) and V_{t0} = 0.6V.

3.2 Influence of threshold voltage on critical voltage values and delay times in CMOS inverters

The threshold voltage will have influence on critical voltages values which characterize MOS inverters and voltage transfer characteristic. The impact of V_t on critical voltages values for a symmetric CMOS inverters are represented in below diagrams (for supply voltage V_{DD}=3.3V) Fig. 22, Fig. 23, Fig. 24 and Fig. 25.

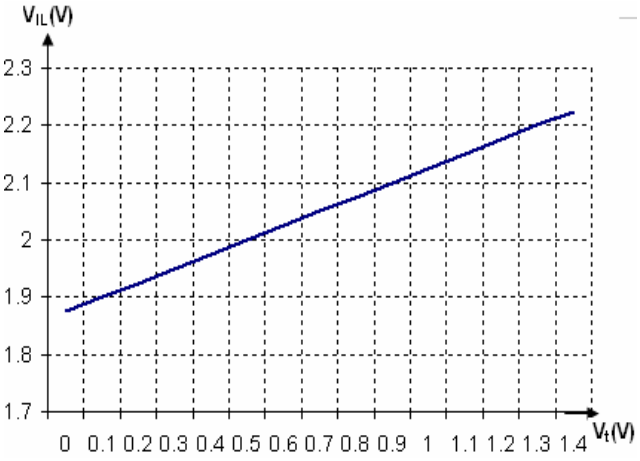


Fig.22 Variation of V_{IL} (maximum input voltage which can be interpreted as logic "0") as function of the threshold voltage V_t.

Fig. 23 Variation of V_{IH} (minimum input voltage which can be interpreted as logic "1") as function of the threshold voltage V_t.

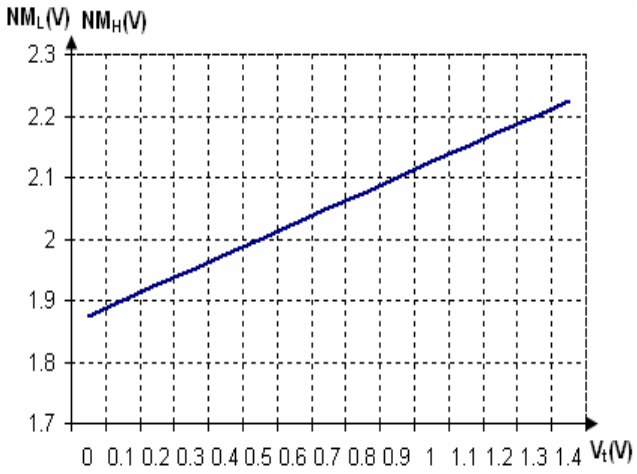


Fig. 24 Variation of noise margin MN (NM_L-noise margin for low logic level, NM_H-noise margin for high logic level) as function of the threshold voltage V_t.

In symmetric case on CMOS inverters the noise margins for two levels are equal NM_L=NM_H.
The voltage value V_{IL} will increase for higher value of threshold, while V_{IH} will decrease for higher value of threshold voltage. The noise margins (NM) for two levels (NM_L and NM_H) will increase for higher values of threshold voltage.

For higher value of threshold voltage the propagation delay will increase and this variation is presented in Fig. 24. Moreover, the threshold voltages determine minimum level of supply voltage on CMOS inverters, which will continue to operate correctly [2].

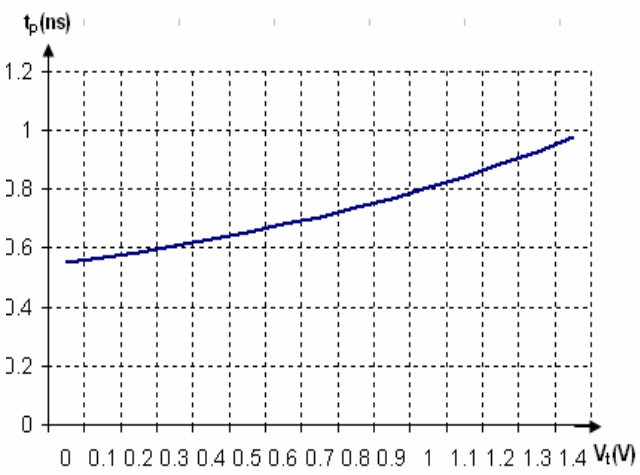


Fig. 25 Variation of propagation delay t_P as function of the threshold voltage V_t

3.3 Influence of threshold voltage on critical voltage values and delay times in pseudo-NMOS inverters

In many applications in digital circuits use pseudo-NMOS gate, based on pseudo-NMOS inverter. The threshold voltage will have impact on critical values which characterize pseudo-NMOS inverter, as: V_M (the threshold voltage of pseudo-NMOS inverters), V_{OL}, V_{IL}, V_{IH}, static current in the low-output state (I_{stat}), noise margin (NM) and propagation delay.

Variations of these parameters on threshold voltage are represented in below diagrams by Fig. 26, Fig. 27, Fig. Fig 28, Fig. 29, Fig. 30, Fig. 31 and Fig. 32 (when r=9, V_{DD}=3.3V, V_{tn}=-V_{tp}).
r-is ratio of transconductance parameters of the device (NMOS and PMOS transistors).
For higher value of the threshold voltage of MOS transistors will have higher values of the threshold voltage (V_{th}) and will increase values V_{IL}, V_{IH} and NM_L of pseudo-NMOS inverters. But, will have decrease of the values V_{OL}, NM_H and I_{stat} when the threshold voltage V_t take the higher values.

The impact of the threshold voltage on propagation delays in pseudo- NMOS inverters will be same as in CMOS inverters. But, in pseudo-NMOS inverters propagation delays are asymmetric (t_{PHL}>t_{PLH} or t_{PHL} will be r times larger than t_{PLH}).

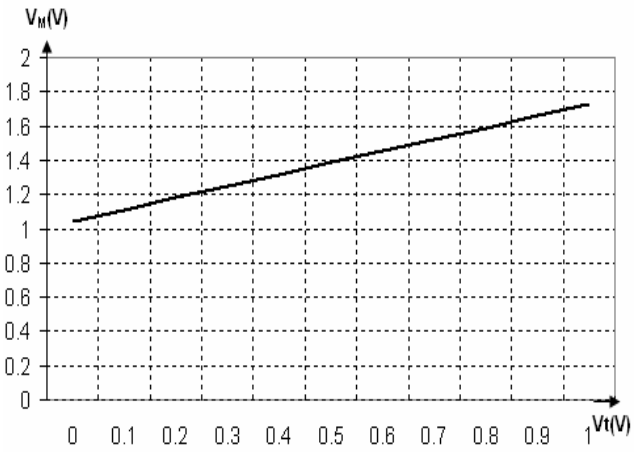


Fig. 26 Variation of the threshold voltage of pseudo-NMOS inverter (V_M) as function of the threshold voltage V_t.

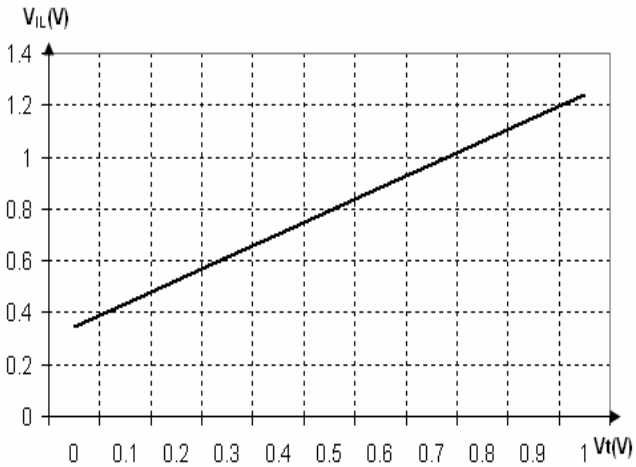


Fig. 27 Variation of the V_{IL} of pseudo-NMOS inverter as function of the threshold voltage V_t.

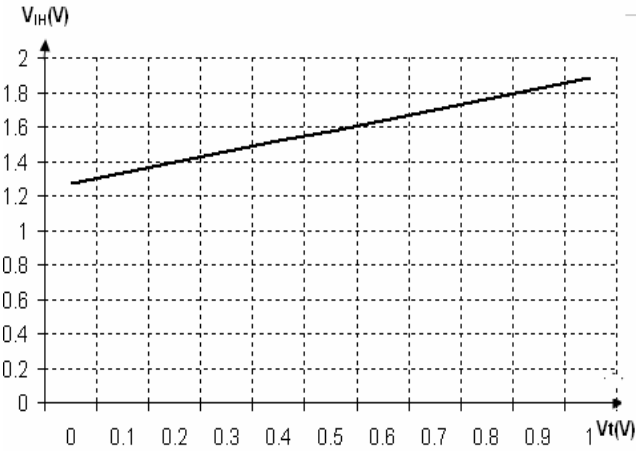


Fig. 28 Variation the V_{IH} of pseudo-NMOS inverter as function of the threshold voltage

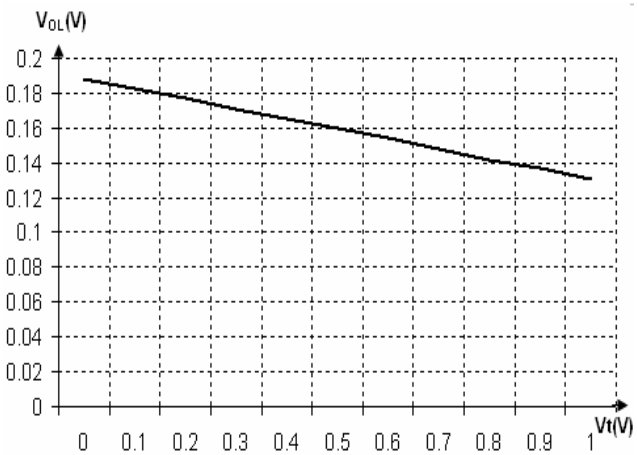


Fig. 29 Variation of the V_{OL} of pseudo-NMOS inverter as function of the threshold voltage V_t.

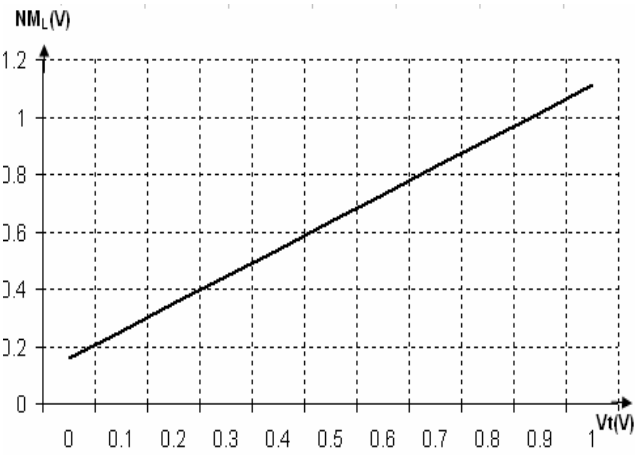


Fig. 30 Variation the NM_L of pseudo-NMOS inverter as function of the threshold voltage V_t.

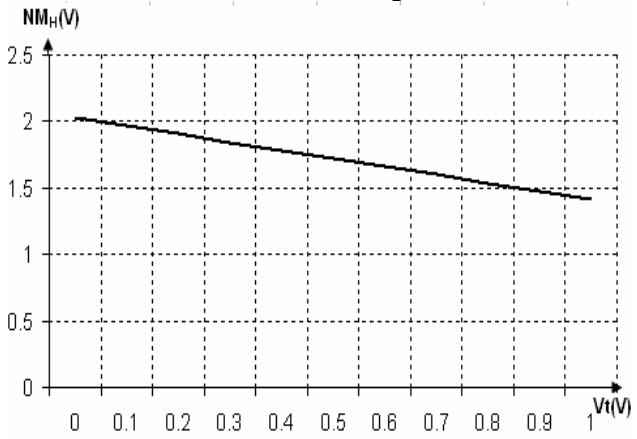


Fig. 31 Variation the NM_H of pseudo-NMOS inverter as function of the threshold voltage

The value of static current I_{stat} will have influence on static power dissipation, therefore this value mast be lower, Fig. 32.

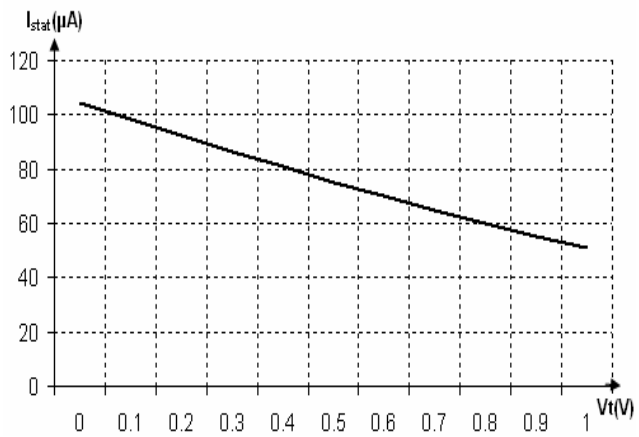


Fig. 32 Variation the I_{stat} of pseudo-NMOS inverter as function of the threshold voltage

4 Conclusion

Based on the results obtained, as shown in figures (2-9), we have seen the impact of several physical parameters which characterize the MOSFET transistors (NMOS) on the threshold voltage, which mast take in consideration during fabrication faze. Therefore, it can be concluded that for long-channel device the threshold voltage will decrease when: the substrate doping (N_A) decreases, the oxide thickness (t_{ox}) decreases, the oxide-interface charge (N_{ox}) increases (but, will have little effect). For short-channel device we will have reduction of the threshold voltage by ΔV_t term compared with the long-channel device, which depends of: the length of channel (L), the junction depth (x_j), drain diffusion doping (small effect) and drain-to-source voltage (V_{DS}). For narrow-channel device the threshold voltage will increase by ΔV_t term compared with the long-channel device, which is dependent of: the width channel (W), the maximal depletion region thickness (x_{dm}). The positive source-to-substrate voltage V_{SB} (body effect, as in IC) will cause the increment on total value of threshold voltage. For MOSFETs which have a small channel length and a small channel width, the threshold voltage variations due to short- and narrow-channel effects may tend to cancel each other out. Also, in pass-transistors logic (PTL) the threshold voltage will reduce level of output voltage during the logic "1" transfer by according the Vt, the propagation delay during transfers logic states will increase for higher value of V_t, hence the V_t must be lower but the device is more sensitive. The values of the threshold voltage will have significant influence on critical voltages values which characterise CMOS inverters and propagation delay, when for higher value of threshold voltage will have better noise margin (NM) for two logic levels and propagation delays will increase resulting in lower operation speed. In pseudo-NMOS inverters the higher threshold voltage values will results on better noise margin for low logic level, lower value of V_{OL} and static current resulting on lower static power dissipation. But, the higher value of the threshold voltage will decrease the noise margin for high logic level. The impact V_t on propagation delays in pseudo-NMOS inverters are same as in CMOS inverters, but are asymmetric.

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