DSP-Based Two-Synchronized Motors Control System Using External FPGA Design

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Abstract: There are many applications that have more than one motor to be controlled dependently to execute the same task or independently to execute different tasks at the same time with high performance low cost control system. This paper presents a Two-Synchronized Motors Control System Using External FPGA Design with high performance and low cost for a variety of applications. The proposed technique is DSP and FPGA based system. An external FPGA structural design is interfaced with the PWM Generation Unit of the D SP board for the use of Two-Motor Control using one DSP Processor. The system is implemented using the Analog Devices Blackfin™ ADSP-BF561 dual core Digital Signal Processor (DSP). Core 1 is dedicated to implement the motor one control algorithm while core 2 mainly implements the motor two control algorithm with one PWM Generation Unit to reduce the overall cost and complexity of the motors control system. The FPGA design is implemented using VHDL language and downloaded successfully to the XILINX VERTEX-E FPGA. The FPGA board is then interfaced successfully with the ADSP PWM Unit. Simulation and experimental results are achieved successfully and introduced in this paper.

Key-Words: - Blackfin ADSP-BF561, FPGA, Two Motors Control.

1 Introduction

In so many applications there is a need to control more than one motor at the same time either dependently or independently, such as two-wheel mobile robot that has two-independently motors [1], [2]. It is difficult and costly to use DSP board for each motor to be controlled. It is better and easier to use only one DSP board with one PWM Generation Unit, to control more than one motor concurrently.

The DSP EZ-kit Lite board contains one three phase16-bit PWM Generation Unit, [3], [4]. The DSP board especially designed for motion control [5] but, only one three phase motor can be connected to the board to be controlled because it has only one PWM Unit with six output signals that is required for high-low switching of three-phase motor, like three-phase brushless DC motor.

Therefore, there is a need for a design to be interfaced with the DSP PWM Unit for two motors control that reach for (N) number of motors. Thus, a dedicated FPGA Buffering design is introduced in this paper. The FPGA design is simulated and downloaded successfully to the XILINX boards VERTEX-E. The FPGA board is then interfaced successfully with the DSP PWM Unit.

This paper introduces Two Motors Control System in section II, section III presents the FPGA Design Implementation, section IV presents Two Motor Control Implementation, section V gives Simulation Results and experimental results are introduced in section VI and Conclusions in section VII.

2 Two Motors Control System

In motion control, there are many applications that have two motors to be controlled at the same time either dependently to implement the same task or independently to implement different tasks. For example, mobile robots that have two wheels can be considered as Two Motors Control System (TMCS). In case of two-wheel mobile robot, which has two independently controlled motors, each motor needs its own controller to implement its own task, [1], [2], [6], [7].

Recently, most of motion control units have the ability to control only one motor. Thus, in case of

two motors control there is a need to use a control unit for each motor to be controlled. After that, all control units can be connected together to control two motors in synchronization, [8], [9]. But, this technique complicates the control system and makes it costly.

Therefore, there is a need for a design to control two motors using only one control unit with one PWM Generation Unit. Thus, an FPGA Structural Design is introduced to do so. The FPGA design is a sort of two buffers design that can be interfaced with the DSP board PWM Unit. The design has the same input (6-bit) and two outputs (6-bit each) equal to the number of motors to be controlled. A sort of control logic (CS) is used to switch between buffers to choose which buffer needs to be updated. This concept is described in the block diagram shown in Fig.1 below.

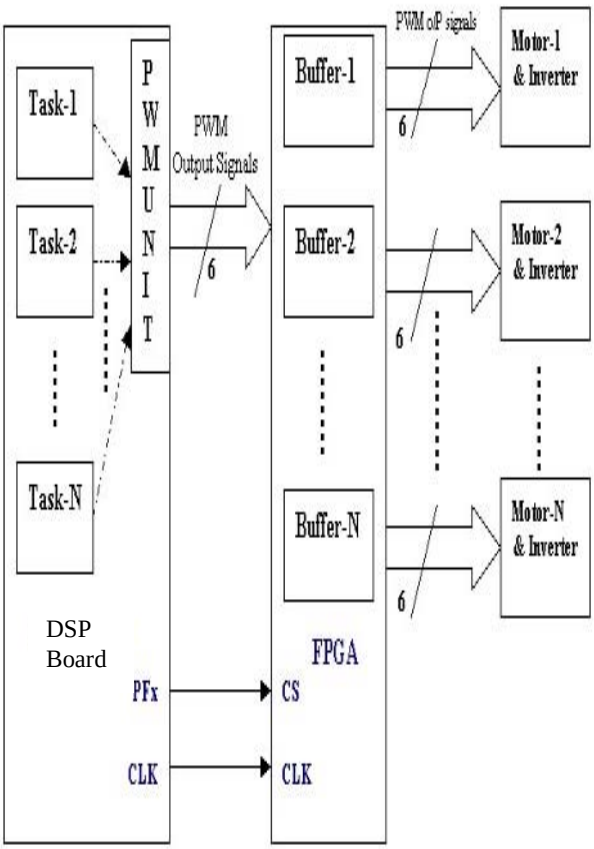


Fig.1. (DSP-FPGA) Two Motors Control System.

The (DSP-FPGA) based two motors control system shown in Fig.1 above is composed of:

- The DSP Processor executes motors control algorithms (Blackfin™ ADSP-BF561).
- The FPGA block contains the two buffers design interfaced with the PWM Unit of the DSP board.
- Inverters supply the power to each motor.
- Sensors (such as: current, speed, position, etc.).
- Motors (such as: three-phase BLDC Motors).

The FPGA Two Buffers design is implemented using VHDL language and XILINX (ISE) project navigator software, [10]. Then, the design is downloaded to the FPGA VERTIX-E XILINX board [11], which is interfaced with the DSP board PWM Unit. Each motor's inverter is connected to its own output buffer. The (CS), is connected to a DSP toggled I/O Pin and the design Clock is connected to the DSP Clock.

Fig.1 above shows that; (N) number of motors can be controlled using this structural design. Besides the complexity of control algorithms, there are some factors that limit the maximum number, (N), of controlled motors. These factors are:

- DSP Processor Core Clock (CLK).
- Number of Cycles that each motor needs, or how many cycles does each motor task need to be implemented?
- Updating time for each Motor.
- Number of FPGA board I/O Pins.

With commercially available high performance DSPs like Blackfin™ ADSP-BF561, that has one on board PWM Generation Unit and the power to control only one motor, the system can be developed to control more than one motor in synchronization using single DSP processor and one PWM Unit by interfacing the FPGA buffering design with the DSP on board PWM Unit as shown in Fig.1 above.

The DSP processor with 160 MHZ Core Clock for example, (160 MIPS) [3], [4], can theoretically control up to 10 motors if each requires 16 MIPS using the above FPGA design. For more illustration:

The DSP Processor that has a Core Clock (CLK=160 MHZ and Cycle period = 6.25 ns). If each task, each motor control loop, needs (8000 Cycles) to be implemented, then, each Task will take (50 us = 50 000 ns).

From the aforementioned, if each motor needs (0.5ms = 500000 ns) to be updated, then the number (N) can be calculated for this case as the following:

0.5ms = 500000 ns, which has 500000/6.25 = 80 000 CLK Cycle. Each motor task needs 8000 cycles then: **N** = 80 000/8000 = **10 Motors**.

By using VERTEX-E XILINX FPGA board with (100 pins), it is possible to control up to N=10 motors. But, in this paper the discussion will be based on **N=2** independently BLDC motors with two different tasks to enhance two-wheel mobile robot.

3 FPGA Design Implementation

The FPGA design is implemented using VHDL Language. It is implemented to control two BLDC Motors to enhance two-wheel mobile robot using XILINX (ISE) Software as shown in Fig.2.

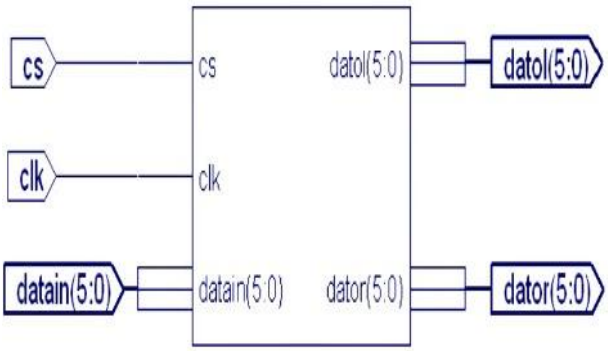
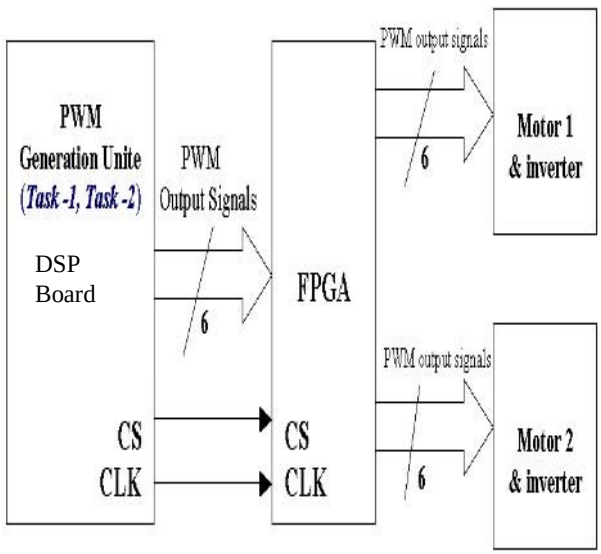
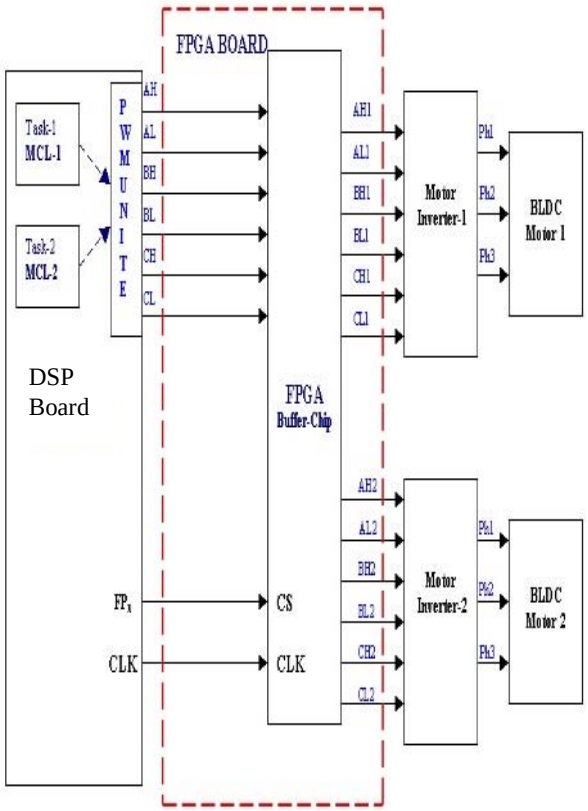


Fig.2. FBGA Two Buffers design Implementation

Then, the design is simulated and downloaded successfully to VERTIX-E XILINX FPGA board. The XILINX FPGA board is interfaced with the DSP PWM Generation Unit and motor inverters are connected to the FPGA buffer's outputs as shown in Fig.3 below.



(a)



(b)

Fig.3. Implementation of Two Motors Control System for N=2 motors.
(a) General system block diagram,
(b)Implemented system diagram.

Task-1: is Motor-1 control loop (MCL-1) and the output of this task goes into FPGA BUFFER-1 to control Motor-1

Task-2: is Motor-2 control loop (MCL-2) and the output of this task goes into FPGA BUFFER-2 to control Motor-2

A type of control logic is used to switch between both motor buffers to choose which one needs to be updated. It is a (CS) logic that has two cases, 0 and 1. The buffer related to Motor 1 is active LOW (0), and buffer related to Motor 2 is active HIGH (1).

When CS is (0), the PWM signals will appear on the buffer output 1 that related to motor 1. When it is (1), the PWM signals will appear on the buffer output 2 that related to motor 2. This way guarantees that both buffers are active at any given time.

4 Two Motors Control Implementation

To verify the robustness and the activeness of the proposed system it is implemented for two motors torque control of 2-BLDC motors to enhance two-wheel mobile robot. Following sub sections illustrate the implementation of two motors torque control.

4.1 BLDC Motor Torque Model

BLDC motors have a widely use in control systems. They can directly provide rotary and transitional motion. Also, they can easily couple with wheels or drums. BLDC motor consists of two parts, electrical part and mechanical part like any DC motor. The 3-phase electric circuit and free body diagram of the BLDC motor are shown in Fig.4 below [12], [13], [14], [15].

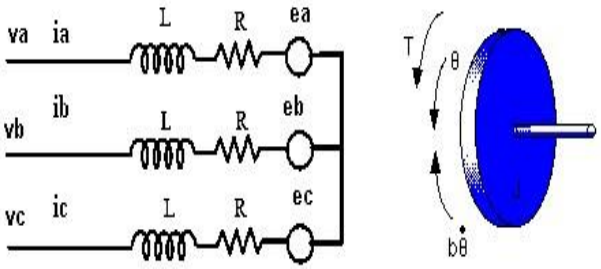


Fig.4. BLDC Motor 3-phase electric circuit & Free-Body diagram

From Fig.4 above, the voltage equations of 3-phase with six switches and Y connected motor can be expressed as:

$$\begin{vmatrix} v_a \\ v_b \\ v_c \end{vmatrix} = \begin{vmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{vmatrix} \cdot \begin{vmatrix} i_a \\ i_b \\ i_c \end{vmatrix} + \begin{vmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{vmatrix} \cdot \frac{d}{dt} \begin{vmatrix} i_a \\ i_b \\ i_c \end{vmatrix} + \begin{vmatrix} e_a \\ e_b \\ e_c \end{vmatrix}$$

Where v_a, v_b & v_c are 3-phase voltages, R the phase resistance, L the phase inductance, i_a, i_b & i_c are phase currents, e_a, e_b & e_c are phase back emf.

However, in this kind of motor, only two of three phases are conducting simultaneously at any time. The equivalent electrical circuit, which is considered for BLDC motor modelling in this paper, is as shown in Fig.5 below.

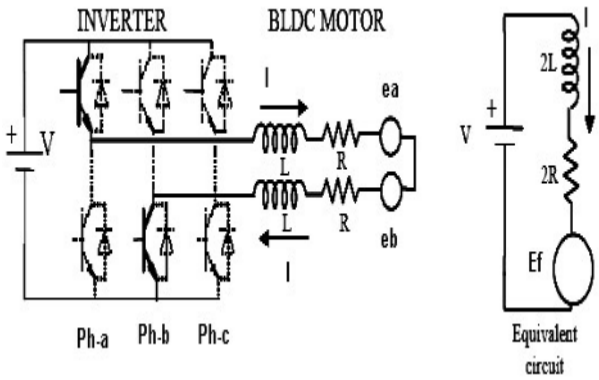


Fig.5. BLDC Motor equivalent circuit when only 2-pheses conducting

From the circuit shown in Fig.5, the 3-phase motor terminal voltage based on Kirchoff's low is performed as:

$$\begin{aligned} V &= 2R.I + 2L\frac{dI}{dt} + E_f \\ V - E_f &= 2R.I + 2L\frac{dI}{dt} \end{aligned} \quad (1)$$

Where V is the supply voltage of the inverter, R & L are the winding resistance and inductance respectively, I is the phase armature current being controlled by PWM, and E_f is the back emf between conducting phases. Back emf can be expressed as a function of rotor speed:

$$E_f = K_e.\dot{\theta}$$

Where: K_e motor constant and $\dot{\theta}$ rotor angular velocity.

By substituting E_f in the differential equation (1) it becomes:

$$V - K_e.\dot{\theta} = 2R.I + 2L\frac{dI}{dt} \quad (2)$$

From the free body diagram the mechanical part equation can be performed based on Newton's second law for rotation:

$$\sum T = J.\alpha$$

Where T motor torque, J rotor inertia and $\alpha = \ddot{\theta}$ rotor acceleration. The motor torque is related to the

armature current I by torque constant K_t. It looks like as:

$$T = K_t . I$$

Referring to the motor free body diagram and Newton's second law for rotation then:

$$\begin{aligned} T &= J.\ddot{\theta} + b.\dot{\theta} \\ K_t.I &= J.\ddot{\theta} + b.\dot{\theta} \end{aligned} \quad (3)$$

Where b is the damping ratio of the mechanical system, $\ddot{\theta}$ is the rotor acceleration, $\dot{\theta}$ is the rotor angular velocity and θ is the rotor angular position. Considering $K_t = K_e = K$ is the motor constant.

From equations (2) and (3) the motor Speed transfer function can be obtained. Using Laplace transforms, equations (2) and (3) can be expressed in terms of *S*.

$$V - KS\theta(s) = 2(R + LS)I(s) \quad (4)$$

$$(JS + b)S\theta(s) = KI(s) \quad (5)$$

By solving the above equations, (4) and (5), the following motor transfer function is obtained, where the rotating speed ($\dot{\theta} = \omega$) is the output and the voltage (V) is the input.

$$\frac{\dot{\theta}}{V} = \frac{S\theta(s)}{V} = \frac{K}{2(R + LS)(b + JS) + K^2} \quad (6)$$

The above Transfer Function can be broken into two parts:

- Electrical part for current/torque control.
- Mechanical part

The following block diagram, Fig.6, illustrates the BLDC motor model and its electrical and mechanical parts.

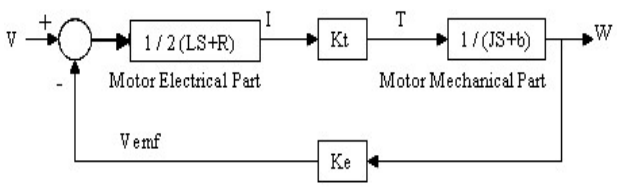


Fig.6. BLDC Motor model in S domain

To design a digital system, the continuous transfer function must be converted to a discrete transfer function (from the S-domain to the Z-domain). Using MATLAB and the 'Zoh' method, the transfer function in equation (6), can be converted to a discrete transfer function after substituting the motor constant values. In general, after conversion; it takes the pole-zero form in the Z-domain shown in equation (7).

$$\frac{\omega(z)}{V(z)} = \frac{g(Z + a)}{(Z - b)(Z - c)} \quad (7)$$

Where *g* is the model gain, *a* is the model zero and *b* & *c* are model poles. The BLDC Motor electrical and mechanical parts model in the Z-domain is shown in Fig.7 below.

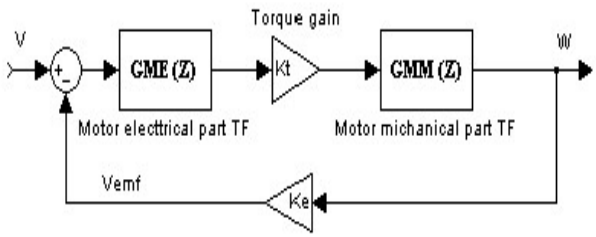


Fig.7. BLDC Motor model in Z-domain

4.2 Torque Control Structure of BLDC Motor

Fig.8 below shows the closed loop torque control scheme for one BLDC Motor where the feedback current is measured using a current sensor on the DC bus and it acts as a torque estimator shared with the torque constant K_t. In general the motor torque can be expressed as the following:

$$T = K_t . I$$

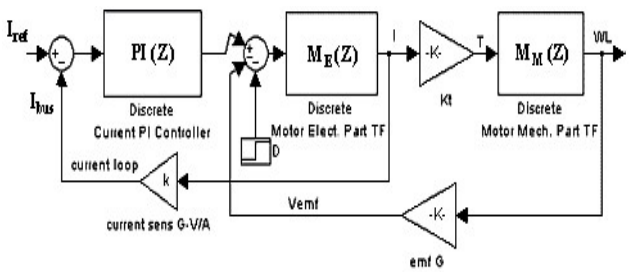


Fig.8. Torque Closed Control Loop of BLDC Motor.

As shown in fig.8 above, the closed loop torque control consists of motor electrical part and current PI controller. For DSP control, the current PI controller can be expressed as:

$$u(n) = u(n-1) + K_0\left[e(n)\right] + K_1[e(n-1)]$$

Where:

$$K_0 = K_p + \frac{K_i \cdot T}{2},$$

$$K_1 = -K_p + \frac{K_i \cdot T}{2}.$$

Where: *e(n)* is the present error sample, *e(n-1)* is the previous error sample. Same applies for *u(n)* and *u (n-1)*, which are the output samples and T is the sampling period, K_P is the proportional gain and K_I is the integral gain.

4.3 DSP Based Motor Torque Control Structure

Fig.9 below shows the DSP implemented closed loop torque control scheme for one BLDC motor. It shows the Software part, which highlighted in red and Hardware part, which highlighted in black. The software part contains following algorithms:

- Six-step commutation driving technique algorithm.
- Current/torque controller algorithm.

The hardware part contains the following devices:

- DSP board (Blackfin™ ADSP-BF561).
- BLD motor Inverter and power stage.
- BLDC motor itself with three position hall sensors.
- Current Sensor on the DC bus to measure the feedback current.
-

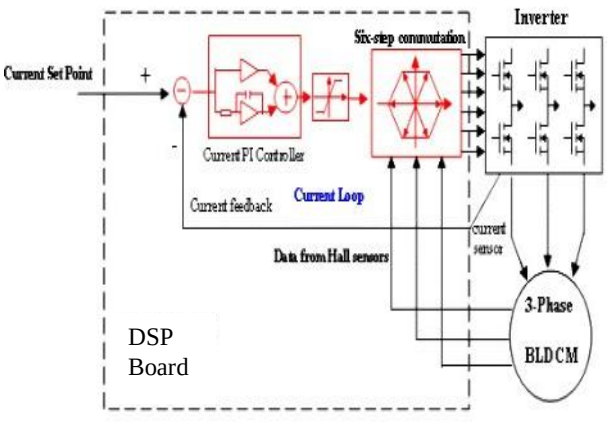


Fig.9. BLDC Motor implemented Current/Torque closed control loop.

The above structure shown in fig.9 was implemented successfully using Blackfin™ ADSP-BF561 processor. Fig.10 below shows the overall control system implementation for one BLDC motor.

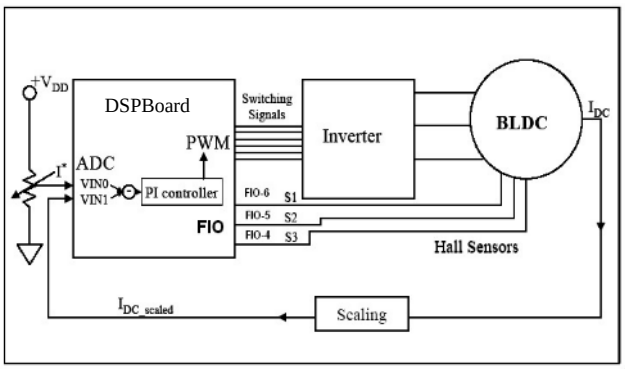


Fig.10. Hardware/Software Overall System Implementation for one motor.

The above system was expanded to control two motors at the same time to enhance two-wheel mobile robot. The system was expanded for two motors torque control by interfacing an external FPGA buffering design with the DSP PWM Unit, as shown in e following section.

4.4 Two Motors Torque Control Structure

The system shown in Fig.11 has been developed and expanded for two motors torque control by interfacing an external FPGA buffering design with the DSP PWM Unit. The system shown in Fig.11 developed to control 2-BLDC motors at the same time using only one DSP Processor with one PWM Generation Unit to enhance two-wheel mobile robot.

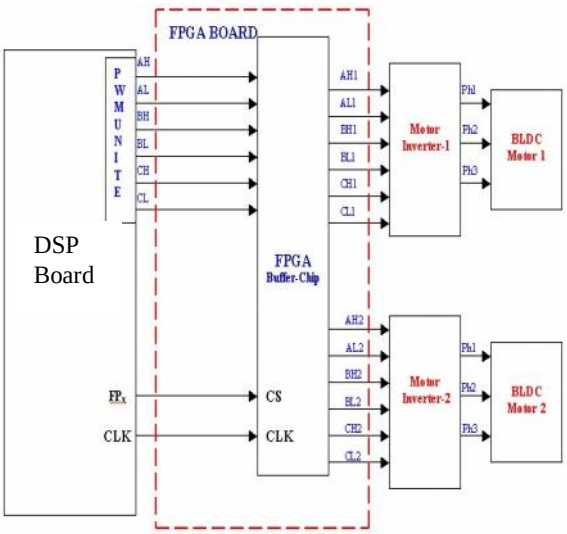


Fig.11. DSP/FPGA Implementation for Two Motors Torque Control

The above system was implemented successfully using FPGA buffering design downloaded to FPGA Vertex-E [11], interfaced with the DSP on board PWM unit.

5 Simulation Results

5.1 FPGA Design Simulation Results

The FPGA buffering design was implemented successfully using VHDL language for two motors control. Simulation results for the design shown in Fig.2 were achieved successfully as shown in Fig.12 below.

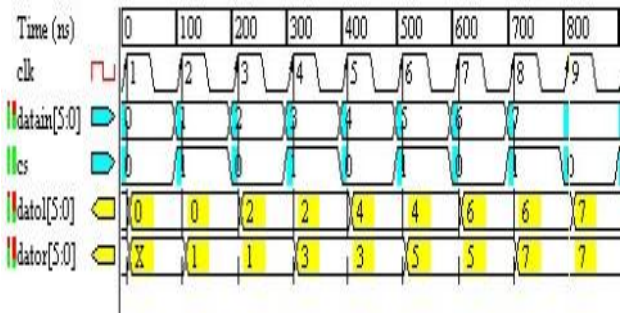
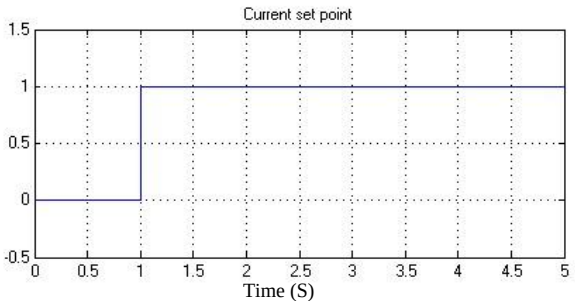


Fig.12. Simulation results for FPGA design shown in fig.2.

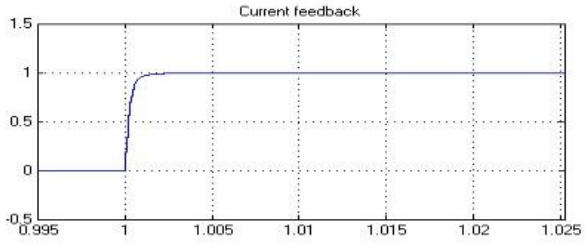
Simulation results show that when the CS is LOW the input signals appear on the first buffer output while the other remain as it is, and when the CS is HIGH the input signals appear on the second buffer output while the first one remains as it is. The above simulation results indicate and prove that the FPGA design operates as expected.

5.2 Motor Torque Control Simulation Results

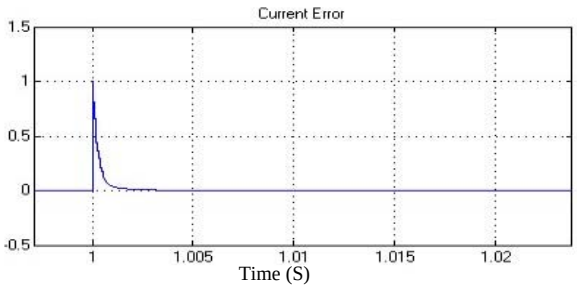
The system shown in Fig.8 was modelled successfully using MATLAB SIMULINK. Simulation results were obtained as shown in Fig.13 below.



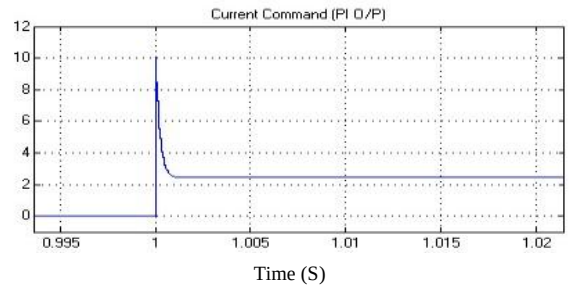
(a)



(b)



(c)



(d)

Fig.13. Closed loop current/torque control simulation results

(a): current set point, (b): current feedback, (c): current error, (d): PI controller output

Simulation results show that the closed loop torque control system achieves constant current and constant torque. Also, it is found that the torque control system rejects disturbances that affect the motor as shown in the simulation results in Fig.14.

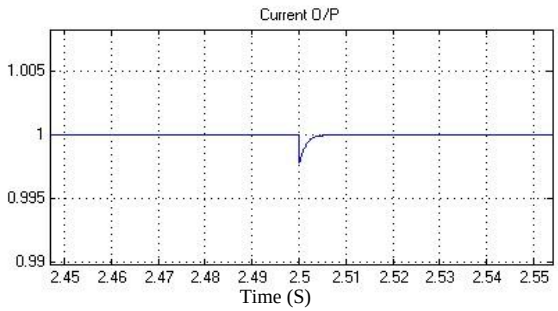


Fig.14. Disturbance rejection

6 Experimental Results

6.1 Two Motors Control Experimental Results

The system shown in Fig.3 was implemented successfully to control two BLDC motors. The FPGA design was downloaded successfully on the Xilinx VERTEX-E FPGA. The FPGA Xilinx board was interfaced successfully with the DSP PWM Unit. An I/O pin of the DSP was toggled to act as CS, the FPGA design Clock was connected to the DSP Clock.

Two BLDC motor inverters were connected to the FPGA design output pins and each BLDC motor was connected to its inverter as shown in Fig.3- (b). The control algorithms (Task1 & Task2) were downloaded successfully to the DSP Processor and both motors were controlled as anticipated.

It has been seen that the DSP processor implemented both tasks successfully by switchi ng between them and the CS controls and chooses the buffer to be updated to keep both motors run and controlled all the time. Fig.15 below shows pair of the experimental PWM signals on the output of each FPGA buffer. (AH1&BL1) appear on the output of the FPGA buffer 1 and (AH2&BL2) appear on the output of the FPGA buffer 2.

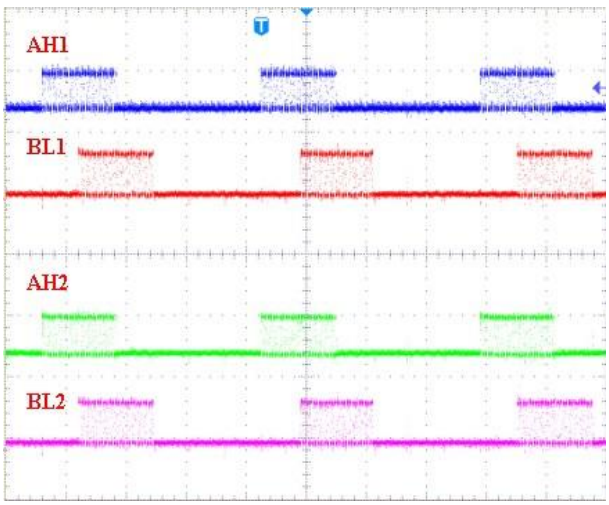
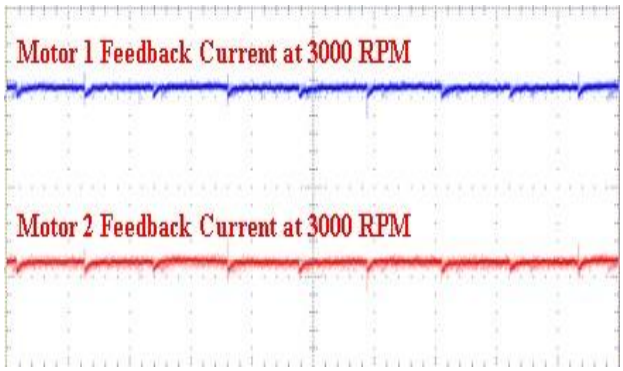
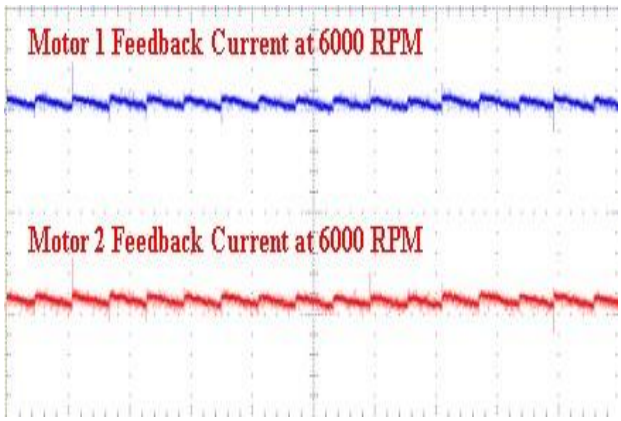


Fig.15. PWM signals on the output of each FPGA buffer.

Fig.16 below shows the experimental feedback current for both BLDC Motors that were controlled using the Two Motor control system shown in fig.3 above.



(a)



(b)

Fig.16. The experimental feedback current for both controlled BLDC Motors
(a) at speed ≅ 3000 RPM, (b) At speed ≅ 6000 RPM.

Fig.17 below shows the experimental phase voltage for both BLDC Motors that were control led using the Two Motor control system shown in fig.3 above.

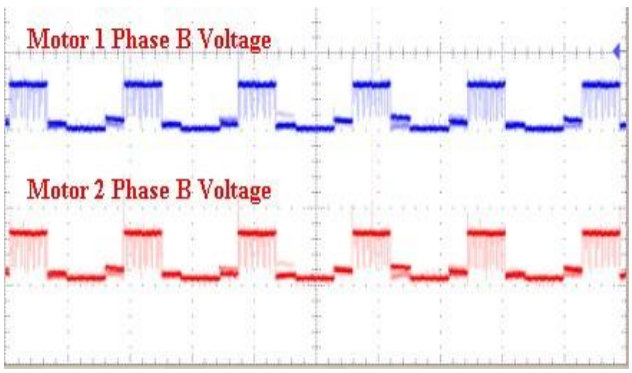


Fig.17. The experimental phase voltage for both controlled BLDC Motors.

The above experimental results indicate and prove that the (DSP-FPGA) based Two Motor Control

System operates as anticipated. Also, they show that the system has the capability to control more than one motor at the same time in synchronization with high performance and low cost system.

6.2 Two Motors Torque Control Experimental Results

For more evidence the system shown in Fig.3 was used and implemented for two motors torque control. The experimental set up of the two motors torque control is composed of the Blackfin™ ADSP-BF561 dual core Processor [16] board from Analog devices, which execute the control algorithms, Vertex-E FPGA board from Xilinx, which execute the FPGA buffering design, Inverters and power stages, BLDC Motors and Current Sensors to measure the DC buss feedback current for each motor.

The above motor torque control system, shown in Fig.9, Fig.10 and Fig.11, was implemented successfully. Following experimental results shown in Fig.18 below were obtained, which are similar for each motor:

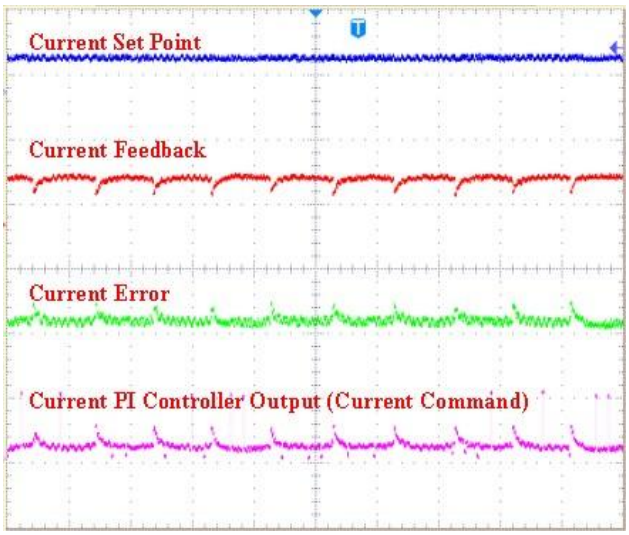


Fig.18. Two motors torque control experimental results

The above results show the step response of the current PI-controller when load is absent. Results above show the trace of the current set point, motor current feedback, the error and the output from the current PI controller. From experimental results shown in Fig.18, one can clearly see that the current PI controller algorithm and the 6-step commutation technique are working effectively with the 3-Phase BLDC motor using Blackfin™ ADSP-BF561 dual core processor. Note that these curves are the outputs from the DSP evaluation board DAC Unite, which initialised for monitoring purpose.

From these Experimental results it can be seen that the closed loop torque control system achieves constant current and constant torque. By comparing above results with MATLAB simulation results, they were found so much similar.

Furthermore, above results verify that the two motors torque control system is sufficient to control successfully more than one motor.

7 Conclusions

This paper has presented the concept of using the Blackfin™ ADSP-BF561 dual core Processor with an external FPGA Buffering Design for Two Motors Control System (TMCS). The various peripheral interface and configuration for Two Motors Control System were discussed and illustrated. The design of the FPGA was also discussed and simulated, implemented and tested experimentally. Experimental results for the DSP-FPGA Two Motors Control System were achieved and introduced successfully.

Moreover, and for more verification a two motors torque control scheme has presented in this paper. The control scheme was implemented successfully using Blackfin™ ADSP-BF561 dual core Processor and Vertex-E FPGA with two BLDC Motors. Simulation and Experimental results have verified the feasibility of the proposed two motors torque control concept.

Accordingly, the DSP-Based Two-Synchronized Motors Control System using external FPGA Design was found to work according to the requirements of the two motors control system implementation.

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