A new High-Speed Interconnect Crosstalk Fault Model and Compression for Test Space

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Abstract: - Signal integrity of high-speed interconnects has significant adverse effect on the proper function and performance of VLSI. A new crosstalk fault model is presented for testing glitch and delay in this paper. This model takes odd and even mode transmission into account based on parasitic RLC elements of interconnect. It can stimulate the maximal signal integrity loss compared to maximal aggressor (MA) model and maximal dominant signal integrity (MDSI) model. Then a compression algorithm for test space is proposed. Several properties such as symmetry, decay and superimposition are studied. Compression steps are explained in detail. Finally simulation is performed and experimental results show that this model is more effective than MA and MDSI models.

Key-Words: - crosstalk, compression algorithm, fault model, high-speed interconnect

1 Introduction

Signal integrity (SI) issue of high-speed interconnect caused by crosstalk has become a big problem in deep-submicron (DSM) technology [1]. There is a critical need to test delay and logic error caused by crosstalk. Fault model and test pattern generation (TPG) are one of key technologies. Test pattern generation for crosstalk glitches is presented in [2]-[4]. Traditional interconnects in system on chip (SOC) have to be treated as transmission line with improvement of operating frequency. The authors in [5] propose a test pattern generation method for signal integrity faults on long interconnects. Order reduction algorithm is used to generate test patterns in order to decrease execution time [6]. There are many algorithms of order reduction. They are not discussed here for limits of this paper. Test generation for capacitance and inductance induced noise on interconnects is studied in [7].Test pattern generation of delay is studied in [8][9]. Many researchers have presented various fault model of crosstalk. Maximal aggressor (MA) fault model for ideal transmission line is presented in [10][11]. With increase of frequency, it can't generate test patterns to create maximal crosstalk fault when mutual inductance comes into play. That is testified too in [12].Multiple transition (MT) model is proposed in [13]. But it is inefficient with too many test patterns. So its test set is compressed according to characteristics of symmetry [14]. A maximal dominant signal integrity (MDSI) fault model is reported in [15]. Odd mode and even mode transmission are studied which amend the limitation of MA. However the same problem of MDSI is that it can't reflect the worst case of crosstalk.The algorithm of test pattern generation based on distributed RLC equivalent circuit in this paper considers odd-mode and even mode transmission characteristics which overcomes limits of MA and MDSI. The test pattern set is optimized in condition of maintaining the fault coverage. Test efficiency is increased after optimization

2 Properties and Concepts of Crosstalk

2.1 Interconnect Model

The accuracy of a test pattern generation depends heavily on the interconnect model. In low and mid-range frequency, interconnection line can be seen as a simple metal wire, only a conductive connectivity role. However, interconnection line will behavedistributed parameters effect when signal wavelength and the length of wire can be compared in the high-requency. For example conductor is hot when currents flow theconductor. That shows that there exists distributed resistance. The leakage current between conductors shows that there existsleakage conductivity. There is voltage between conductors then coupling capacitance must exist between conductors. So these interconnects must be modeled as distributed parameters circuits. In essence signal integrity is caused by parasitic capacitance and inductance which happen crosstalk in high-speed interconnect. Crosstalk means that there are induced voltages and currents between no electrical connection lines for electric and magnetic coupling. The interconnect equivalent circuit of

crosstalk is shown in Fig. 1. It can be seen from the figure that there are mutual inductance(M2), self-inductance(M1), coupling capacitance(C1、C2) and self-capacitance(Cg).The values of distributed R, L and C depend on operating frequency, length , technology and so on.

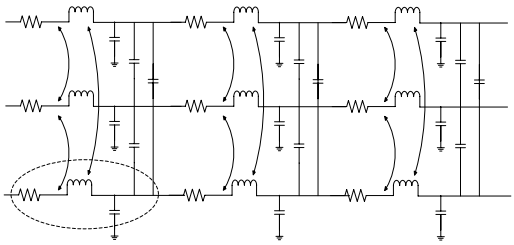


Fig.1 A fragment of R, L, C equivalent circuits of interconnects.

Crosstalk faults appear mainly positive and negative glitch and delay. The glitch happens when induced voltage leads to a pulse on the constant signal lines. If the pulse is too high or hold time is long enough, performance of circuit will degrade seriously, even lead to logic error or breakdown. The delay is caused by crosstalk for time delay in the course of signal propagation. It may lead to timing confusion. There are also speedup and slowdown of crosstalk delay.

2.2 Properties of Crosstalk

Several properties of crosstalk are presented under HSPICE simulation. Technology parameters are listed as follows. Width of interconnection line (W) is 127μm, coupling length is 3mm (L), dielectric thickness (H) is 254μm, rise time is 10ps and input signal is step function. The structure of interconnection lines is shown in Fig. 2.

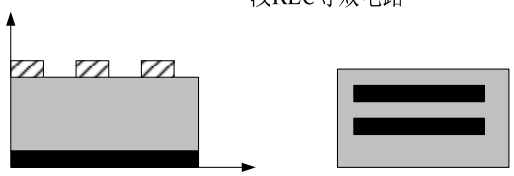


Fig.2 Structure of interconnects.

Definition 1： Degree of crosstalk [10], for an N lines interconnect system, degree of crosstalk caused by k ($k \le N$-1) aggressors near the victim line i is defined k .

Property 1： For an N line interconnect system, if $N-1$ degree of crosstalk is applied on victim line i, no crosstalk fault is detected. Then it is said that no crosstalk faults will happen on this line during work.

Property 2： For an N line interconnect system, multiple aggressors will induce currents on victim line. All degree of crosstalk has the property of superposition for induced currents can be added.

The simulation results of superposition property are shown in Fig. 3.

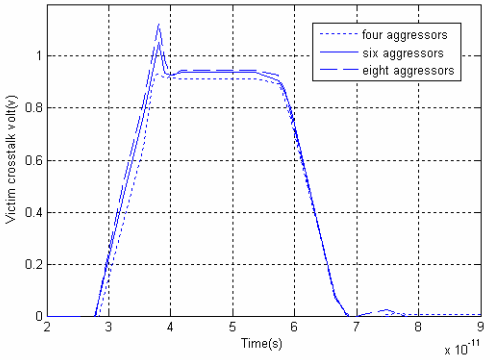


Fig.3 Property of superposition.

Property 3：Degree of crosstalk will decrease with increase of distance between aggressor and victim. The total degree of crosstalk is prone to saturation although the number of aggressors is more and more. In other words, the increase of total degree is too little to be ignored.

The simulation results of decay property are shown in Fig. 4.

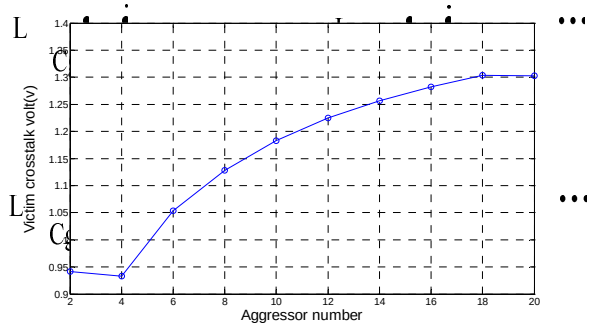
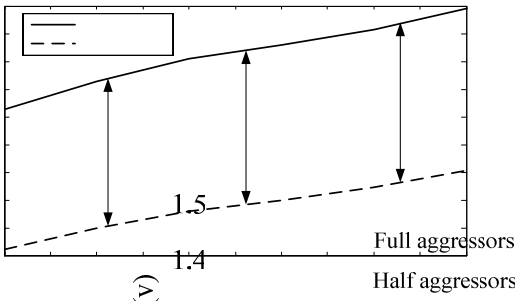


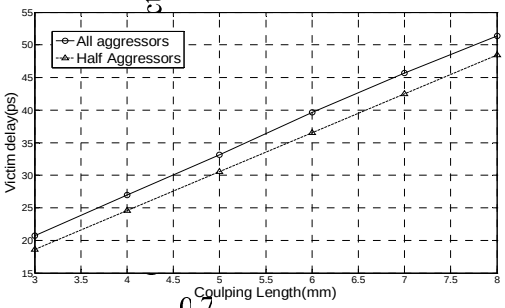
Fig.4 Property of decay.

Property 4: For an N line interconnect system, the same signal transition of right-and-left aggressors has the same effect on the victim taking the victim as symmetry axis. According to the symmetry if $N-1$ aggressors can stimulate the maximal signal integrity loss, then $\lceil (N-1)/2 \rceil$ aggressors at one side of victim can stimulate the maximal signal integrity loss too.

Glitch and delay caused by crosstalk are shown in Fig. 5 taking coupling length for example. It can be seen that full aggressors and half aggressors keep the same property of stimulating the maximal signal integrity loss.



(a) Symmetry properties of glitch fault



(b) Symmetry properties of delay fault

Fig.5 Property of symmetry.

3 Algorithm of Test Pattern Generation

3.1 Fault Definition

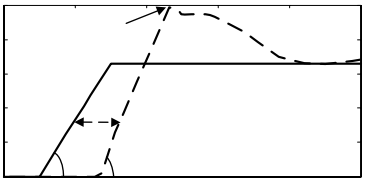
The main faults of Crosstalk are glitch and delay. Eight types of crosstalk fault for our algorithm are shown in Fig. 6.

gp/gn: Positive/negative glitch.

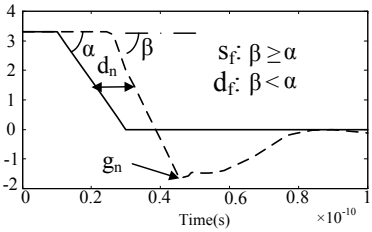
dr/df : Rise/fall slowdown.

sr/sf : Rise/fall speedup.

dp/dn: Positive/negative propagation delay.



(a) Fault of gp,dr,sr and dp



(b) Fault of gn,df,sf and dn

Fig.6 Type of crosstalk faults (a) fault of gp,dr,sr and dp(b) fault of gn,df,sf and dn.

3.2 Test Pattern Generation

The idea of this TPG algorithm is to apply the test pattern which can stimulate the maximal crosstalk to the victim line. If no fault is detected then we can say no crosstalk fault will happen on this line during working. Based on defined crosstalk fault above, test patterns are shown in table 1 for a interconnect system of one victim line and six aggressor lines.

Table 1 Test Patterns for Seven Interconnects

Fault type	Test patterns						
gp	-1	-1	1	s-0	1	-1	-1
	1	1	1	s-0	1	1	1
gn	1	1	-1	s-1	-1	1	1
	-1	-1	-1	s-1	-1	-1	-1
dp/dr	1	1	1	1	1	1	1
dn/df	-1	-1	-1	-1	-1	-1	-1
sr	-1	-1	-1	1	-1	-1	-1
sf	1	1	1	-1	1	1	1

In this table, "1" represents positive transition namely the signal on the line transits from 0 to 1. For example a step signal transits from 0v to 3.3v during rising time. The meaning of "-1" is opposite to "1". s-0 and s-1 represent the signal is quiescent at 0 or 1.

Glitch fault is caused by coupling capacitance and mutual inductance which will induce current on the victim line. MA fault model is valid to some extent which takes only coupling capacitance into account. With improvement of frequency, inductance-induced current become bigger. However currents induced by capacitance are opposite to current induced by inductance. Considering this non-linear changing relationship, test patterns for gp/gn not only contain MA but also take odd-even mode patterns into account in order to trigger the maximal signal integrity loss.

Delay is determined by effective dielectric constant. When signals on aggressor lines are in even mode transmission, each interconnect is at the same potential and there are few field lines in the air; most of them are in the bulk material. This means the effective dielectric constant the victim line sees will be higher, dominated by the bulk-material value. This will increase the effective dielectric constant for the victim-line signal when the aggressor lines switch in the same direction. This will decrease the signal speed and increase the time delay of the victim signal. The odd mode is just opposite to even mode. The electric field of odd-mode and even mode transmission is shown in Fig. 7.

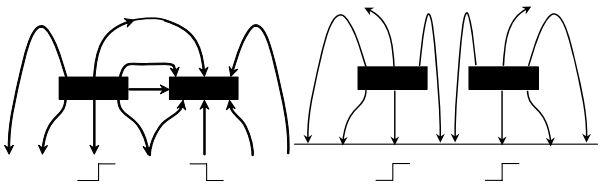


Fig.7 Electric filed of odd-mode and even mode transmission.

3.3 Optimization of Test Pattern Set

Definition 2：For an N line interconnect system, the fault model in this paper has 8N two-pattern tests, and requires total 16N patterns. Each pattern has N bits. The test space s is defined as follows.

$$s = \sum_{i=1}^{N} 16 \times N \qquad (1)$$

Definition 3：Decay factor, for an N line interconnect system, when the total degree of crosstalk is prone to saturation based on property 3. Now the degree of crosstalk is k, decay factor α is defined below.

$$\alpha = (N\text{-}k)/N \times 100\% \qquad (2)$$

Definition 4: Compression ratio β, β is defined as the ratio of compressed test space to test space.

$$\beta = \frac{\text{compressed test space}}{\text{test space}} \times 100\% \qquad (3)$$

Based on properties and definitions above, test pattern set can be optimized. The detailed steps of optimization algorithm are presented as follows.

Step 1: For an N lines interconnect system, initial test space s is built.

Step 2: According to property 3, decay factor α can be determined depending on precision of test. Then bits of each pattern is $m = \lceil N(1-\alpha) \rceil$, test space is shown as follows:

$$s' = \sum_{i=1}^{N} 16 \times \lceil N(1-\alpha) \rceil \qquad (4)$$

Step 3: For each pattern of compressed test space s', if it has the symmetry based on property 4 then bits on one side of victim are gotten rid of. Bits of each pattern are

$$m' = \begin{cases} \lceil N(1-\alpha) \rceil / 2 & \text{m is odd} \\ \lceil N(1-\alpha) \rceil / 2 + 1 & \text{m is even} \end{cases} \qquad (5)$$

Step 4: Repeat the step3 until all patterns in test space are over. The test space is compressed below:

$$s'' = \sum_{i=1}^{N} 16 \times m' \qquad (6)$$

Step 5：The optimization algorithm is ove.

The flow chart of this compression algorithm is shown in Fig.8.

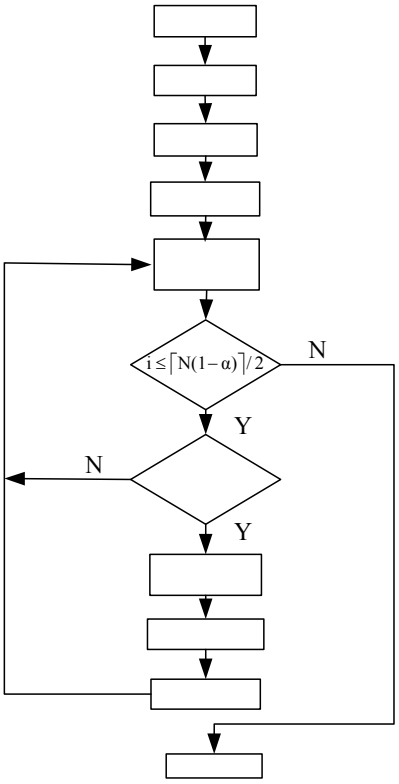


Fig.8 Flow chart of compression algorithm

The test set decrease greatly after optimization. The optimization results are shown in table 2.

Table 2 Compression Ratios

Numberof interconnects	N=21	N=31	N=67	N=89
Initial test space (bits)	7056	15376	71824	126736
Compressed space (bits)	3360	4960	10730	14240
compression ratio(%)	47.6	32.3	14.9	11.2

note：N is the number of interconnects

It can be seen that degree of crosstalk and bits of each pattern will decrease greatly after optimization. The less number of aggressors applied patterns at the same time, the more interconnects can be test. The position of victim line is in the center of interconnect system in table 2. If victim line is on the one side of interconnect system, compression results will be worse and compression ration will be larger. However test set after compression is still smaller than initial test set.

4 Experiment Results

4.1 Validity of Test Pattern

The maximal crosstalk of different patterns on victim for positive glitch is shown in Fig. 9. These patterns include MA, MDSI and odd and even mode patterns.

Crosstalk by the pattern [-1 -1 1 0 1 -1 -1] is larger than other patterns when distance is less than 215 um. When distance of lines is larger than 215um, crosstalk by the pattern [1 1 1 0 1 1 1] of MA is larger than others. Two patterns are both contained in this TPG algorithm that can stimulate maximal crosstalk.

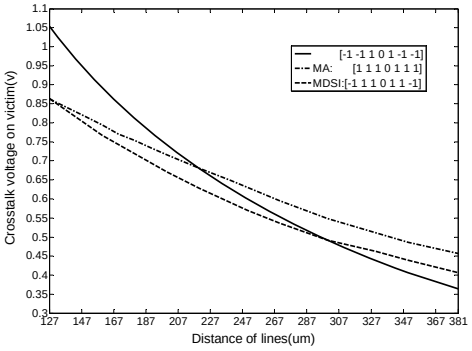


Fig.9 Comparison of test patterns for gp.

4.2 Maximal Delay Simulation

The maximal delay fault with the increase of rise time is shown in Fig. 10. Delay caused by patterns of MA fault model decrease with the increase of rise time. However both the MDSI model and our model stimulate maximal crosstalk delay.

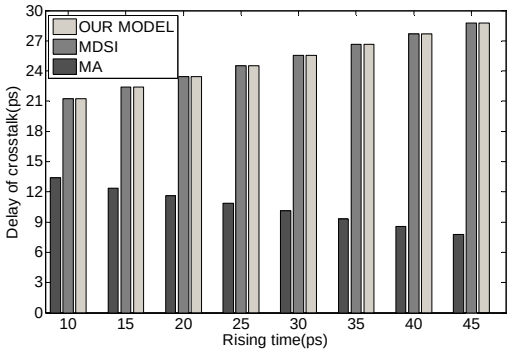


Fig.10 Maximal delay caused by three models.

4.3 Maximal Glitch Simulation

When changing geometry parameters of interconnects, such as length of line, width, distance and rise time, patterns of this algorithm still triggers the maximal glitch and delay compared to MA and MDSI model. The results are shown in table 3.

4.4 Test Space Comparison

The test space of MA, MDSI and model in this paper is shown in table 4. It can be seen from this table that once decay factor is determined, test space capacitance has little difference near the degree of crosstalk. The test space of our algorithm increases with the increase of N. However test space of MA and MDSI increase with the increase of N2. It is obvious that our algorithm is more effective than other two models.

Table 3 Maximal Glitch Voltages of Three Models

Fault model	length(mm)				Distance between lines (um)				width（um）				Rise time (ps)			
	2	4	5	6	254	381	508	635	130	160	200	254	10	15	20	50
MA (v)	0.8637	0.8575	0.8457	0.8309	0.6254	0.4571	0.3492	0.2641	0.8627	0.8535	0.8339	0.8103	0.8634	0.8419	0.8385	0.5899
MDSI (v)	0.8618	0.8608	0.8632	0.8633	0.5630	0.4068	0.3022	0.2402	0.8623	0.8474	0.8249	0.8743	0.8636	0.8530	0.8520	0.5899
our model (v)	1.0213	1.1110	1.1587	1.1968	0.6254	0.4571	0.3492	0.2641	1.0536	1.0475	1.0269	0.9852	1.0536	1.0115	0.9958	0.5829

Table 4 Test Space of MA, MDSI and Algorithm in This Paper

Fault model	Test space (bits)	N=21	N=31	N=67	N=89	Detect maximal glitch	Detect maximal delay
MA（bits）	$8N^2$	3528	7688	35912	63368	×	×
MDSI （ bits ）	$12N^2$	5292	11532	53868	95052	×	√
Algorithm in this paper(bits)	$8N\lceil N(1-\alpha)\rceil$ □ $8N\lceil N(1-\alpha)\rceil+16N$□	3360	4960	10730	14240	√	√

note：□*N* is odd □*N* is even

4 Conclusion

A test pattern algorithm for crosstalk is presented considering odd-mode and even-mode characteristics based on properties of crosstalk. Eight types of crosstalk fault are defined. Test patterns for these faults can stimulate the maximal glitch and delay compared to MA and MDSI models. Test set is optimized based on several properties of crosstalk. Finally simulation is performed using HSPICE and results testify validity of this algorithm.

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