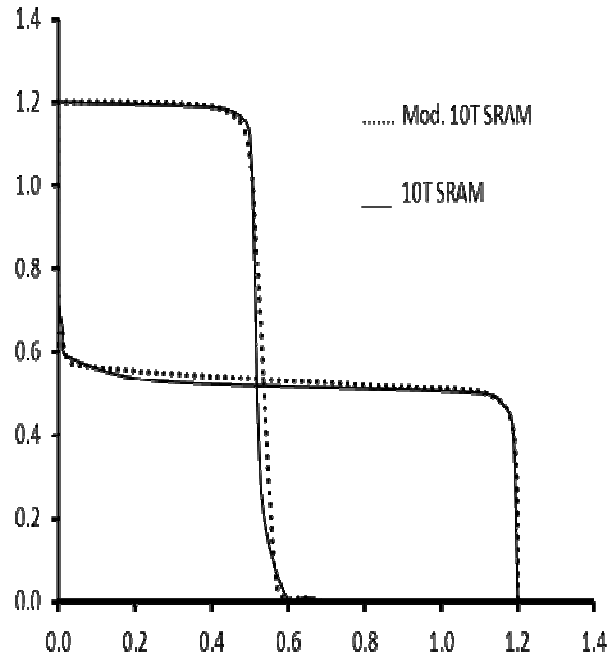

Figure 4c: Butterfly curve of 10T and modified 10T SRAM architecture
Scale: Horizontal Axis- 1 Unit = .01 Volts
Vertical Axis- 1 Unit = .01 Volts

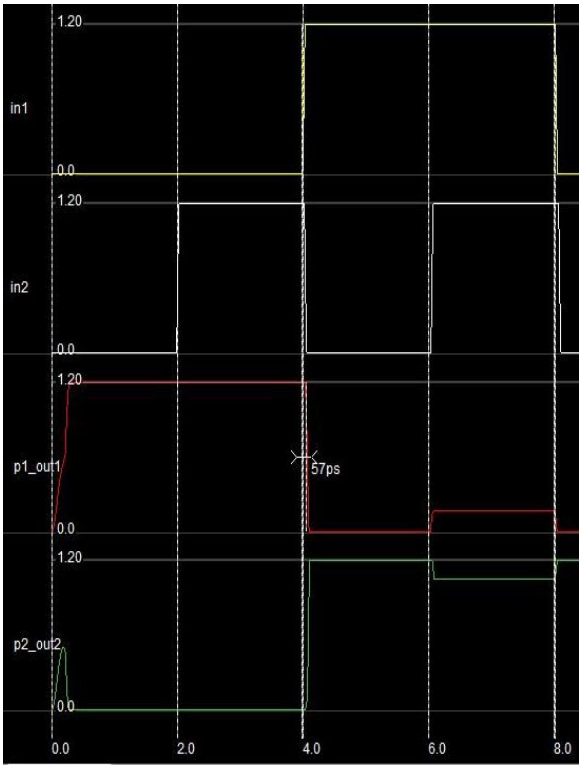

Fig. 4d: Simulation result for 10T-SRAM architecture with same V_T and W/L NMOSs
Horizontal Axis- Time in Nano Seconds
Vertical Axis- Voltage level in Volts

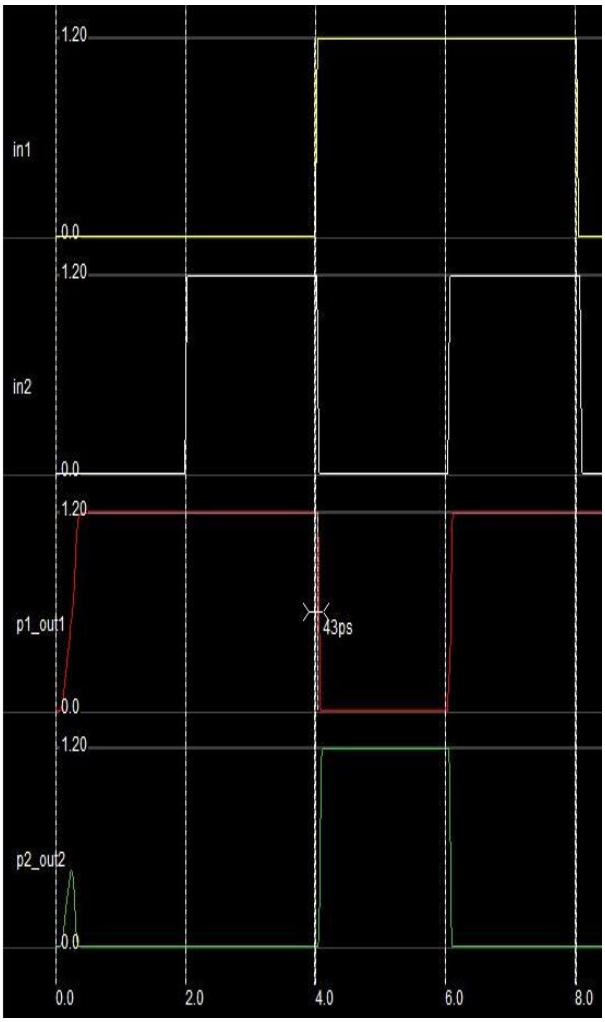

Fig. 4e: Simulation result of modified 10T-SRAM
Horizontal Axis- Time in Nano Seconds
Vertical Axis- Voltage level in Volts

2.4 An 8T- SRAM architecture with transmission Gates in place of access transistor

In this section the proposed technique is applied on an SRAM cell architecture which utilizes the transmission gates in place of access transistors connected to its word line. Improvements in static and dynamic performance are obtained when the switches are implemented with CMOS transmission gates. Researchers are working with transmission gates at different positions in SRAM architecture [8]. Fig. 5a shows the SRAM cell architecture which utilizes the transmission gates in place of access transistors connected to its word line. While simulating this architecture the threshold voltages and W/L ratios of all the NMOS and PMOS are identical.

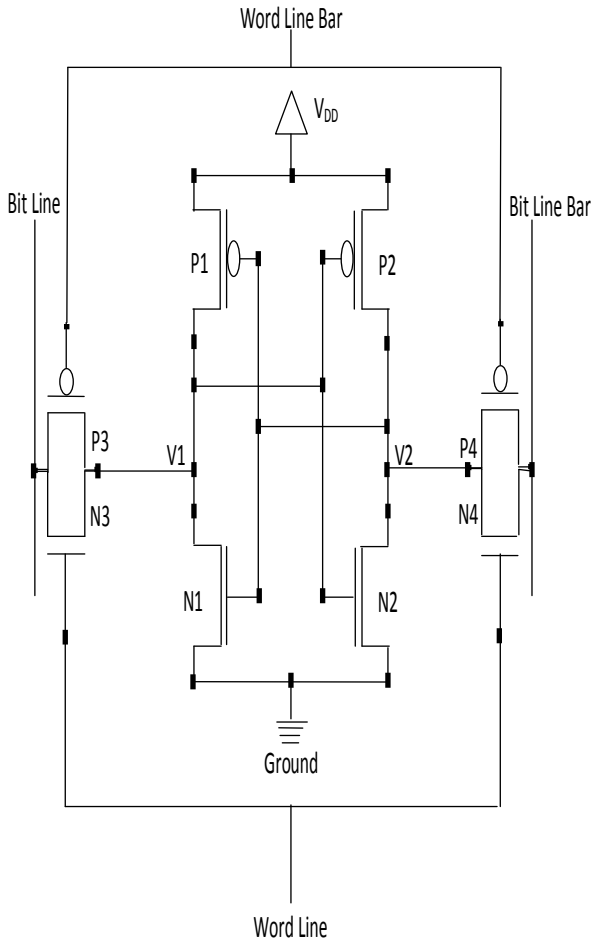

Fig. 5a: 8T-SRAM architecture with transmission gate in place of access transistor

The proposed technique for write delay improvement is applied on the above 8T-SRAM architecture resulting in a modified 8T-SRAM architecture which uses transmission gate in place of access transistors as shown in fig. 5b. Fig. 5c presents the butterfly curve for 8T and modified 8T with transmission gate. In which the solid lines represents the butterfly curve for 8T-SRAM architecture and dotted line represents the butterfly curve for modified 8T-SRAM architecture. In these butterfly curves both the horizontal and vertical axes represent the voltages in volts. In both the axes 1 unit is taken equal to .01 volts. Fig. 5d and fig. 5e represents the simulation results for 8T SRAM (with transmission gate in place of NMOS access transistor) and modified 8T SRAM architecture respectively. In the simulation results the horizontal axis represents the timing in nano seconds and the vertical axis represents the voltage level in volts. Here again the threshold voltages and W/L ratios of all the NMOS and PMOS are identical. The dotted line in fig. 5c represents butterfly curve for the modified 8T SRAM architecture and continuous line represents butterfly curve for 8T SRAM architecture. The SNM for 8T SRAM is .53 volt and for modified 8T is .51 volts (Fig. 5c) which represents the degradation in SNM is of 3.77% From simulation results in fig. 5d and fig. 5e, the improvement in write delay is about 8.89% while improvement in power dissipation is not significant in this particular case where transmission gates are used in place of NMOS access transistors.

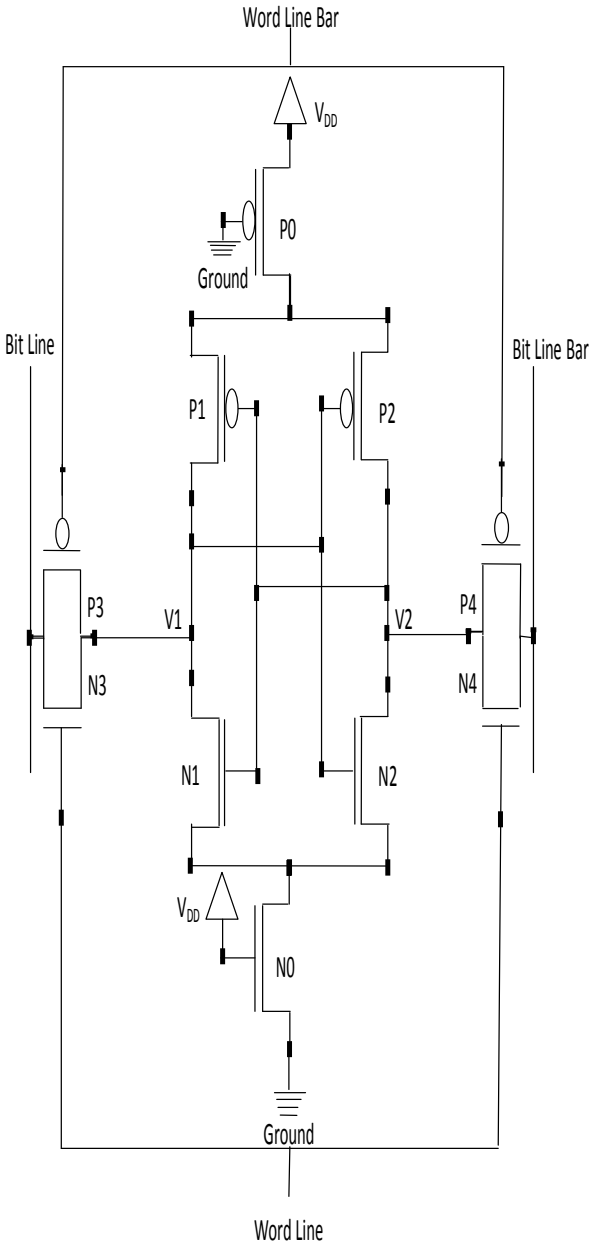

Fig. 5b: Modified 8T SRAM architecture with transmission gate in place of access transistor

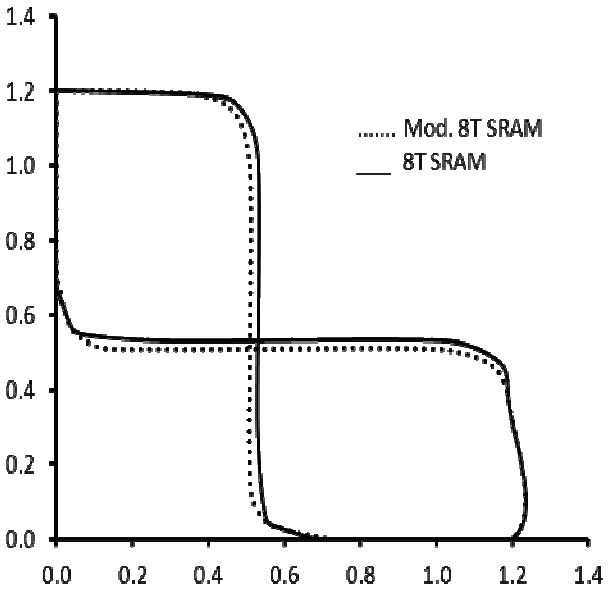

Fig. 5c: Butterfly curve for 8T-10T (modified 8T with transmission gate) SRAM architecture with transmission gate in place of access transistor
Scale: Horizontal Axis- 1 Unit = .01 Volts
Vertical Axis- 1 Unit = .01 Volts

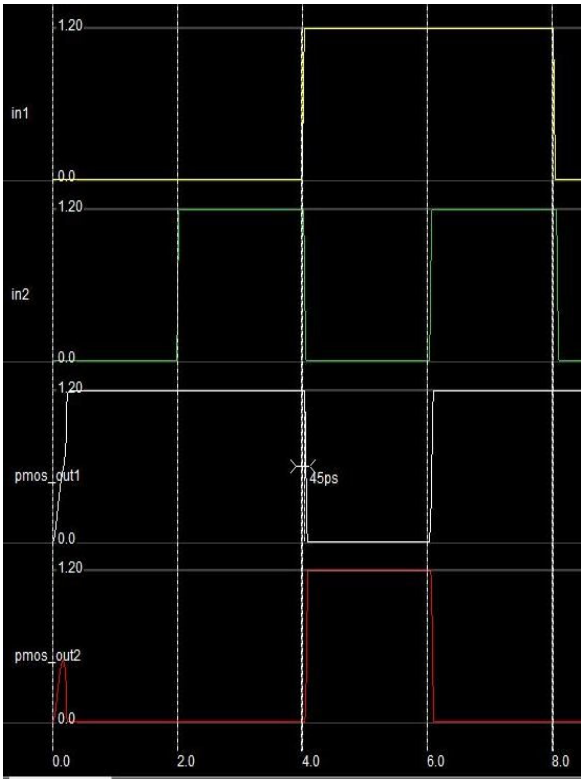

Fig. 5d: Simulation result for 8T-SRAM architecture with transmission gate in place of access transistor
Horizontal Axis- Time in Nano Seconds
Vertical Axis- Voltage level in Volts

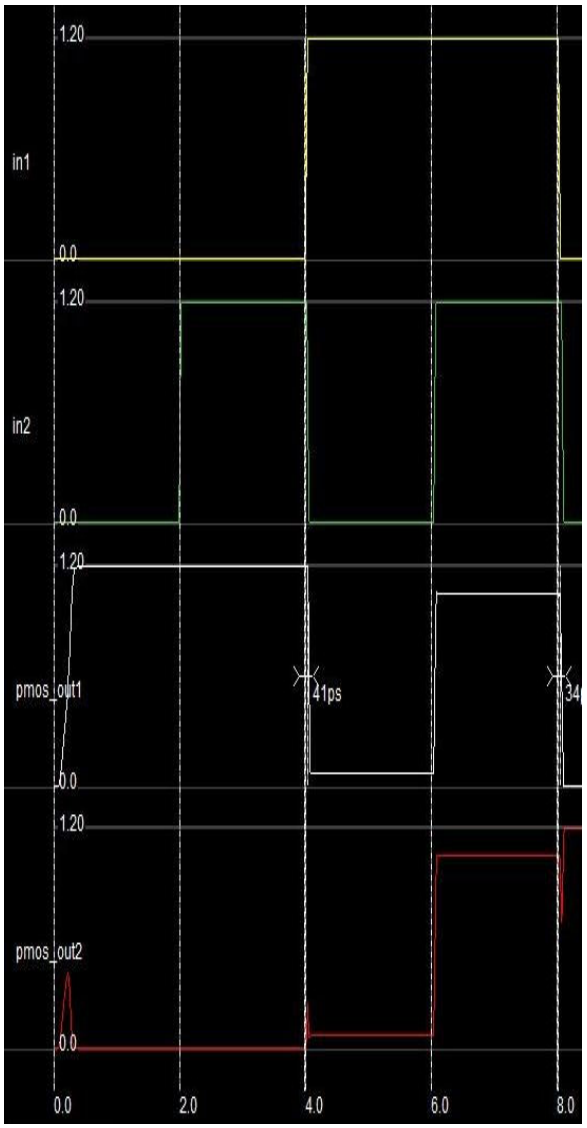

Fig. 5e: Simulation results for 10T-SRAM (modified 8T with transmission gate) architecture with transmission gate in place of access transistor
Horizontal Axis- Time in Nano Seconds
Vertical Axis- Voltage level in Volts

The results mentioned in the Table-1 were obtained after simulation for various SRAM architectures using 120 nm technology. The three important parameters obtained from simulation were SNM, write delay and power dissipation.

The analysis of simulation results reveals that the proposed technique provides write delay improvement in both the cases of 6T and 10T-SRAMs and hence one can say that it will show significant improvement in other cases also. The chip area consumed by the two transistors will be

insignificant as it can be used for several SRAM cells connected in parallel.

Table.1: Performance parameter of basic SRAM architecture and its modified version (as per the proposed technique)

S.No	SRAM Arch.	Write Delay (in ps)	SNM (inV)	Power Dissipation (in µW)
1.	Basic 6T-SRAM	47	.53	10.837
2.	Modified 6T-SRAM	41	.51	9.189
3.	10T-SRAM architecture	57	.50	17.992
4.	Modified 10T-SRAM architecture	43	.49	13.219
5.	8T-SRAM architecture with transmission gates in place of access transistors	45	.53	14.911
6.	Modified 8T-SRAM architecture with transmission gates in place of access transistors	41	.51	14.90

3 Conclusion

This work proposes a new technique for reducing write delay of an SRAM cell. The proposed technique is then applied on three different SRAM architectures. First circuit on which this technique was applied was basic 6T SRAM where as the other circuit was 10T SRAM given by Sheshadri and Houstan. The third architecture on which the proposed technique is applied is one in which the transmission gates are used in place of access transistors. Simulation results for all three cases, before and after the application of proposed technique, were obtained and listed in Table-1. The three fold advantage associated with this technique as evident from the above study is (a) The amount of write delay improvement is significant and (b) Reduction in power dissipation were significant compared to the degradation of SNM (c) The application of proposed technique is independent of the SRAM architectures. Although the application of proposed technique increases the area required by the SRAM architecture but reduction in speed and power dissipation can be helpful in the applications where area occupied by SRAM architectures is not major concern and a fast and power efficient SRAM architecture is the prime requirement. All the SRAM architectures used in the present work are symmetrical SRAM architectures. As a future scope of this technique it will be interesting to see the behavior of proposed technique on non symmetrical SRAM architectures.

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