Investigation of Some Quite Interesting Divisibility Situations in a Signature Analyzer Implementation

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Abstract: - When designing error detecting and correcting systems, cryptographic apparatus, scramblers and other secure, safe and authenticated communication and digital system response data compression devices, the division of polynomials are frequently involved. Commonly, the process of division is implemented by using hardware known as Linear Feedback Shift Registers (LFSRs). In digital system testing the technique of Built-In Self Test (BIST) uses this LFSR based division process for response data compression and is popularly known as Signature Analyzer (SA). This paper presents a simulation experiment on the effectiveness study of the SA schemes. The finding of the results of the simulation study reveals that in SA implementation; in general the uses of primitive characteristic polynomials are the best. However, the study further investigates that the use of some critical primitive characteristic polynomials may reverse the effectiveness of the SA schemes i.e. lead to observe maximum aliasing errors.

Key-Words: - Signature Analyzer, Linear Feedback Shift Registers, Built-In Self-Test, VLSI, Aliasing Errors, Characteristic Polynomial, Primitive Polynomials, Polynomial Division, Cyclic Redundancy Check

1 Introduction

Because of its many inherent advantages, currently, Built-In Self-Test (BIST) has become an effective and widely acceptable tool for tackling test problems for VLSI chips and digital systems [1-6]. By building test circuitry on chip, BIST techniques usually combine a built-in stimulus source (test sequence generator) with a response data compressor. This approach eliminates the complex task of integrating separate circuits for test-pattern generation and response data compression. Besides, BIST approach minimizes the storage requirements of test sequences and large response data, as well as reduces the test time, and isolates defect to chip level itself. Furthermore, because test stimuli are applied using normal clock rate, testing of a self-testable chip can be performed at-speed. Additionally, since the test resources are available during the entire life of the chip, they can significantly simplify the diagnostics and maintenance procedures for digital systems [1 - 8].

In built-in self-test environment Linear Feedback Shift Registers (LFSRs) is an integral part of sequential design, such that they can be used for both generating the test sequences and compressing the output response data using SA scheme (see Fig. 1).

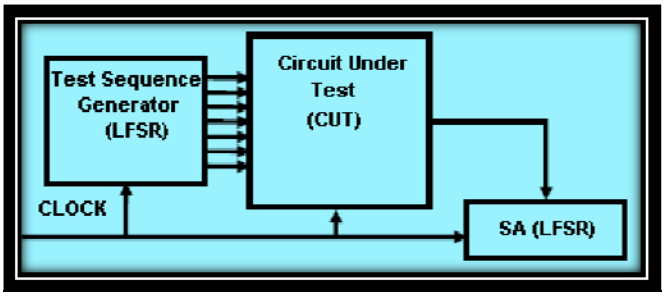

Figure 1: BIST approach of testing

But the difficulty arises when the resulting response data obtained from the Circuit Under Test (CUT) is compressed into small signatures using Signature Analyzer (SA) via response data compression tool. Although, SA scheme is easily implemented by an LFSR, but this leads to loss of information, due to the erroneous response patterns that gets compressed into the same signature as the fault free signature of the CUT. Thus, some of the faults might go undetected due to this error-masking

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Author (Short Biography)

Afaq Ahmad belongs to department of Electrical and Computer Engineering department at Sultan Qaboos University, Sultanate of Oman. He holds B.Sc. Eng., M.Sc. Eng., DLLR and Ph.D. degrees. Ahmad did his PhD from IIT Roorkee, India in 1990. Before joining Sultan Qaboos University, Dr. Ahmad was Associate Professor at Aligarh Muslim University, India. Prior to starting carrier at Aligarh, he also worked as consultant engineer with Light & Co., lecturer with REC Srinagar and senior research fellow with CSIR, India.

Dr. Ahmad is Fellow member of IETE (India), senior member of IEEE Computer Society (USA) and life member of SSI (India), senior member IACSIT, member IAENG and WSEAS; He has published over 100 technical papers. At present he is associated as editors and reviewers of many reputed journals. He has delivered many keynote, invited addresses, extension lectures, organized conferences, short courses, and conducted tutorials at various universities of globally repute. He chaired many technical sessions of international conferences, workshops, symposiums, seminars, and short courses. He has undertaken and satisfactorily completed many highly reputed and challenging consultancy and project works. His research interests are: fault diagnosis and digital system testing, data security, graph theoretic approach, microprocessor and microcontroller based systems, advanced logic design and interfacing using Verilog – HDL, system reliability, fault tolerance, algorithm design, test and computer programming.

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