A new CMOS Current Controlled Oscillator with Minimum Phase Noise Based on a Low Parasitic Resistance CCII

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Abstract---In this paper we present a design of a minimum phase noise current controlled oscillator in CMOS technology. Owing to their high degree of controllability, the second generation current conveyer is used as a basic block for our oscillator. Thus, the first step in our design was to improve static and dynamic behaviour of second generation current conveyers. We present therefore a design of CMOS class AB second generation current conveyors. The translinear implementation in CMOS technology was first studied and then a considerable improvement of the parasitic series resistance on port X is done by presenting a structure of CCII. With a control current of 300 µA, a reduction of RX by a factor of 10 is observed leading to a notable improvement of the frequency behaviour. This improved CCII version was used as a basic building block in the design of a new current controlled oscillator covering [100MHz-600MHz] frequency is presented. Phase noise characteristics of the presented oscillator are investigated. We present then a new methodology of modelling and optimisation of phase noise of current controlled oscillators for CMOS process. This optimization strategy leads to a minimum phase noise acting on device geometries and design sources. PSpice simulation results are performed using CMOS 0.35 µm process of AMS.

Key-Word--- Current Controlled Oscillators, Standard CMOS current conveyor, CCII, cascode structure, Conveyor characterization, RF application, Phase noise optimisation.

I. INTRODUCTION

Variable Frequency Oscillators are basic signal-generating blocks frequently needed in communication systems, such as phase-locked loops, clock recovery circuits, and intermediate frequency synthesizer in wireless transceivers, etc,… In order to get controllable characteristics for the oscillator, CCII based oscillator have proven better tuning characteristics [1-2-3]. Among these implementations translinear second generation current controlled conveyer based structure seems to be the most attractive. In fact, being able to control the output resistance at port X by means of a current source [4-8] , one may exploit this in the synthesis of electronically adjustable functions. As an application, the CCII was used to build up a current controlled oscillator covering [100MHz-700 MHz] frequency range.

Early configurations of CCII has overcome the frequency limitations by means of translinear loops. This family of CCII is first proposed in bipolar technology resulting in good performances regarding current and voltage bandwidth [9-10]. Recently, translinear CCII family was extended to MOS submicron technologies going towards VLSI design. Reaching submicron technologies, the MOS transistor becomes able to achieve high transit frequencies. In order to get accurate and high frequency transfer functions, special design techniques should be applied In this optic, we propose the design of a new version of a CCII using the 0.35µm CMOS technology of AMS. First, we implement the translinear CCII structure, propose an improved version and compare their performances by means of a full characterization. The presented CCII has the advantage of presenting a low parasitic resistance at port X which can be controlled by a bias current of the CCII.

Moreover, strict requirements on phase noise of local oscillators makes phase noise optimisation an integral part of the oscillator design. Phase noise can be defined as frequency or phase deviations in the oscillator signals due to

errors introduced by electronic device noise. Phase noise has been subject to numerous studies [1-3]. Most of the proposed noise models remain applicable to only a special class of oscillators. Besides, each of these models ignores the direct effect of device noise and scaling device dimension on phase noise. A general and appropriate study of phase noise is lucking. Our final objective in this paper is an accurate optimisation of phase noise acting eventually on device parameters and design sources. Therefore, we propose in this paper a CCII based variable frequency oscillator with minimum phase noise.

This paper is organized as follows: in section II, we present the CCII based oscillator structure. Then After, presenting the general characteristics of second generation translinear current conveyors an improved version is giving. Leading to a decrease of the series resistance R_X. Then, we present a characterization of the oscillator tuning over a decade of frequency. In section III, we introduce a general approach of minimizing phase noise in controlled oscillators. In section IV, we model in a first step the CCII noise, its dependence over transistor geometries and biasing sources and in a second step, its contribution to the oscillator phase noise. Then, we end to a generic expression of the controllable oscillator phase noise. Section V is finally devoted to phase noise minimization acting on transistors scaling and current sources magnitudes, based on the heuristic algorithm.

II. The current controlled oscillator synthesis:

Let's consider the oscillation structure of Fig. (1.a) Where the CCII's are assumed to be ideal. The corresponding oscillation condition is given by:

$$Y_1 Y_5 + Y_4 (Y_3 + Y_5) = Y_2 Y_5 \quad (1)$$

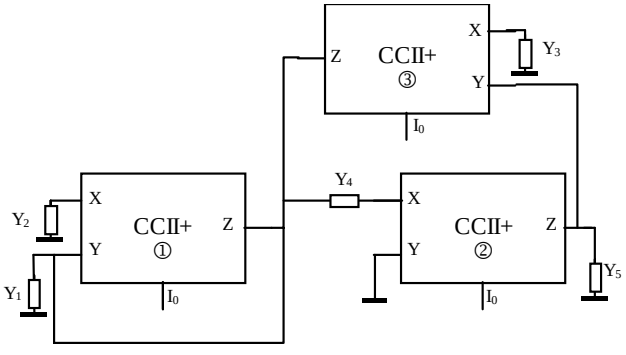

Fig.(1.a) The Oscillator Structure

One implementation of this oscillator can be done taking:

$$Y_1 = pC_1, Y_2 = \frac{1}{R_2} = Y_4 = R_4, Y_3 = \frac{1}{R_3} \quad and \quad Y_5 = pC_5 \quad (2)$$

The implementation of the structure is shown in Fig.(1.b)

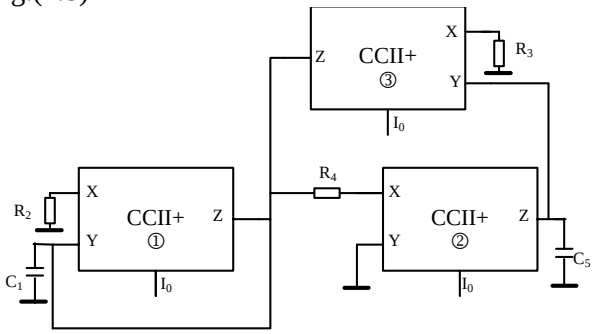

Fig.(1.b) Variable Frequency Oscillator Implementation

It leads to the following oscillation condition

$$R_2 = R_4$$

for which the oscillation frequency is given by:

$$f_0 = \frac{1}{2\Pi\sqrt{C_1 C_5 R_3 R_4}} \quad (3)$$

From eqn (3), we get a variable frequency oscillator. The oscillation frequency can be adjusted independently without modification of the oscillation condition by varying R_3. Since R_3 is connected to a CCII port X, we can use one implementation of the CCII presenting a variable resistance on port X such as the translinear configuration. The oscillator will be in that case controlled by means of a current source. In order to get higher values of the oscillation frequency, R_3 should be as low as possible. We can therefore materialize it only by the internal resistance at port X without any external connections. For this strategy we give a new proposed structure of oscillator. The proposed structure is given in Fig. (1.c).

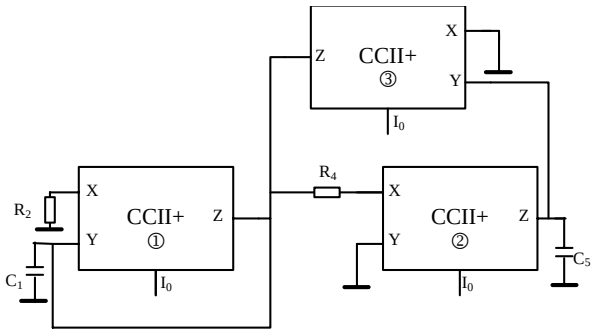

Fig.(1.c) Variable proposed Frequency Oscillator

II.1. CMOS implementation of the CCII

Many implementations of CCII are possible, the most attractive in our oscillator design seems to be that representing a variable parasitic impedance on port X and built around the translinear loop[].
The CCII ensures two functionalities between its terminals:

- A Current copy between terminals X and Z.
- A Voltage follower between terminals X and Y.

Thus, in order to get nearly ideal transfers, a CCII should be characterized by low impedance on terminal X and high impedance on terminals Y and Z.
The CCII behaviour taking into account parasitic impedances is given by the following relation:

$$\begin{pmatrix} I_Y \\ V_X \\ I_Z \end{pmatrix} = \begin{pmatrix} \frac{1}{Ry//Cy} & 0 & 0 \\ \beta & Rx & 0 \\ 0 & \alpha & \frac{1}{Rz//Cz} \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix} \quad (4)$$

where α and β are current and voltage transfers of the CCII. R_Y,C_Y and R_Z,C_Z are parasitic resistances on port Y and Z respectively , they are ideally infinite impedances. Rx is the parasitic resistance at port X being ideally a short circuit.

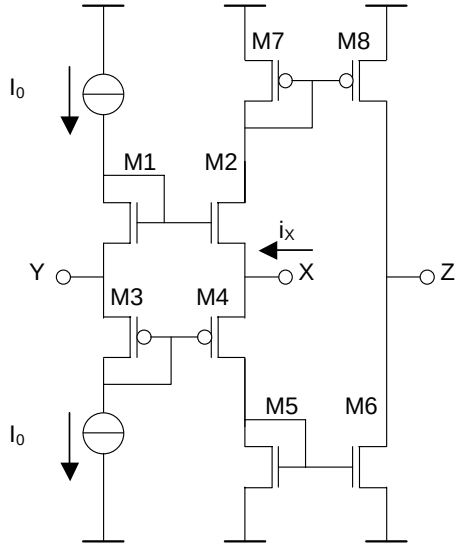

Fig .2: CCII+ implementation using translinear loop

Let's consider the translinear implementation of CCII in fig.2. Assuming the same gain factors for both NMOS and PMOS transistors, the parasitic impedances can be given by the following equations:

$$Rx = \frac{1}{\sqrt{2K_N(\frac{W}{L})_{NX}(1+\lambda_N V_{DS})Io} + \sqrt{2K_P(\frac{W}{L})_{PX}(1+\lambda_P V_{DS})Io}} \quad (5)$$

$$Ry = \frac{1}{\lambda_N Io + \lambda_P Io} \quad (6)$$

$$Rz = \frac{1}{\lambda_N Io + \lambda_P Io} \quad (7)$$

According to this relation, tunable characteristics of R_X can be obtained. A simulated value of RX versus Io shows that this resistance can be controlled between 7.1kΩ and 427Ω by varying the current control in the range [1u-400u].

Simulation results of the oscillator using this CCII implementation leads to a variable frequency ranging from 72.9MHz to 470MHz
Getting higher oscillation frequencies requires a further reduction in the parasitic impedance on port X. Our effort is therefore concentrated on lowering R_X. The translinear loop is worth leading to a voltage transfer of the conveyer nearly ideal with an excellent frequency behaviour as proven above. Therefore, we think to separate in the CCII current conveying path from signal conveying path by making a signal path for the current transfer between ports X and Z presenting very low impedance on port X. A synoptic representation of the structure is shown in Fig3 - [20] .

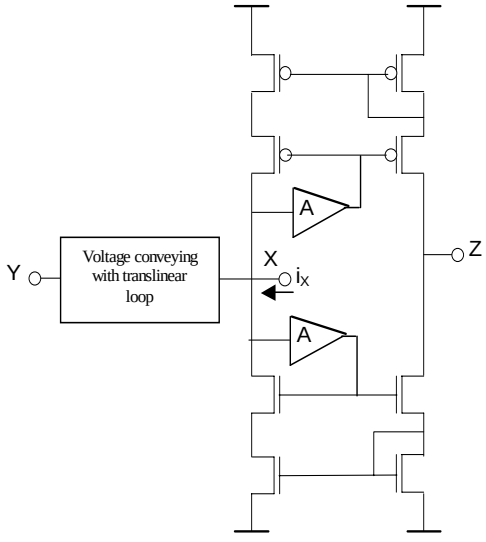

Fig3. A synoptic representation of a low parasitic impedance CCII implementation.

In that scheme, a modified Wilson current mirror is used. The added voltage gain A ensures a lowering of the input impedance by a factor A. In order to lower the quiescent current in this mirror and to get higher output impedance of that mirror, an improved Wilson structure is used. The

remaining point in our design is how to make the voltage gain A dependent to the control current of the translinear structure for preserving the same degree of controllability of the oscillator. This can be done by the presented implementation in Fig.4. Considering the path between X and M7,M8 gates, the voltage gain A is given in eqn (8)

$$A=\left(1+g_m r_o\right) \tag{8}$$

where g_m and r_o are respectively the transconductance and output resistance of transistor M_2.

The corresponding input parasitic resistance at port X is shown in eqn(9)

$$R_X=\frac{1}{g_{m7,8}\left(1+g_{m2}r_{o2}\right)}//\frac{1}{g_{m5,6}\left(1+g_{m4}r_{o4}\right)} \tag{9}$$

Taking into account the accompanying variations of resistances R_Y, small signal analysis of the implemented CCII leads to the theoretical expressions of the parasitic impedances on ports Y and Z respectively given in eqn(10) and eqn(11).

$$R_Y=\left(\frac{1}{g_{m1}}+r_{09}\right)//\left(\frac{1}{g_{m3}}+r_{011}\right) \tag{10}$$

$$R_Z=r_{06}\left(1-\frac{g_{m6}}{4\alpha\sqrt{\beta I_0}}\right)//\,r_{07}\left(1-\frac{g_{m7}}{4\alpha\sqrt{\beta I_0}}\right) \tag{11}$$

where r_{oi} and g_{mi} are respectively the output impedance and the output transconductance of transistors Mi.

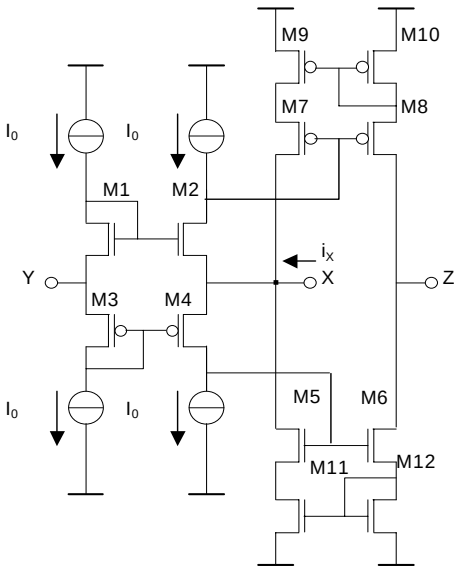

Fig.4:CCII implementation with low parasitic impedance R_X

Fig.5 shows simulated values of R_X versus Io. It is shown in this figure that this resistance can be controlled between 44Ω and 187Ω by varying the current control in the range [1u-400u].

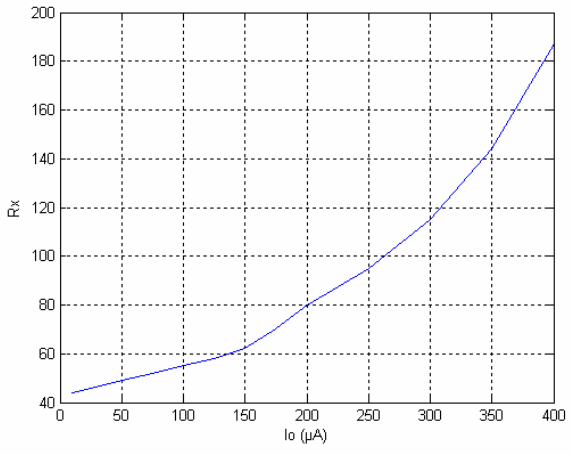

Fig.5. Port X parasitic resistance R_X versus control current Io

According to these theoretical expressions (10, 11), inversion of Rz, variations of R_Y with respect to control current Io can not be ignored. In fact, both transconductances gm1 and gm3 in eqn(10) are dependent on Io. Fig.6 shows simulated parasitic resistances on port Y and Z versus control current Io. According to these results, RY could not be considered constant when varying Io, and their variations should be taken into account.

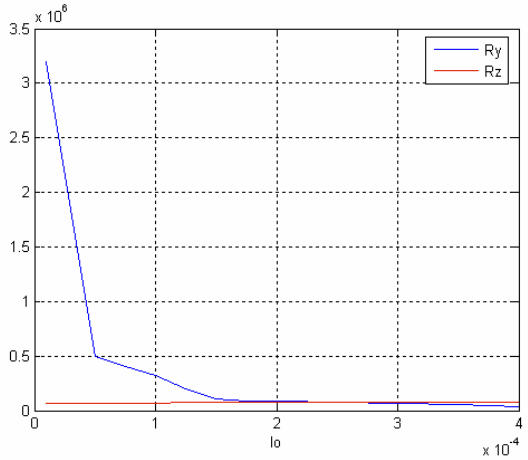

Fig.6. Simulated Parasitic Resistances R_Y and R_Z on port Y and Z respectively versus control current Io

Moreover, simulated current and voltage gains are almost insensitive to the control current Io. Table I summarizes the remaining static characteristics of the CCII.

Table I: Simulated Static characteristics of the CCII

α	1.02
β	0.98
C_Y	63fF
C_Z	23fF

The last point of interest in the CCII characterization is both current conveying and voltage conveying frequency behavior variations with respect to control current Io. The corresponding simulation results are presented in Fig.7.

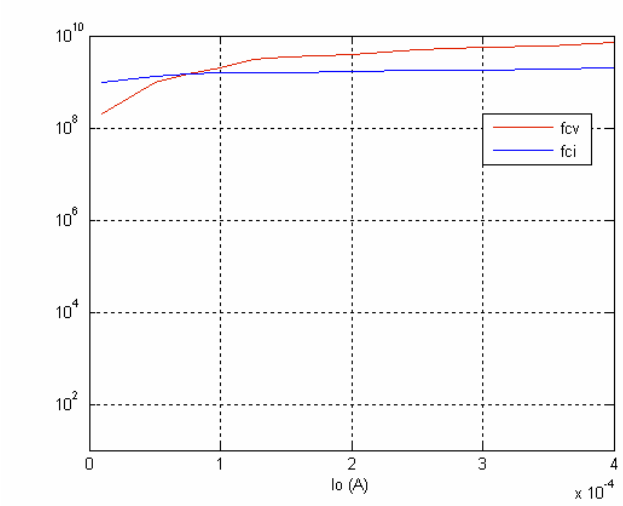

Fig.7. Simulated current conveying and voltage conveying Cut-Off frequencies with respect to control current Io.

Simulation results show a reduction of RX by a factor of 10, ensuring better performances regarding the frequency behaviour of the CCII.

II.3. The new current controlled Oscillator frequency tuning characteristics:

The new structure of oscillator is simulated for different CCII polarisation currents. Simulation results are shown in Fig.8. The oscillation frequency is varied between [100MHz-700MHz] by varying the control current in the range [10u-400uA].

In fact, the parasitic impedances interfere in this relation as shown in table II. This leads to a small shift in the frequency of oscillation.

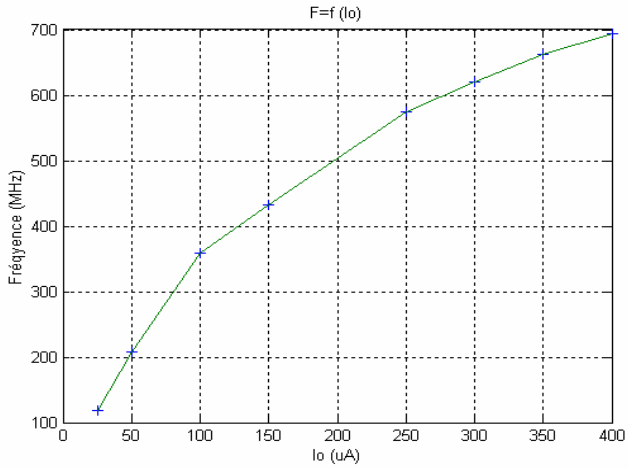

Fig.8. Oscillation Frequency versus control current

Table II. Ideal and actual impedances origin of small shift in the oscillation frequency

Type	C_1	R_2	R_x	R_4	C_5
Ideal	C_1	R_2	R_x	R_4	C_5
Actuel	$C_1+C_{y1}+C_{z1}$	R_2+R_{x1}	R_{x3}	(R_4+R_{x4}) //R_{z3}// R_{z1}	$C_5+C_{y3}+C_z$

A more accurate expressions tking into account the most important parasitic resistance is given by:

$$\omega_o^2 = \frac{\frac{1}{R_{Y1}}\frac{1}{R_{Y3}} + \frac{1}{R_{X3}}\frac{1}{R_4}}{C_5\left(C_2 - C_1\right)} \qquad (12)$$

III- General Approach of minimizing phase noise in controlled oscillators:

The output of an ideal sinusoidal oscillator can be expressed by:

$$s(t) = A_0 \sin\left(\omega_0 t + \phi_0\right) \qquad (13)$$

where A is the amplitude of the oscillator, ω_0 is the frequency of oscillation and ϕ_0 is an arbitrary fixed phase reference.

According to this relation, the power spectrum density is ideally composed of a pair of pulses at $\pm\omega_0$. However, the presence of noise leads to fluctuations in the phase reference $\phi(t)$ and the amplitude $A(t)$, which creates frequency side bands close to the frequency of oscillation ω_0 .One

way of evaluating these fluctuations is to use the single side band power at a frequency offset of $\Delta\omega$ [18].

In order to evaluate the single side band power, we consider the oscillator as a feed back system and each noise source as an input In as represented in Fig 9. The phase noise observed at the output is a function of the noise source In shaped by the transfer function between the node where the noise is injected and the oscillator output.

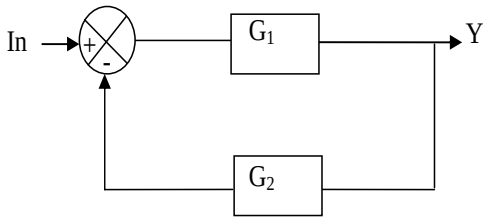

Fig 9. Feed-Back Oscillator System Model

According to Fig.6 and using the assumption of a small signal analysis model, the noise shaping function at an offset $\Delta\omega$ is thus given by:

$$\frac{|Y|^2}{|In|^2} = \frac{|G_1|^2}{\Delta\omega^2 \left|\frac{dH}{d\omega}\right|^2} \quad (14)$$

Where H is the open loop oscillator transfer function and G_1 is the transfer function between the injected noise and the oscillator output.

In class A operations, we can assume that the phase noise remains the same during oscillations. Therefore, one can evaluate phase noise by considering the quiescent point of the different transistors and their corresponding level of impedances. We adopt in the following sections this linear invariant model.

With the assumption that the different device noise sources are non correlated, we can generalize this approach and get for the output phase noise the following expression:

$$J_{tot} = \sum |F_i|^2 |I_{ni}|^2 \quad (15)$$

where $|F_i|$ is the noise shaping function of the noise source I_{ni}. For MOS device, we consider a random device noise current $i_n(t)$ whose Power Spectral Density is formed with a flat region and $1/f$ region.

$$\bar{i^2}_n = \bar{i^2}_{th} + \bar{i^2}_{1/f} = \frac{8.K.T.g_m}{3} + \frac{KF}{f^{AF}.C_{OX}.Leff.Weff}.g^2m \quad (16)$$

where gm is the channel transconductance, K *is* the Boltzmann constant, T is the absolute temperature, f *is* the frequency, C_{OX} is the gate capacitance per unit area, *Weff* and *Leff* are respectively the channel length and width, and AF and KF are user-defined parameters which are heavily dependent on the used technology [19] .

An optimization of the oscillator phase noise should be achieved once a study of the different electrical noise sources and the way they are transferred to the oscillator output node.

Our methodology in minimizing phase noise consists on the optimization of the related objective noise function J_{tot} under two equality constraints g_1 fixing the oscillation frequency and g_2 preserving the condition of oscillation. The objective function is expressed as follows:

$$\text{Min } J_{tot}\left(\underbrace{W_i, L_i}_{i=1,\ldots}, \underbrace{I_j}_{j=1,\ldots}\right) \text{ under } g_1 = 0 \text{ and } g_2 = 0 \quad (17)$$

Where W_i, L_i (i=1,…) are transistor geometries of the different MOS devices and I_j (j=1,…) are the different current sources interfering in the oscillator design.

IV. Phase noise Modelling

Optimization of the noise in the conveyors can be made independently of the structure of the oscillator. In order to evaluate each CCII phase noise, we apply a linear invariant model. Thus, we get a generic model depending only on device geometries and current sources. A small signal analysis model is thus applied taking as source drain resistance and canal transconductance respectively the following expressions:

$$rdsi = \frac{1}{\lambda.Idi} \quad (18)$$

$$g_{mi} = \sqrt{2\frac{W}{L}\mu.C_{ox}.I_{di}} \quad (19)$$

where λ is the early coefficient factor and *Idi* are the corresponding drain currents.

Once we determine a generic model of the CCII, the total equivalent noise in the output of the oscillator can be written as follows:

$$\bar{i}_{total}^{\,2} = \left(\bar{i}_{Z1}^{\,2} + \bar{i}_{Z3}^{\,2}\right) \frac{|G|^2}{(\Delta w)^2 . \left|\frac{dH}{dw}\right|^2} + \bar{i}_{Z2}^{\,2} \qquad (20)$$

Where $\bar{i}_{Z1}^{\,2}$, $\bar{i}_{Z2}^{\,2}$ and $\bar{i}_{Z3}^{\,2}$ are the equivalent spectral density of the current conveyers①, ② and ③ respectively.

V. PHASE NOISE OPTIMIZATION AND SIMULATION RESULTS

The heuristic we use for optimizing Phase noise oscillator and current conveyor performances is essentially a random procedure; it consists of the following steps [16,20]: The first step consists of building mathematical models for both constraints and preliminary conditions to satisfy. They are necessary to insure saturation of all transistors, complimentarily, symmetry between PMOS and NMOS branches and a dynamic range up to 50% of supply voltage. All relations were programmed by mean of C++ software. This program gives all possible quiescent parameters, which are candidate for the second optimization step. The second step is the optimization approach. Firstly, performance the total equivalent noise in the output of the oscillator, the oscillation frequency and The CCII parasitic resistance are mathematically modelled, as introduced in section II and III. These relations are then taken into consideration in the C++ program thus optimal parameters can be selected between the already calculated quiescent parameters. We notice that a function of merit (Fob) was built for this purpose, it is given at eq(21):

$$Fob = \bar{i}_{total}^{\,2} + a_1 \frac{(f - fo)}{fo} + a_2 \frac{\text{condosc}}{R_2} + a_3 Rx + \frac{a_4}{(Ry + Rz)} \qquad (21)$$

where $a_1, ..., a_4$ are positive coefficients used for normalization.

It is important to notice that for a precise convergence of the algorithm to optimal parameters, we need to correct constants values such as those used for the calculus of MOS conductance. So we have to do simulations with obtained parameters then correct constants values and re-run the algorithm and so on until full convergence of obtained results [17] figure.10 summarizes different steps of this optimization procedure.

The adopted optimization approach is an algorithm driven methodology which consists of minimizing X port input resistance value, maximizing Y and Z ports resistance values, minimizing the total equivalent noise in the output of the oscillator. Simulation conditions are presented in table I

TableIII: Simulation conditions

Technology	0.35µm CMOS AMS
Supply voltage	3.3V
Bias current	100uA

In table II are presented the obtained optimal transistors sizes (w and L).

Table VI: Transistors geometric dimensions

Device Name	**Aspect ratio W/L**
M1, M2	16.35/1(µm)
M3, M4	26.65/0.6(µm)
Mxx (in PMOS current mirrors)	18.9/0.35(µm)
Mxx (in NMOS current mirrors)	7/0.35(µm)

VII.The minimum phase noise oscillator characterisation :

A comparison was made between three different dimensions which the third is the optimised structure, in order to show the importance of such optimisation.

Table V: three different dimensions of the CCII

Structure	**Device Name**	**Aspect ratio W/L**
1	M1, M2 M3, M4	16.35/1(µm) 30/0.6(µm)
2	M1, M2 M3, M4	16.35/1(µm) 28/0.6(µm)
3	M1, M2 M3, M4	16.35/1(µm) 26.65/0.6(µm)

The figure.11 presents the harmonic study of three forms. On the one hand, we notice that the optimized structure presents the greatest shift between the two first harmonics and presents a minimum distortion harmonic about 1.22%. On the other hand , the others present two THD about 1.44% and 1.66%.

VII. Conclusion

In this paper, we have presented a design of variable frequency current controlled oscillators. In order to get high frequency performances of the oscillator, a translinear CCII structure with low parasitic resistance RX is presented in 0.35µm CMOS process of AMS. Simulation results show that this new oscillator provides an independent control of oscillation frequency and oscillation condition in the range [100MHz-700MHz] by varying the control current in the range [10u-400uA].

Phase noise characteristics of the proposed oscillator are investigated. We have presented then a new methodology of modelling and optimisation of phase noise in current controlled oscillators for CMOS process. This optimization strategy leads to a minimum phase noise acting on device geometries and design sources. Our optimization started with a determination of the contribution of each component in the total circuit. Then it is followed by an evaluation of the transfer functions which bring back the noise of the different components to the output of the conveyor and then to the output of the oscillator.

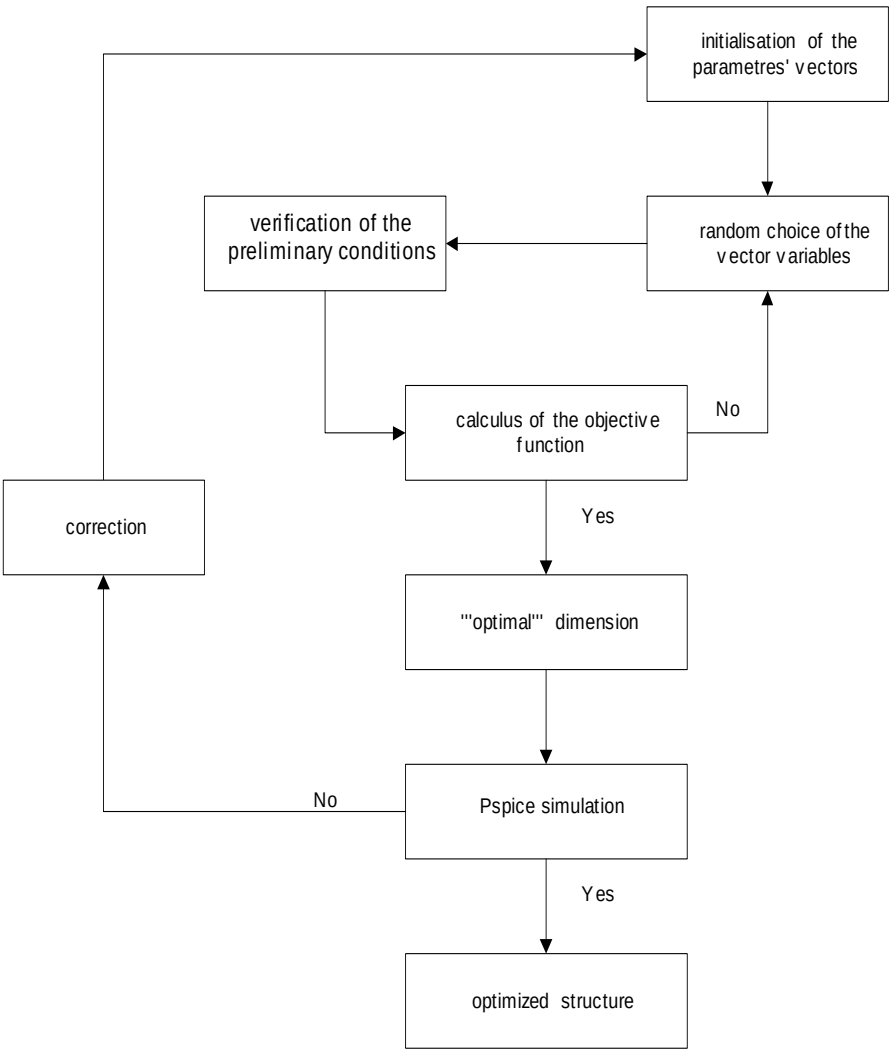

Fig.10 The adopted optimization approach

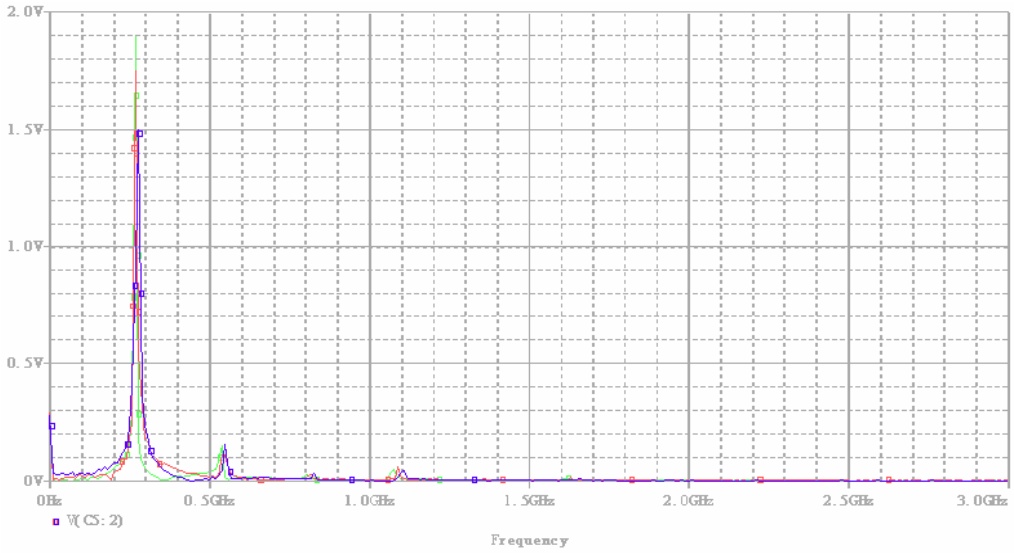

Fig.11 The harmonic simulation

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