Design of Accurate Power Factor Measurement Approach Using FPGA-based Chip

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Abstract: - In recent years, power electronic components introduce harmonic pollution on electric power systems. It makes the traditional electromechanical power meter can not act accurately when it feeds unbalanced and harmonic loads. Power quality analysis now tends to use digital signal technology. But it is hard to avoid measurement errors in estimating power quality by digital signal technology. In this paper, it is to improve the computation errors by using FPGA. The simulation circuits were created and measured by Matlab. Then it will discuss the case of single-phase full-wave bridge rectifier loads. And then in the three-phase circuit the effective power factor, arithmetic power factor, and fundamental power factor will be compared in several simulation cases. The computation errors have been greatly reduced. In the study, the Fast Fourier Transform (FFT) is used to analyze the formula of power factor. The simulation system was modeled in Hardware Description Language (VHDL) and some novel IP (intellectual property) cores, such as CORDIC core and FFT core by the way of Bottom-Up. Design of SOC (System on a Chip) is a trend to achieve the strong and small volume in the future.

Key-Words: - Power Quality, Harmonic, Unbalance, FPGA, FFT.

1 Introduction

If inductive electro-mechanical (rotating disc type) three-phase kWh and kVarh meters are used, the power quantities essentially only contain the fundamental components and neglect effects of imbalance. The results of power metering cannot really reveal the problems of load fluctuation, load imbalance, and harmonics. It has been reported that if traditional electro-mechanical meters are used in circumstances of non-sinusoidal and unsymmetrical voltages or currents, the errors can reach 20%~30%. Thereafter in recent years, there are many discussions regarding the power factor definitions and calculations. Several definitions have been given in the IEEE Standard 1459-2000, such as effective apparent power, arithmetic apparent power, vector apparent power, and corresponding power factors [1-13].

The usage and performance of FPGA has risen significantly in recent years for its reconfigurability and flexibility. The FPGA has been applied to analyzing and controlling a power system [14-33]. The major difference between FPGA and DSP-based solutions is that FPGA enables simultaneous execution of all control subroutines, which allows high performance and novel control methods. While conventional designs are based on functions, FPGA is based on the reuse of IP or the function assembly. When a large system is constructed from a number of macro-modules, IP cores can be used to represent those modules. Several particular functional IP cores such as CORDIC and FFT cores could be developed. VHDL was also employed to model a digital control system at many levels. VHDL can be considered as a combination of sequential, concurrent, timing specification, and waveform generation languages. It utilizes the top/down design methodology and can be used to model a complete digital electronic system. The design benefits include easy error correction and technology independence. The same algorithm can be synthesized into any other FPGA.

In this paper, six average power factor definitions, three by the IEEE Standard 1459-2000 and three only considering fundamental components

are compared. The effects of harmonic, imbalance, and load fluctuation are investigated. The effective power factor and the 2nd modified fundamental power factor could be better choices when load fluctuation, load imbalance, and harmonics are fairly considered. In this paper, the calculation approaches for power factor values are developed by using the FPGA. Several power factor definitions have been compared. The effects of unbalance and harmonics are considered in calculating the power factor values. Power electronic circuits are used to represent the nonlinear loads. To reduce the computation errors, several approaches are compared, which consider algorithm causing errors and floating-point errors. From the study results, the computation errors can be greatly reduced by a well design computation method.

2 Power Factor Definitions

2.1 Power and Power Factor

The definitions for a single-phase circuit are helpful in understanding the situations of a three-phase system. For a single-phase load under sinusoidal conditions and non-harmonic, the instantaneous voltage and current are, respectively,

$$v(t) = \sqrt{2}V\sin(\omega t + \alpha) \quad (1)$$

$$i(t) = \sqrt{2}I\sin(\omega t + \beta) \quad (2)$$

Hence the apparent power, active power, reactive power, and power factor are, respectively,

$$S = VI \quad (3)$$

$$P = VI\cos\theta \quad (4)$$

$$Q = VI\sin\theta \quad (5)$$

$$PF = \frac{P}{S} = \frac{P}{\sqrt{P^2 + Q^2}} \quad (6)$$

where $\theta = \alpha - \beta$ is the phase angle difference between voltage and current.

Nevertheless, for a single-phase load under non-sinusoidal conditions, the instantaneous voltage and current are, respectively,

$$v(t) = V_0 + \sqrt{2}\sum_{h\neq 0}^{\infty} V_h \sin(h\omega t + \alpha_h) \quad (7)$$

$$i(t) = I_0 + \sqrt{2}\sum_{h\neq 0}^{\infty} I_h \sin(h\omega t + \beta_h) \quad (8)$$

where V_o is DC voltage.

I_o is DC current.

V_h is the fundamental harmonic voltage, $h = 1, 2, \ldots$

α_h is the fundamental harmonic voltage phase angle.

I_h is the fundamental harmonic current.

β_h is the fundamental harmonic current phase angle.

The RMS values are

$$V = \sqrt{\sum_{h=0}^{\infty} V_h^2} \quad (9)$$

$$I = \sqrt{\sum_{h=0}^{\infty} I_h^2} \quad (10)$$

Hence the apparent power is

$$S = VI \quad (11)$$

The active power (average power) is

$$P = \sum_{h=0}^{\infty} V_h I_h \cos(\alpha_h - \beta_h) = P_1 + P_H \quad (12)$$

The active power includes the fundamental active power $P_1 = V_1 I_1 \cos(\alpha_1 - \beta_1)$ and the harmonic active power $P_H = P - P_1$. Since there are many definitions for reactive power under non-sinusoidal conditions, the most popular Budeanu's reactive power is chosen in this paper [5]. It is given by

$$Q_B = \sum_{h=0}^{\infty} V_h I_h \sin(\alpha_h - \beta_h) \quad (13)$$

And the power factor is

$$PF = \frac{P}{S} \neq \cos(\tan^{-1}\frac{Q_B}{P}) \quad (14)$$

The Budeanu's distortion power can be given as

$$D_B = \sqrt{S^2 - P^2 - Q_B^2} \quad (15)$$

In the three-phase conditions, there are many definitions under different considerations. In Taiwan, the Taipower does not provide neutral lines to customers in 161-kV, 69-kV, and 11.4/22.8-kV voltage levels. These customers can be seen as three-phase three-wire (3Φ 3W) loads.

The arithmetic apparent power of a three-phase three-wire load under non-sinusoidal and unbalanced conditions is [5]

$$\begin{aligned} S_A &= V_R I_R + V_S I_S + V_T I_T \\ &= S_R + S_S + S_T \\ &= \sqrt{S_{R1}^2 + S_{RN}^2} + \sqrt{S_{S1}^2 + S_{SN}^2} + \sqrt{S_{T1}^2 + S_{TN}^2} \end{aligned} \quad (16)$$

It is noted that S_A is the direct sum of each phase apparent power, so that it cannot reveal the load imbalance. But harmonic components are fully considered. The arithmetic power factor is

$$PF_A = \frac{P}{S_A}, \quad P = P_R + P_S + P_T \quad (17)$$

If the three-phase active power, reactive power, and distortion power are considered individually, the vector apparent power can be defined as

$$\begin{aligned} S_V &= \sqrt{\left(P_R + P_S + P_T\right)^2 + \left(Q_{BR} + Q_{BS} + Q_{BT}\right)^2 + \left(D_{BR} + D_{BS} + D_{BT}\right)^2} \\ &= \sqrt{P^2 + Q_B^2 + D_B^2} \\ &= \sqrt{(P_1 + P_H)^2 + (Q_1 + Q_H)^2 + D_B^2} \end{aligned} \quad (18)$$

And the corresponding vector power factor is

$$PF_V = \frac{P}{S_V} \quad (19)$$

It is always $S_V \le S_A$, because signs of active power, reactive power, and distortion power of each phase may be different.

Another definition is based on the effective consideration of voltages and currents [5]. The RMS values are

$$V_e = \sqrt{\frac{V_R^2 + V_S^2 + V_T^2}{3}} \quad (20)$$

$$I_e = \sqrt{\frac{I_R^2 + I_S^2 + I_T^2}{3}} \quad (21)$$

The effective apparent power is

$$S_e = 3V_e I_e = \sqrt{\begin{aligned} &\left(V_R I_R\right)^2 + \left(V_R I_S\right)^2 + \left(V_R I_T\right)^2 \\ &+ \left(V_S I_R\right)^2 + \left(V_S I_S\right)^2 + \left(V_S I_T\right)^2 \\ &+ \left(V_T I_R\right)^2 + \left(V_T I_S\right)^2 + \left(V_T I_T\right)^2 \end{aligned}} \quad (22)$$

Since RMS values are used, harmonics components are included. In a relative unbalanced condition, for example, if $I_T = 0$ but V_T is given, it can be found that $S_e \ge S_A$, by comparing (16) and (22). It has been reported that the effective apparent power is more suitable to reveal the power line losses caused by unbalanced loads. The effective power factor is

$$PF_e = \frac{P}{S_e} \quad (23)$$

If a three-phase four-wire (3Φ 4W) loads, the effective current and voltage are, respectively,

$$\mathrm{I_e} = \sqrt{\frac{\mathrm{I_R^2 + I_S^2 + I_T^2 + I_N^2}}{3}} \quad (24)$$

$$\mathrm{V_e} = \sqrt{\frac{1}{18}\left[3\left(\mathrm{V_R^2 + V_S^2 + V_T^2}\right) + \left(\mathrm{V_{RS}^2 + V_{ST}^2 + V_{TR}^2}\right)\right]} \quad (25)$$

In some circumstances, only fundamental components are considered and power factors are calculated indirectly using fundamental active powers and reactive powers. For examples, if inductive electro-mechanical (rotating disc type) kW and kVar meters are used, only fundamental components could be obtained, considering the frequency responses of meters. Then the fundamental (displacement) power factor is

$$PF_1 = \cos\left(\tan^{-1}\frac{Q_1}{P_1}\right) \quad (26)$$

Where

$$P_1 = P_{R1} + P_{S1} + P_{T1} \quad , \quad Q_1 = Q_{R1} + Q_{S1} + Q_{T1} \quad (27)$$

Then the corresponding fundamental apparent power is

$$S_1 = \sqrt{P_1^2 + Q_1^2} \quad (28)$$

However, if unidirectional (anti-reverse) kVar meters for fundamental components are used, the first modified fundamental power factor would be

$$PF_{1m1} = \cos\left(\tan^{-1}\frac{Q_{1m1}}{P_1}\right) \quad (29)$$

Where

$$Q_{1m1}(t)=\begin{cases} Q_1(t) & Q_1(t)\ge 0 \\ 0 & Q_1(t)<0 \end{cases} \quad (30)$$

And

$$S_{1m1}=\sqrt{(P_1)^2+(Q_{1m1})^2} \quad (31)$$

Equation (30) means that leading reactive powers could be accepted by the utility, and only lagging reactive powers should be included in revenue.

If both lagging and leading fundamental reactive powers from customers are not desired, there is also the second modified fundamental power factor as

$$PF_{1m2}=\cos\left(\tan^{-1}\frac{Q_{1m2}}{P_1}\right) \quad (32)$$

Where

$$Q_{1m2}(t)=|Q_1(t)| \quad (33)$$

And

$$S_{1m2}=\sqrt{(P_1)^2+(Q_{1m2})^2} \quad (34)$$

2.2 Average Power Factor

In the revenue practice for large-size users, the average power factor values of a fixed period, such as a month, may be used. Therefore, there are three definitions for the average power factor if harmonics are considered.

$$PF_A=\frac{\int_T P(t)\,dt}{\int_T S_A(t)\,dt},\quad PF_V=\frac{\int_T P(t)\,dt}{\int_T S_V(t)\,dt},\quad PF_e=\frac{\int_T P(t)\,dt}{\int_T S_e(t)\,dt} \quad (35)$$

There are also three average power factor values if only fundamental components are considered.

$$PF_1=\cos\tan^{-1}\frac{\int_T Q_1(t)\,dt}{\int_T P_1(t)\,dt},\quad PF_{1m1}=\cos\tan^{-1}\frac{\int_T Q_{1m1}(t)\,dt}{\int_T P_1(t)\,dt},\quad PF_{1m2}=\cos\tan^{-1}\frac{\int_T Q_{1m2}(t)\,dt}{\int_T P_1(t)\,dt} \quad (36)$$

The six power factor definitions can be divided two groups. The first group is the three definitions where their differences are dominated by the choices of apparent powers and affected by harmonics and load imbalance. The second group is focused on the fundamental components, and they are affected by the consideration methods of fundamental reactive power fluctuation.

2.3 Harmonic and Unbalanced Powers

Some power quantities are useful to represent the conditions of harmonics and imbalance. The effective representation of three-phase four-wire and three-phase three-wire fundamental voltages and currents can be given as (37)-(38) and (39)-(40), respectively,

$$V_{e1}=\sqrt{\frac{1}{18}\left[3\left(V_{R1}^2+V_{S1}^2+V_{T1}^2\right)+\left(V_{RS1}^2+V_{ST1}^2+V_{TR1}^2\right)\right]} \quad (37)$$

$$I_{e1}=\sqrt{\frac{I_{R1}^2+I_{S1}^2+I_{T1}^2+I_{N1}^2}{3}} \quad (38)$$

$$V_{e1}=\sqrt{\frac{V_{R1}^2+V_{S1}^2+V_{T1}^2}{3}} \quad (39)$$

$$I_{e1}=\sqrt{\frac{I_{R1}^2+I_{S1}^2+I_{T1}^2}{3}} \quad (40)$$

Then the fundamental effective apparent power is

$$S_{e1}=3V_{e1}I_{e1} \quad (41)$$

It is noted that S_{e1} is different from S_1. The non-fundamental effective apparent power to reveal harmonic components is

$$S_{eN}=\sqrt{S_e^2-S_{e1}^2} \quad (42)$$

The normalized non-fundamental effective apparent power, S_{eN}/S_{e1}, can be used to reveal the harmonic distortion degree of load powers.

When there is an unbalanced circuit, the fundamental positive-sequence apparent power is

$$S_1^+ = 3V_{e1}^+ I_{e1}^+ \tag{43}$$

Where $V_{e1}^+ = 1/3\left(\mathrm{V_{R1}} + \mathrm{aV_{S1}} + \mathrm{a^2 V_{T1}}\right)$ and $I_{e1}^+ = 1/3\left(\mathrm{I_{R1}} + \mathrm{aI_{S1}} + \mathrm{a^2 I_{T1}}\right)$, $\mathrm{a} = 1\angle 120^0$ are the fundamental positive-sequence components.

Therefore the unbalanced components can by represented by the fundamental unbalanced apparent power as

$$S_{1U} = \sqrt{S_{e1}^2 - S_1^{+2}} \tag{44}$$

By the way, the normalized fundamental unbalanced apparent power, S_{1U} / S_1^+ , can be used to reveal the degree of load imbalance.

3 System Module

The FFT algorithm is used to calculate the fundamental and harmonic components of each phase voltage and current per power cycle as shown in Figure 1. Each FFT uses 64 samples.

(1) FFT module

The Fast Fourier Transform (FFT) is a computationally efficient algorithm for deriving the Discrete Fourier Transform (DFT). The FFT core developed by Xilinx can compute an *N*-point forward DFT or inverse DFT (IDFT) where $N = 2^m, m = 4 \sim 14$. The FFT core applies the Cooley-Tukey decimation-in-time (DIT) algorithm to determine the DFT.

(2) Quantification module

The FFT module outputs 16-bit frequency domain data samples for both the real and imaginary components are fed into this module that picks out the complex pair corresponding to a target frequency. The squared root operation is also implemented using the simplified CORDIC algorithm. The harmonic component magnitudes are then computed.

4 Primary Test

The most important issue in designing the calculation IC is the choice of numerical data processing scheme. Floating-point arithmetic has the advantage of a wide dynamic range, but its hardware realization is very complicated. Fixed-point arithmetic is a more practical solution to most industrial applications than floating-point arithmetic owing to its simple circuit realization. The proper numerical scaling plays a very significant role in synthesizing an integer controller. In this study, numerical variables and parameters must be transformed into approximate integers with finite word lengths.

FPGA has become the main stream in complex logic circuit design owing to its flexibility, ease of use and short time to market. The programmable hard-wired feature of FPGA provides a solution to the conflict between the demanding computation requirements and the cost. Therefore, FPGA can be beneficially applied as part of a digital controller to relieve the microprocessor from time-consuming computations. In the application of an arc furnace power system, the IC should serve as a coprocessor with a general-propose microprocessor to provide interface function.

This investigation presents a novel digital circuit design methodology, in which all modules were described by using VHDL, and a synthesis tool, ISE, was adopted to map these designed codes directly onto FPGA. A design implementation software application, Modelsim, was utilized to obtain results. The logic and timing simulation software is (especially OR particularly) important for the design of complicated digital circuits, because can resolve circuit problems during the early design stage. Xilinx's tool was applied to implement this design.

To verify the effect of harmonic distortion and imbalance load was performed using MATLAB and FPGA simulation methods.

(1) The system is supplied by a three-phase three-wire symmetrical voltage source as Figure 2. The base values are 24 kVA and 220 V.

(2) The three-phase load is composed of parallel RLC load black and harmonic current source black.

(3) The measurement block of voltages and currents were performed using the three-phase instantaneous voltages and currents.

The situations of a three-phase non-harmonic system, the fundamental active and reactive power are 5kw and 1.65kVar, respectively. The means power factor is 0.9496.

(4) To reveal the power and power factor by using FPGA measures the instantaneous voltages and currents. The measurement data were employed to calculate the six formula of power factor. Compare the simulation results of FPGA and Matlab, the error rate can be defined as

$$\varepsilon(\%) = \frac{PF_{(\mathrm{FPGA})} - PF_{(\mathrm{Matlab})}}{PF_{(\mathrm{Matlab})}} \times 100\% \tag{45}$$

Table 1 and Table 2 list the six formula of power factor, which were performed using Matlab and FPGA simulation methods. The calculation results using FPGA were approximately equal to these using Matlab. So the error rate is small.

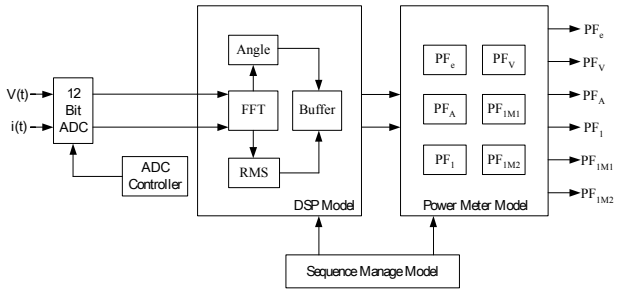

Figure 1. System Module

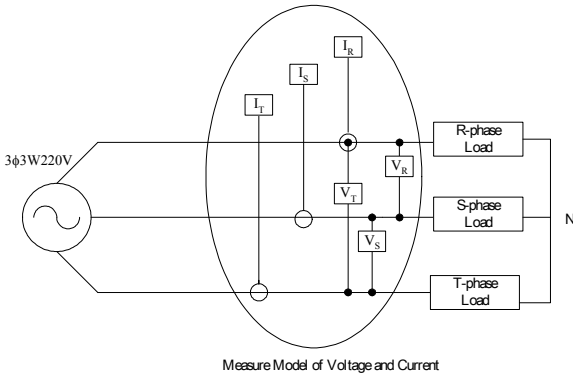

Figure 2. Three-Phase Three-Wire System

Table 1. Power Factor Using Matlab and FPGA of the First Group

$\frac{S_{1U}}{S_1^+}$(%)	PF_e			PF_A			PF_V		
	Matlab	FPGA	ε(%)	Matlab	FPGA	ε(%)	Matlab	FPGA	ε(%)
0	0.6702	0.6703	0.0189	0.6702	0.6698	-0.0576	0.6702	0.6698	-0.0578
5	0.6698	0.6699	0.0170	0.6700	0.6696	-0.0595	0.6702	0.6698	-0.0593
10	0.6685	0.6686	0.0202	0.6693	0.6689	-0.0571	0.6702	0.6698	0.0582
15	0.6663	0.6665	0.0273	0.6682	0.6679	-0.0489	0.6702	0.6699	0.0489
20	0.6633	0.6634	0.0142	0.6666	0.6663	-0.0523	0.6702	0.6699	-0.0541
25	0.6595	0.6597	0.0270	0.6646	0.6643	-0.0489	0.6703	0.6699	-0.0525
30	0.6550	0.6551	0.0198	0.6621	0.6618	-0.0513	0.6703	0.6699	-0.0538
35	0.6497	0.6498	0.0207	0.6591	0.6588	-0.0470	0.6703	0.6699	-0.0534
40	0.6438	0.6439	0.0158	0.6556	0.6553	-0.0527	0.6703	0.6699	-0.0548
45	0.6373	0.6375	0.0343	0.6517	0.6514	-0.0389	0.6703	0.6700	-0.0446
50	0.6302	0.6303	0.0205	0.6472	0.6469	-0.0420	0.6703	0.6700	-0.0495
55	0.6227	0.6228	0.0145	0.6423	0.6420	-0.0446	0.6704	0.6700	-0.0518

Table 2. Power Factor Using Matlab and FPGA of the Second Group

$\frac{S_{1U}}{S_1^+}$(%)	PF_1			PF_{1M1}			PF_{1M2}		
	Matlab	FPGA	ε(%)	Matlab	FPGA	ε(%)	Matlab	FPGA	ε(%)
0	0.9496	0.9496	0.0017	0.9496	0.9496	0.0017	0.9496	0.9496	0.0017
5	0.9496	0.9496	0.0006	0.9496	0.9496	0.0006	0.9496	0.9496	0.0006
10	0.9496	0.9496	0.0006	0.9496	0.9496	0.0006	0.9496	0.9496	0.0006
15	0.9497	0.9496	-0.0004	0.9497	0.9496	-0.0004	0.9497	0.9496	-0.0004
20	0.9497	0.9496	-0.0004	0.9497	0.9496	-0.0004	0.9497	0.9496	-0.0004
25	0.9497	0.9496	-0.0004	0.9497	0.9496	-0.0004	0.9497	0.9496	-0.0004
30	0.9497	0.9496	-0.0015	0.9497	0.9496	-0.0015	0.9497	0.9496	-0.0015
35	0.9497	0.9496	-0.0015	0.9497	0.9496	-0.0015	0.9497	0.9496	-0.0015
40	0.9497	0.9496	-0.0015	0.9497	0.9496	-0.0015	0.9497	0.9496	-0.0015
45	0.9497	0.9496	-0.0025	0.9497	0.9496	-0.0025	0.9497	0.9496	-0.0025
50	0.9497	0.9496	-0.0025	0.9497	0.9496	-0.0025	0.9497	0.9496	-0.0025
55	0.9497	0.9496	-0.0036	0.9497	0.9496	-0.0036	0.9497	0.9496	-0.0036

5 Improvement Method of Accuracy

To improve the accuracy of power factor calculation in FPGA, the errors of measurement should include algorithm errors and floating-point errors. The content is mainly the 12-bit input-pins for programming design.

(1) Algorithm causing error

The algorithm deviation usually comes from the irrational operation. The HDL (Hardware Description Language) is often involved with irrational numbers. It lets the binary system hard to describe the power formula. In the program process, the instantaneous voltage and current values are simulated by Matlab module. And then it transfers the signals from time-domain to frequency-domain by Xilinx FFT core. In frequency domain, the real and imaginary components are used to calculate each order of voltage and current harmonic components by $(\sqrt{2}/64)\times\sqrt{xk_{re}(n)^2+xk_{im}(n)^2}$. But the value of $\sqrt{2}/64$ can not be effectively calculated in FPGA. Nominally, it will be multiplied by 2^n to improve the deviation. The deviation will be reduced when the order increases.

In the following, two mathematic functions in simulation will be compared to reveal how to improve the values for best solution.

Method 1:

In the programming, the value of frequency domain parameter $(\sqrt{2}/64)\times 2^{16}=1448.154688$ will have a corresponding binary system value of 1448 for calculation. Obviously, the result of calculation will have deviation because the value of 0.152688 is omitted in the binary system. And the multiply value 2^{16} will involve the problem of system complex. Table 3 and Table 4 show the result of calculation, and simulation calculation procedure as following:

(a) The effective voltage value is 120.2077V, and all instantaneous values will be divided by the peak value of 170 for normalization.

(b) The calculation of effective current values is the same way. All instantaneous values will be divided by the peak value for normalization.

(c) The normalized values are multiplied by 2048 in FPGA to increase read/write number and therefore improve the accuracy.

Table 3. Fundamental Component Calculation Result in Mathod1

	S_1(VA)	P_1(W)	Q_1(Var)	PF_1
MATLAB	255.27	244.02	74.943	0.9559
FPGA	254.93	243.69	74.884	0.9559
Error(%)	0.1323%	0.1363%	0.0787%	-0.005%

Table 4. Power Quantity Computing Result in Mathod1

	P(W)	Q(Var)	S(VA)	D
MATLAB	244.02	74.943	333.25	214.23
FPGA	243.69	74.884	332.54	213.52
Error(%)	0.136%	0.078%	0.215%	0.332%

Table 5. Fundamental Component Computing Result in Method 2

	S_1(VA)	P_1(W)	Q_1(Var)	PF_1
MATLAB	255.27	244.02	74.94	0.9559
FPGA	255.20	243.94	74.96	0.9559
Error(%)	0.027%	0.032%	-0.026%	0.001%

Table 6. Power Quantity Computing Result in Method 2

	P(W)	Q(Var)	S(VA)	D
MATLAB	244.02	74.943	333.25	214.23
FPGA	243.92	74.991	333.15	214.16
Error(%)	0.040%	-0.070%	0.0323%	0.0345%

Table 7. Fundamental Component Calculation Results with Improved Floating-point Error

	S_1(VA)	P_1(W)	Q_1(Var)	PF_1
MATLAB	255.270	244.021	74.943	0.9559
FPGA	255.025	243.759	74.959	0.95583
Error(%)	0.0959%	0.1073%	-0.0215%	0.0078%

Table 8. Power Quantity Computing Results with Improved Floating-Point Error

	P(W)	Q(Var)	S(VA)	D
MATLAB	244.021	74.943	333.252	214.23
FPGA	243.697	74.985	332.847	213.95
Error(%)	0.1327%	-0.0549%	0.1218%	0.1289%

Method 2:

In the programming, the frequency domain components will be multiplied by $(2/64)\times 2^5 = 1$. So there is no floating point calculation. The bit number of 2^5 is smaller, so that the accuracy can be increased. Table 5 and Table 4 show the result of calculation.

(2) Floating-point error

In the digital system, floating point calculations need large circuit field and operation time. In order to save the chip utilization rate, the voltage and current instantaneous values will be normalized and then be multiplied by an integer number before FPGA reads the values. It can reduce the errors. Normally, the integer value is bigger; the floating point error will be smaller. For example, if the input signals are 12-bit values, the multiplied value could be 2048 after the normalization. Of course it can adjust input bit number for more accurate input signals. But the chip utilization rate will increase. Table 7 and Table 8 show the result of calculation, and simulation calculation procedure as following:

(a) The effective voltage value is 120.2077V. All instantaneous values will be divided by the peak value 170 for normalization.

(b) The effective current values are treated in the same way. All instantaneous value will be divided by the peak current value for normalization.

(c) Normalized values of voltage and current are multiplied by 1000 in FPGA to increase read/write number. And to compare with the method-3 which multiply by 2048.

6 Test of System with Nonlinear Load

The simulation block is developed using the simulation blocks which are developed using the Simulink and SimPower System, which work together with the MATLAB. The three-phase system is shown in Fig. 3. The power source and load line impedance is $9.425\times10^{-5}+j1\times10^{-6}\Omega$. Each load has single-phase full-wave bridge rectifier circuit connection. The load active power is fixed at $P_{3\Phi}=10000\text{W}$. The calculation results are given in Table 9 to Table12. The chip utilization conditions are shown in Table 13-15. The simulation parameters are as follows:

Single-phase full-wave bridge rectifier:

Load side filters capacitor: $C_O=470\mu\text{F}$

Capacitor initial value: $V_{C0}=157\text{V}$

Source side filters inductance: $L_S=5\text{mH}$

Load side branch inductance: $L_O=1\mu\text{H}$

The three-phase main circuit parameters:

Input source: $V_P=220\text{V}$

Source side branch resistor: $R_m=94.25\mu\Omega$

Frequency: $f=60\text{Hz}$

Source side branch inductance: $L_m=1\mu\text{H}$

Load conditions:

(a) Three-phase Four-wire Balance Load

Three-phase resistor load: R_r=5.37155ohm

$P_{3\Phi}=10000\text{W}$

$\bar{S}_{eN}$=53.8384 (%)

$\bar{S}_{1U}$=0.0782 (%)

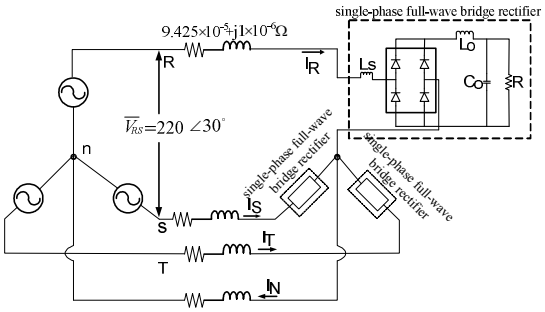

Figure 3. Three-Phase Four-Wire Simulation Model

Table 9. Three-Phase Four-Wire Balance Load Calculation Result

	PF_c	PF_A	P(W)	S_c(VA)
MATLAB	0.8229	0.9010	10000.1	12152.2
FPGA	0.8233	0.9014	9997.39	12143.5
Error(%)	-0.044%	-0.039%	0.027%	0.071%

Table 10. Fundamental of Three-Phase Four-Wire Balance Load Calculation Result

	S_A(VA)	PF_{A1}	S(VA)	S_{A1}(VA)
MATLAB	11099	0.9346	10000.1	10700.0
FPGA	11091	0.9347	9978.2	10674.9
Error(%)	0.066%	-0.015%	0.219%	0.234%

Table 11. Three-Phase Four-Wire Unbalance Load Calculation Result

	PF_c	PF_A	P(W)	S_c(VA)
MATLAB	0.7923	0.8961	10000.9	12623.2
FPGA	0.7928	0.8965	9997.4	12611.0
Error(%)	-0.061%	-0.048%	0.035%	0.096%

Table 12. Fundamental of Three-Phase Four-Wire Unbalance Load Calculation Result

	S_A(VA)	PF_{A1}	S(VA)	S_{A1}(VA)
MATLAB	11099	0.9346	10000	10700
FPGA	11091	0.9347	9978	10675
Error(%)	0.066%	-0.015%	0.219%	0.234%

Table 13. FPGA Utilization Conditions in Calculating Effective Power Factor

Logic Utilization	Used	Available	Utilization
Slice Flip Flops	3646	26624	13%
LUTs	3640	26624	13%
Slices	2771	13312	20%
IOBs	232	487	47%
MULT18×18	19	32	59%
Clk	1	8	12%
Global Timmig Constraints	Period	13.421(ns)	
	Offset in	4.899(ns)	
	Offset out	8.896(ns)	

Table 14. FPGA Utilization Conditions in Calculating Arithmetic Power Factor

Logic Utilization	Used	Available	Utilization
Slice Flip Flops	2880	26624	10%
LUTs	2763	26624	10%
Slices	2143	13312	16%
IOBs	203	487	41%
MULT18×18	15	32	46%
Clk	1	8	12%
Global Timmig Constraints	Period	9.873(ns)	
	Offset in	4.899(ns)	
	Offset out	7.241(ns)	

Table 15. FPGA Utilization Conditions in Calculating Fundamental Power Factor

Logic Utilization	Used	Available	Utilization
Slice Registers	24902	26624	93%
LUTs	19371	26624	72%
Slices	13001	13312	97%
IOBs	203	487	41%
MULT18×18	18	32	56%
Clk	1	8	12%
Global Timmig Constraints	Period	12.330(ns)	
	Offset in	10.236(ns)	
	Offset out	8.593(ns)	

I_R=29.1274(A)
I_S=29.128(A)
I_T=29.1276(A)
I_N=22.4988(A)

(b) Three-phase Four-wire Unbalance Load

Three-phase resistor load:
R_r=4.25ohm
R_s=4.25ohm
R_t=8.86ohm
$P_{3\Phi}=10000$W
$\overline{S}_{eN}$=47.003(%)
$\overline{S}_{1U}$=34.901 (%)
I_R=33.4569(A)
I_S=33.4586(A)
I_T=20.9592(A)
I_N=24.7877(A)

7 Conclusion

This study has built a FPGA-based calculation IC for obtaining power factor considering several definitions. Adopting VHDL provides sufficient flexibility and speed to construct the designed circuit by altering some IP cores. The major benefit of the proposed approach is that it executes all logic continuously and simultaneously. The designed FPGA-based system has advantages including concurrent operation, small hardware requirement, easy and fast circuit modification.

In this paper, a lot of algorithms are written into IP. The power quantities and power factors are calculated using the FPGA-based approach. The calculation errors can be greatly reduced. For the three-phase system, the calculation method for the arithmetic power factor is the fastest. And the calculation method for the effective power factor is the second.

It can also be found in the study results that $PF_e < PF_A < PF_V = PF_1 = PF_{1m1} = PF_{1m2}$. The smallest one is also PF_e. The more the unbalanced degree is, the more PF_e is less than others. Since P_1 and Q_1 are kept constant and the later is always positive, PF_1, PF_{1m1}, and PF_{1m2} are also the same. It is noted that PF_V cannot reveal the unbalanced condition. By the way, PF_A is the second choice to reveal load imbalance. The S_e has the largest integral value because it completely contains the harmonic distortion degree of load powers and the degree of load imbalance.

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