Multiplierless, Reconfigurable Folded Architecture for VLSI Wavelet Filter

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Abstract: - In this paper, the high-efficient and reconfigurable architectures for the 9/7-5/3 discrete wavelet transform (DWT) based on convolution scheme are proposed. The proposed parallel and pipelined architectures consist of a high-pass filter (HF) and a low-pass filter (LF). The critical paths of the proposed architectures are reduced. Filter coefficients of the biorthogonal 9/7-5/3 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware. In the proposed architectures, all multiplications are performed using less shifts and additions. The proposed reconfigurable architecture is 100% hardware utilization and ultra low-power. The proposed reconfigurable architectures have regular structure, simple control flow, high throughput and high scalability. Thus, they are very suitable for new-generation image compression systems, such as JPEG-2000.

Key-Words: - Folded reconfigurable architecture, 9/7-5/3 discrete wavelet transform (DWT), high-pass filter (HF), low-pass filter (LF), convolution scheme.

1 Introduction

In the field of digital image processing, the JPEG-2000 standard uses the scalar wavelet transform for image compression [1]; hence, the two-dimensional (2-D) discrete wavelet transform (DWT) and IDWT has recently been used as a powerful tool for image coding/decoding systems. Two-dimensional DWT/IDWT demands massive computations, hence, it requires a parallel and pipelined architecture to perform real-time or on-line video and image coding and decoding, and to implement high-efficiency application-specific integrated circuits (ASIC) or field programmable gate array (FPGA). At the kernel of the compression stage of the system is the DWT.

Daubechies proposed using the JPEG2000 standard biorthogonal 9/7 wavelet based on convolution scheme for lossy compression [2]. The

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symmetry of the biorthogonal 9/7 filters and the fact that they are almost orthogonal [2] make them good candidates for image compression application. Le Gall proposed using the JPEG2000 standard biorthogonal 5/3 wavelet based on convolution scheme for lossless compression [2]. The goal of the proposed architectures is to embed the 5/3 DWT computation into the 9/7 DWT computation. The coefficients of the filter are quantized before hardware implementation; hence, the multiplier can be replaced by limited quantity of shift registers and adders. Thus, the system hardware is saved, and the system throughput is improved significantly.

In this paper, we proposed a high-efficient architecture for the even and odd parts of 1-D DWT based on lifting scheme. The advantages of the proposed architectures are 100% hardware-utilization, multiplier-less, regular structure, simple control flow and high scalability.

The remainder of the paper is organized as follows. Section 2 presents the 2-D discrete wavelet

transform algorithm, and derives new mathematical formulas. In Section 3, the high-efficient and reconfigurable architecture for the 2-D DWT are proposed. Finally, comparison of performance between the proposed reconfigurable architecture and previous works is made with conclusions given in section 4.

2 The 2-D DWT Algorithm

The 2-D DWT is a multilevel decomposition technique. The mathematical formulas of 2-D DWT are defined as follows [3]-[4]:

$$LL^j(m,n) = \sum_{i=0}^{K-1}\sum_{k=0}^{K-1} l(i) \cdot l(k) \cdot LL^{j-1}(2m-i, 2n-k) \quad (1)$$

$$LH^j(m,n) = \sum_{i=0}^{K-1}\sum_{k=0}^{K-1} l(i) \cdot h(k) \cdot LL^{j-1}(2m-i, 2n-k) \quad (2)$$

$$HL^j(m,n) = \sum_{i=0}^{K-1}\sum_{k=0}^{K-1} h(i) \cdot l(i) \cdot LL^{j-1}(2m-i, 2n-k) \quad (3)$$

$$HH^j(m,n) = \sum_{i=0}^{K-1}\sum_{k=0}^{K-1} h(i) \cdot h(k) \cdot LL^{j-1}(2m-i, 2n-k) \quad (4)$$

where $0 \le n, m < N_j$, $LL^0(m,n)$ is the input image, K denotes the length of filter, $l(i)$ denote the impulse responses of the low-pass filter, and $h(k)$ denote the impulse responses of the high-pass filter, which is developed from $(K \times K)$-tap filters, and $LL^j(m,n)$, $LH^j(m,n)$, $HL^j(m,n)$, and $HH^j(m,n)$ denote respectively the coefficients of low-low, low-high, high-low and high-high subbands produced at the decomposition level j (also represented by LL^j, LH^j, HL^j, and HH^j). $N_j \times N_j$ denotes samples of LL^j.

According to the mathematical formulas (1), (2), (3) and (4), the decomposition is produced by four 2-D convolutions followed by the decimation both in the row and in the column dimension for each level. In the three-level analysis for 2-D DWT, the data set LL^{j-1} having $N_{j-1} \times N_{j-1}$ samples is decomposed into four subbands LL^j, LH^j, HL^j, and HH^j each having $N_j \times N_j$ (equals to $(N_{j-1}/2) \times (N_{j-1}/2)$) samples.

Let $LL_m^j(2n)$, $l(i)l(2k)$, $l(i)h(2k)$, $h(i)l(2k)$ and $h(i)h(2k)$ be 1-D DWT consisting of the even-numbered samples, and $0 \le n \le N_j$; $0 \le k \le K/2$ .Moreover, let $LL_m^j(2n+1)$,

$l(i)l(2k+1)$, $l(i)h(2k+1)$, $h(i)l(2k+1)$ and $h(i)h(2k+1)$ be 1-D DWT consisting of the odd-numbered samples, and $0 \le n \le N_j$; $0 \le k \le K/2$. $LL_{m,i}^j(n)$, $LH_{m,i}^j(n)$, $HL_{m,i}^j(n)$, and $HH_{m,i}^j(n)$ can be expressed as follows:

$$LL_{m,i}^j(n) = \sum_{k=0}^{\lceil K/2 \rceil -1} l(i)l(2k) \cdot LL_{2m-i}^{j-1}(2n-2k)$$
$$+ \sum_{k=0}^{K-\lceil K/2 \rceil -1} l(i)l(2k+1) \cdot LL_{2m-i}^{j-1}(2n-2k-1) \quad (5)$$

$$LH_{m,i}^j(n) = \sum_{k=0}^{\lceil K/2 \rceil -1} l(i)h(2k) \cdot LL_{2m-i}^{j-1}(2n-2k)$$
$$+ \sum_{k=0}^{K-\lceil K/2 \rceil -1} l(i)h(2k+1) \cdot LL_{2m-i}^{j-1}(2n-2k-1) \quad (6)$$

$$HL_{m,i}^j(n) = \sum_{k=0}^{\lceil K/2 \rceil -1} h(i)l(2k) \cdot LL_{2m-i}^{j-1}(2n-2k)$$
$$+ \sum_{k=0}^{K-\lceil K/2 \rceil -1} h(i)l(2k+1) \cdot LL_{2m-i}^{j-1}(2n-2k-1) \quad (7)$$

$$HH_{m,i}^j(n) = \sum_{k=0}^{\lceil K/2 \rceil -1} h(i)h(2k) \cdot LL_{2m-i}^{j-1}(2n-2k)$$
$$+ \sum_{k=0}^{K-\lceil K/2 \rceil -1} h(i)h(2k+1) \cdot LL_{2m-i}^{j-1}(2n-2k-1) \quad (8)$$

The above equations imply that $LL_{m,i}^j(n)$, $LH_{m,i}^j(n)$, $HL_{m,i}^j(n)$ and $HH_{m,i}^j(n)$ can be computed as the sum of two 1-D convolutions performed independently on the even part $LL_{2m-i}^{j-1}(2n-2k)$ and the odd part $LL_{2m-i}^{j-1}(2n-2k-1)$.

2.1 The 2-D DWT Algorithm

The proposed architecture performs parallel and pipelined processing. Each analysis level involves two stages: stage 1 performs row filtering, and stage 2 performs column filtering. After stage 1, the input image of size is decomposed into two subbands (L and H) of size. And stage 1 performs result is stored in the memory. The L subbund inputted first of stage 2 performs. Second is H subbund.In a one-level filter bank for 2-D DWT computation. At the first level, the size of the input image is $N \times N$, and the size of the output of each of the three subbands LH, HL and HH is $(N/2) \times (N/2)$. At the second level, the input is the LL subband whose size is $(N/2) \times (N/2)$, and the size of the output of each of the three subbands

LLLH, *LLHL* and *LLHH* is $(N/4) \times (N/4)$. At the third level, the input is the *LLLL* subband whose size is $(N/4) \times (N/4)$, and the size of the output of each of the four subbands *LLLLLL*, *LLLLLH*, *LLLLHL* and *LLLLHH* is $(N/8) \times (N/8)$, and so on. Figure 1 shows 1-level 2-D DWT.

The coefficients of the low-pass filter and the high-pass filter have been derived in the biorthogonal 9/7 and 5/3 wavelet [2]. The 9/7 wavelet coefficients are quantized before hardware implementation. We assume that the low-pass filter has nine tapes: $h_{9/7}(0)$, $\pm h_{9/7}(1)$, $\pm h_{9/7}(2)$, $\pm h_{9/7}(3)$ and $\pm h_{9/7}(4)$, and the high-pass filter has seven tapes: $g_{9/7}(0)$, $\pm g_{9/7}(1)$, $\pm g_{9/7}(2)$ and $\pm g_{9/7}(3)$. The 5/3 wavelet coefficients are quantized before hardware implementation. We assume that the low-pass filter has five tapes: $h_{5/3}(0)$, $\pm h_{5/3}(1)$ and $\pm h_{5/3}(2)$, and the high-pass filter has three tapes: $g_{5/3}(0), \pm g_{5/3}(0)$.

3 The High-Efficient and Reconfigurable Architectures for 5/3 and 9/7 2-D DWT

The proposed reconfigurable architecture for 5/3 and 9/7 convolution based 2-D DWT including hing-pass filter (HF) and low-pass filter (LF) is shown in Figure 2[5][6]. In this reconfigurable architecture, the input architecture are show in Figure 3,4,5 and 6,the multiplexers architecture are show in Figure 7,the architecture of hing-pass filter (HF) and the architecture of low-pass filter (LF)are shown in Figure 8 and 9, respectively. The proposed reconfigurable architecture for hing-pass filter (HF) consists of one delay units, twenty-eight multiplexers, six adders (It doesn't include carrry save adder (CSA)) and four 9/7 wavelet coefficients processing elements (PEs).The proposed reconfigurable architecture for low-pass filter (LF) consists of $5 + 5N$ delay units, seventy-eight multiplexers, seven adders (It doesn't include carrry save adder (CSA)), five 9/7 wavelet coefficients and one 5/3 wavelet coefficients processing elements (PEs).Filter coefficients of the biorthogonal 9/7 and 5/3 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware [9-10]. In the proposed architecture, all multiplications are performed using shifts and additions after approximating the coefficients as a Booth binary recoded format (BBRF). The constant multiplier shown in Figure 10 consists of two carry-save-adders (CSA(4,2)), a Carry Lookahead Adder (CLA) , and six hardwire shifters and replaces conventional

multiplier ($\otimes$) in processing elements (PEs). Figure 11 shows architectures of line delay (LD) for Vertical filter in 2-D DWT [7].

The proposed reconfigurable architectures for 9/7 and 5/3 DWT reduce the critical path [5][6]. In $N \times N$ 2-D DWT, it requires

$$2J + \frac{19}{2}N(1 - \frac{1}{2^J}) + \frac{4}{3}N^2(1 - \frac{1}{4^J})$$ computation

cycles (addition operations) with $N^2 + (25/2)N + 14$ memories to perform 5/3 and 9/7 2-D DWT, where J is number of levels [11-12]. Both of two architectures are 100% hardware utilization.

4 Conclusion

Filter coefficients are quantized before implementation using the biorthogonal 9/7 and 5/3 wavelet. The hardware is cost-effective and the system is high-speed. The proposed architecture in 9/7 DWT reduces power dissipation by m compared with conventional architectures in m-bit operand (low-power utilization).

Three standard images have been used for the test: "Lenna" 256×256 (*I*=1), "Barbara" 512×512 (*I*=2)and "Boat" 512×512 (*I*=3). The number of wavelet decomposition levels (L) has been varied from 1 to 3 for 256×256 images and from 1 to 4 for 512×512 image. Table 1 shows the peak-signal-to-noise ratios (PSNRs) comparison among different 9/7 wavelet implementations for multiple images(I) and decomposition levels(L). *A*-Open-jpeg, *B*-Low-complexity, *C*-This work[5][6]. The proposed architecture in 9/7 and 5/3 DWT with 20-bit fixed point operations had been applied to 512×512 original images Lena is shown in Figures 12(a) and 13(a)and the reconstructed images Lena is shown in Figure 12(b) and 13(b), respectively. The PSNRs of the reconstructed images Lena are 55.701dB and 42.625dB, respectively. Hence, the proposed reconfigurable architecture has been applied to image compression with great satisfaction. In this paper, the high-efficient and low-power reconfigurable architecture for 2-D DWT has been proposed [9-11]. The proposed reconfigurable architecture performs compression in

$$(2J + \frac{19}{2}N(1 - \frac{1}{2^J}) + \frac{4}{3}N^2(1 - \frac{1}{4^J}))T_a$$ computation

time for 9/7 DWT and 5/3 DWT, respectively. where the time unit (Ta is time of addition operation). The critical paths are $2T_a$ for 9/7 and 5/3 DWT, and the output latency time are $49T_a$ for 9/7 and 5/3 DWT. Buffer sizes are $N^2 + (25/2)N + 14$ for 9/7 and 5/3 DWT, respectively. The control complexity is very

simple. The comparisons between previous works [6] [8] and this work are shown in Table 2 for 9/7 DWT. The advantages of the proposed reconfigurable architecture are 100% hardware utilization and ultra low-power. The architecture has regular structure, simple control flow, high throughput and high scalability. Thus, it is very suitable for new-generation image compression systems, such as JPEG-2000. The proposed reconfigurable DWT is a reusable IP, which can be implemented in various processes and combined with an efficient use of hardware resources for the trade-offs of performance, area, and power consumption.

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Table 1 Performance comparison among different 9/7 wavelet implementations for multiple images(I) and decomposition levels(L).

I	L	A[dB]	B[dB]	C[dB]
1	1	49.41	49.35	65.27
	2	49.16	48.79	59.27
	3	49.26	48.48	55.77
2	1	49.57	49.48	66.01
	2	49.25	49.07	60.01
	3	49.21	48.80	56.50
	4	49.21	48.53	56.50
3	1	49.42	49.45	64.42
	2	49.11	48.92	58.41
	3	49.06	48.72	54.90
	4	49.06	48.58	54.90

Table 2 Comparison between previous works and this work (9/7 DWT architecture with two input, T_a :addition time and K : filter length)

Architecture	Performance
Wu [8] 2005 (Dual-input)	Multiplier : $4K$
	adder : $4K$
	Memory Size: $N^2/4 + KN + K$
	Computation Cycle: $\approx (2N^2/3) \cdot T_m$
	Reconfigurable architecture: NO
Martina [6] 2007 (Single-input)	adder : 19
	Memory Size: --
	Computation Cycle: $(16N(1-2^{-J}) + 2N^2(1-2^{-2J})) \cdot T_m$
	Reconfigurable architecture: YES
This work [Sung, Hsin, Chang, 20101] (Single-input)	adder : 33
	Memory Size: $N^2 + (25/2)N + 14$
	Computation Cycle: $(2J + (19/2)N(1-2^{-J}) + (4/3)N^2(1-2^{-2J})) \cdot T_a$
	Reconfigurable architecture: YES
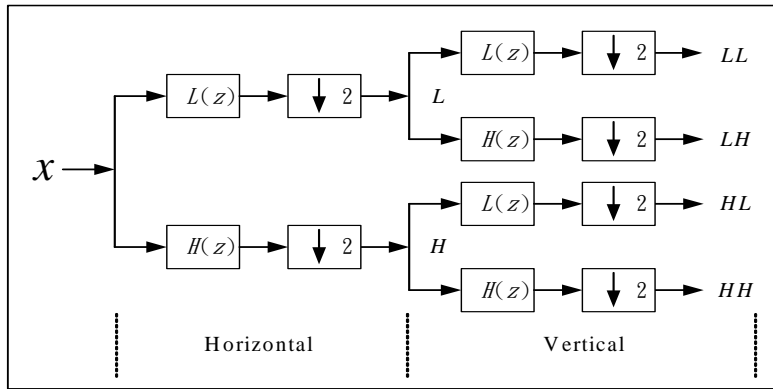
Fig. 1. 1-level 2-D DWT
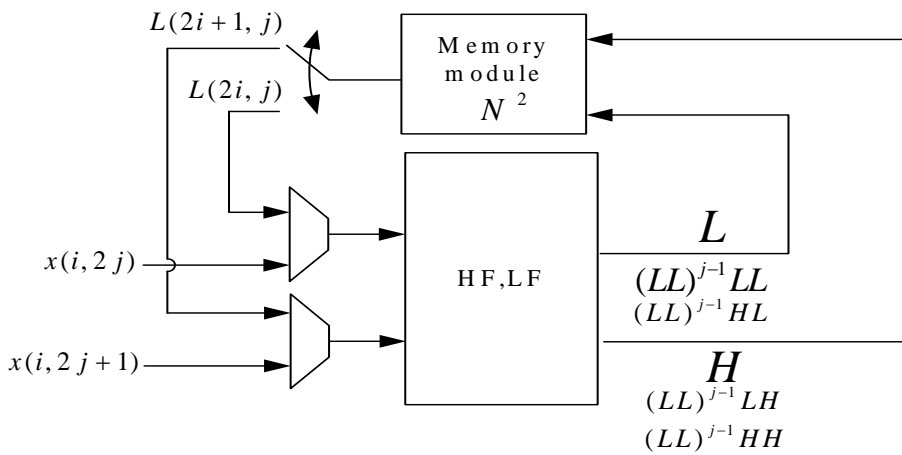
Fig. 2. The proposed reconfigurable architecture for 9/7 and 5/3 2-D DWT based on convolution scheme
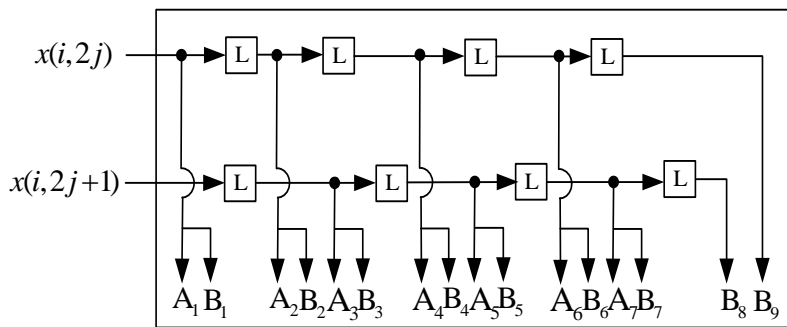

Fig. 3. The inputs architecture of horizontal filter
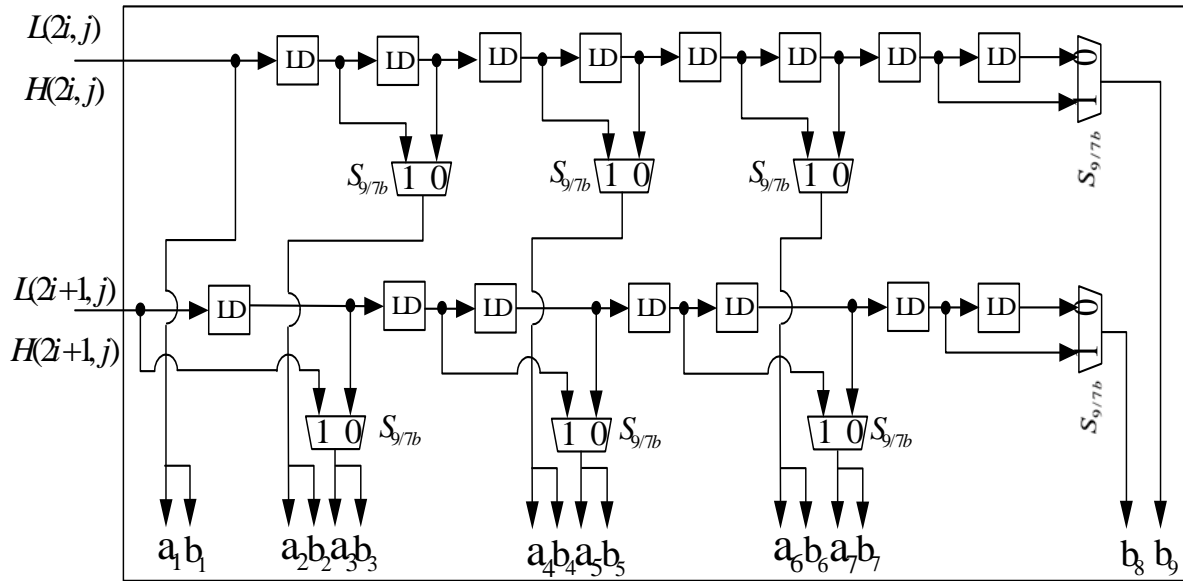
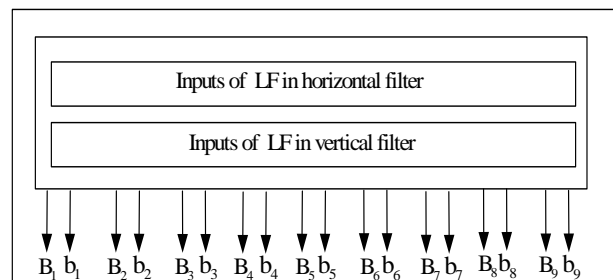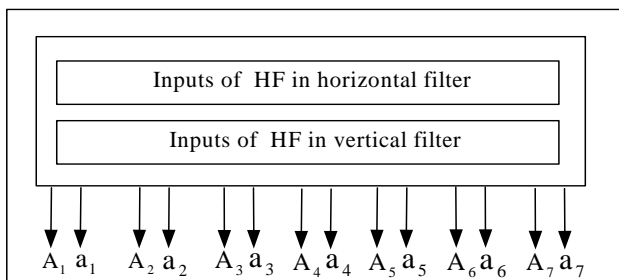Fig. 4. The inputs architecture of vertical filter

Fig. 5. The inputs architecture of high-pass filter (HF)

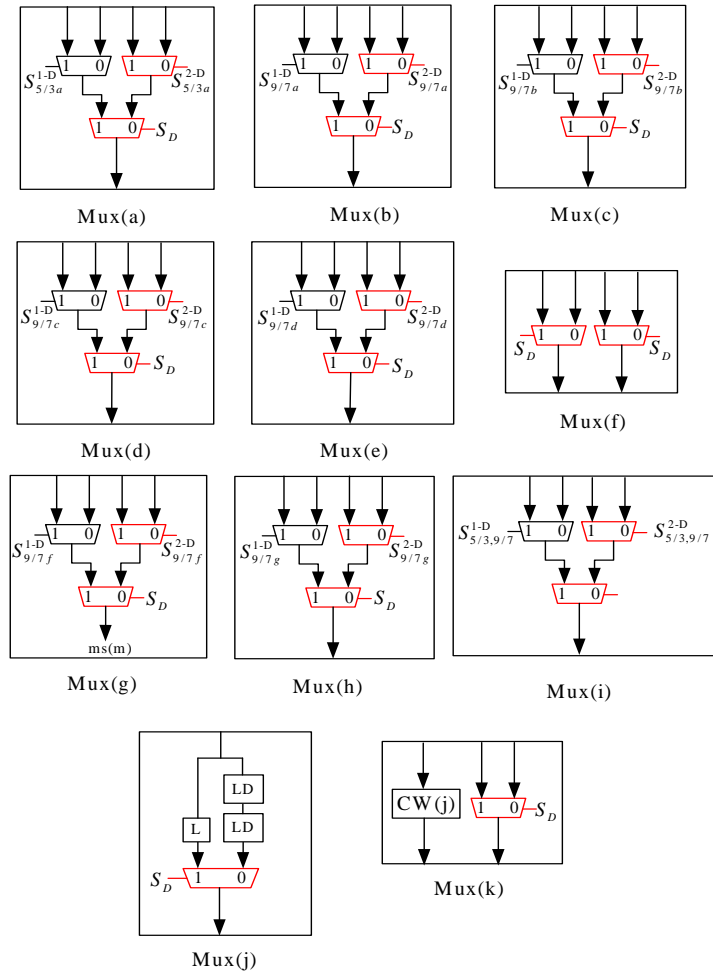Fig. 6. The inputs architecture of low-pass filter (LF)

Fig. 7. The architecture of multiplexers (Mux) (a)~(f) for 1-D or 2-D DWT.
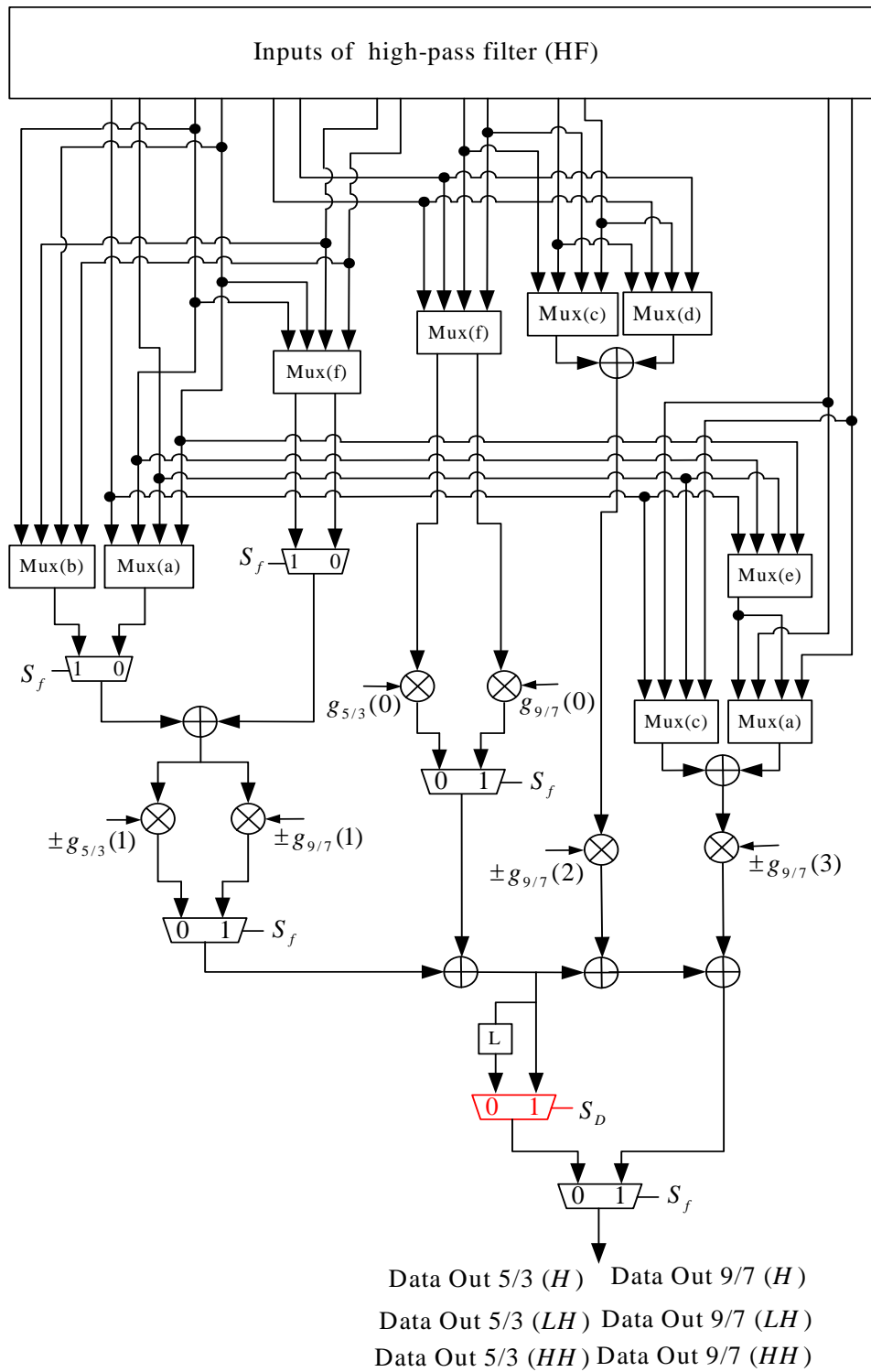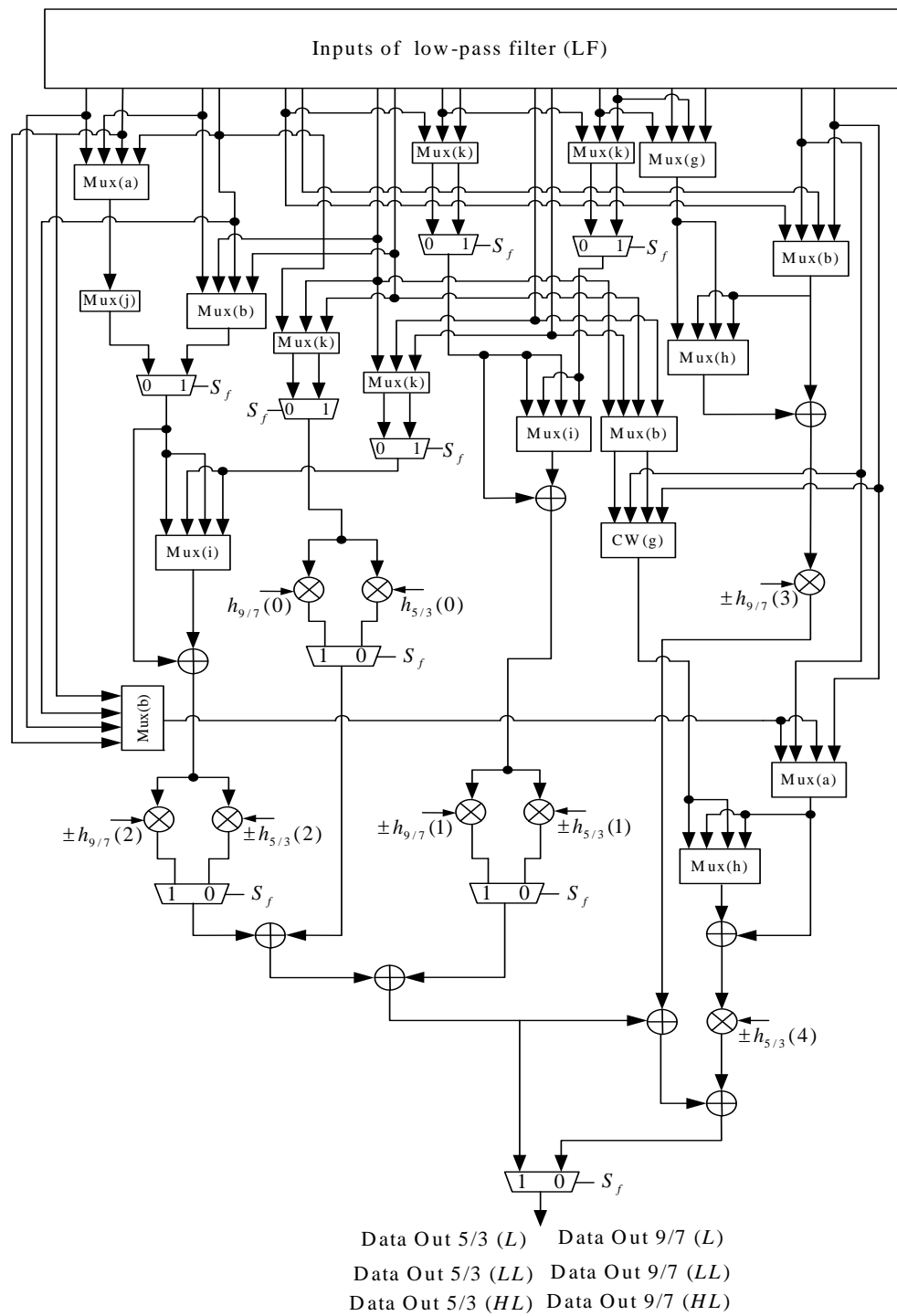
Fig. 8. The architecture of high-pass filter (HF)

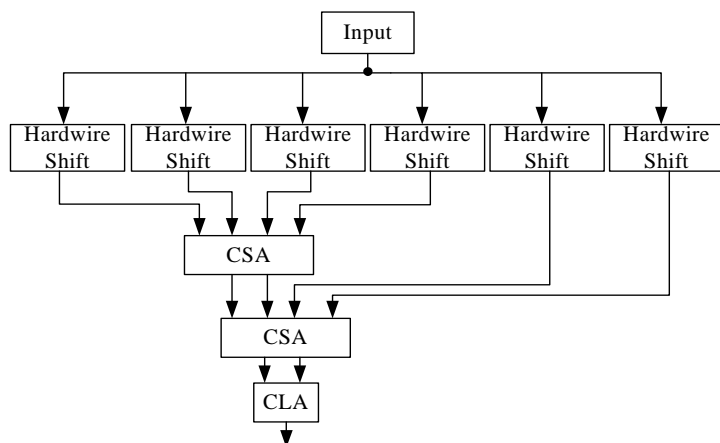Fig. 9. The inputs architecture of low-pass filter (LF)

Fig. 10 The constant multiplier replaces conventional multiplier $(\otimes)$ in processing elements (PEs)
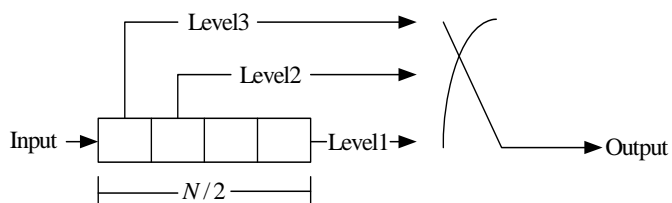

Fig. 11. Line delay(LD) for Vertical filter in 2-D DWT
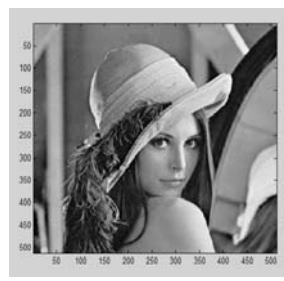

(a)   (b)

Fig. 12 512×512 Lena (a) Original image (b) Reconstructed image (9/7 DWT with 4-level)

(a)   (b)

Fig. 13 512×512 Lena (a) Original image (b) Reconstructed image (5/3 DWT with 4-level)