Reconfigurable Architecture for VLSI 9/7-5/3 Wavelet Filter

Tze-Yun Sung [*] Hsi-Chin Hsin [**]
[*]Department of Microelectronics Engineering
Chung Hua University
707, Sec. 2, Wufu Road, Hsinchu City 300-12
TAIWAN
bobsung@chu.edu.tw
[**]Department of Computer Science and Information Engineering
National United University
1, Lien-Da, Miao-Li, 360-03
TAIWAN
hsin@nuu.edu.tw

Abstract: - In this paper, the high-efficient and reconfigurable lined-based architectures for the 9/7-5/3 discrete wavelet transform (DWT) based on lifting scheme are proposed. The proposed parallel and pipelined architectures consist of a horizontal filter (HF) and a vertical filter (VF). The critical paths of the proposed architectures are reduced. Filter coefficients of the biorthogonal 9/7-5/3 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware In the proposed architectures, all multiplications are performed using less shifts and additions. The proposed reconfigurable architecture is 100% hardware utilization and ultra low-power. The proposed reconfigurable architectures have regular structure, simple control flow, high throughput and high scalability. Thus, they are very suitable for new-generation image compression systems, such as JPEG-2000.

Key-Words: - Reconfigurable architecture, 9/7-5/3 discrete wavelet transform (DWT), horizontal filter (HF), vertical filter (VF), lifting scheme.

1 Introduction

In the field of digital image processing, the JPEG-2000 standard uses the scalar wavelet transform for image compression [1]; hence, the two-dimensional (2-D) discrete wavelet transform (DWT) and IDWT has recently been used as a powerful tool for image coding/decoding systems. Two-dimensional DWT/IDWT demands massive computations, hence, it requires a parallel and pipelined architecture to perform real-time or on-line video and image coding and decoding, and to implement high-efficiency application-specific integrated circuits (ASIC) or field programmable gate array (FPGA). At the kernel of the compression stage of the system is the DWT.

Swelden proposed using the biorthogonal 9/7 wavelet based on lifting scheme for lossy compression [2]. The symmetry of the biorthogonal 9/7 filters and the fact that they are almost orthogonal [2] make them good candidates for image compression application. Gall and Tabatai proposed using the biorthogonal 5/3 wavelet based on lifting scheme for lossless compression [3]. The goal of the proposed architectures is to embed the 5/3 DWT computation into the 9/7 DWT computation. The coefficients of the filter are quantized before hardware implementation; hence, the multiplier can be replaced by limited quantity of shift registers and adders. Thus, the system hardware is saved, and the system throughput is improved significantly.

In this paper, we proposed a high-efficient architecture for the even and odd parts of 1-D DWT based on lifting scheme. The advantages of the proposed architectures are 100% hardware-utilization, multiplier-less, regular structure, simple control flow and high scalability.

The remainder of the paper is organized as follows. Section 2 presents the lifting-based 2-D discrete wavelet transform algorithm, and derives new mathematical formulas. In Section 3, the high-efficient and reconfigurable architecture for the lifting-based 2-D DWT are proposed. Finally, comparison of performance between the proposed reconfigurable architecture and previous works is made with conclusions given in section 4.

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2 The Lifting-Based 2-D DWT Algorithm

Usually the Lifting-based DWT requires less computation compared to the convolution-based approach. However, the savings depend on the length of the filters. During the lifting implementation, no-extra memory buffer is required because of the in-place computation feature of lifting. This is particularly suitable for the hardware implementation with limited available on-chip memory. Many papers proposed the algorithms and architectures of DWT [3]-[11], but they require massive computation. In 1996, Sweldens proposed a new lifting-based DWT architecture, which requires half of hardware compared to the conventional approaches [2].

2.1 The 9/7 2-D DWT Algorithm

The 9/7 discrete wavelet transform factoring into lifting scheme is represented as [12]:

$$\tilde{P}_{9/7}=\begin{bmatrix}1 & \alpha(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \beta(1+z) & 1\end{bmatrix}\begin{bmatrix}1 & \gamma(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \delta(1+z) & 1\end{bmatrix}\begin{bmatrix}\zeta & 0\\ 0 & 1/\zeta\end{bmatrix} \quad (1)$$

where α,β,γ and δ are the coefficients of lifting scheme, and ζ and $1/\zeta$ are scale normalization factors.

The architecture based on lifting scheme consists of splitting module, two lifting modules and scaling modules. The architecture of 9/7 1-D DWT based on lifting scheme is shown in Figure 1.

The 9/7 2-D DWT is a multilevel decomposition technique. According to the architecture of 9/7 1-D DWT based on lifting scheme, the architecture of modified 9/7 2-D DWT based on lifting scheme can be derived and shown in Figure 2.

2.2 The Modified 9/7 2-D DWT Algorithm

According to equation (1), the transform matrix of the 9/7 DWT based on lifting scheme is modified as

$$\tilde{P}_1(z)=\begin{bmatrix}1 & \alpha(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \beta(1+z) & 1\end{bmatrix}\begin{bmatrix}1 & \gamma(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \delta(1+z) & 1\end{bmatrix}\begin{bmatrix}\zeta & 0\\ 0 & 1/\zeta\end{bmatrix}$$

$$=\begin{bmatrix}1/\alpha & (1+z^{-1})\\ 0 & 1/\alpha\end{bmatrix}\begin{bmatrix}1/\beta & 0\\ (1+z) & 1/\beta\end{bmatrix}\begin{bmatrix}1/\gamma & (1+z^{-1})\\ 0 & 1/\gamma\end{bmatrix}\begin{bmatrix}1/\delta & 0\\ (1+z) & 1/\delta\end{bmatrix}\begin{bmatrix}\alpha\beta\gamma\delta\zeta & 0\\ 0 & \alpha\beta\gamma\delta/\zeta\end{bmatrix}$$

$$=\begin{bmatrix}1 & 1+z^{-1}\\ 0 & 1/\alpha\end{bmatrix}\begin{bmatrix}1/\alpha\beta & 0\\ 1+z & 1\end{bmatrix}\begin{bmatrix}1 & 1+z^{-1}\\ 0 & 1/\beta\gamma\end{bmatrix}\begin{bmatrix}1/\gamma\delta & 0\\ 1+z & 1\end{bmatrix}\begin{bmatrix}\alpha\beta\gamma\delta\zeta & 0\\ 0 & \alpha\beta\gamma/\zeta\end{bmatrix}$$

$$=\begin{bmatrix}1 & 1+z^{-1}\\ 0 & A\end{bmatrix}\begin{bmatrix}B & 0\\ 1+z & 1\end{bmatrix}\begin{bmatrix}1 & 1+z^{-1}\\ 0 & C\end{bmatrix}\begin{bmatrix}D & 0\\ 1+z & 1\end{bmatrix}\begin{bmatrix}K_0 & 0\\ 0 & K_1\end{bmatrix} \quad (2)$$

where $A=1/\alpha$, $B=1/\alpha\beta$, $C=1/\beta\gamma$, $D=1/\gamma\delta$, $K_0=\alpha\beta\gamma\delta\zeta$,and $K_1=\alpha\beta\gamma/\zeta$.

2.3 The 5/3 2-D DWT Algorithm

The data flow of 5/3 1-D DWT based on lifting scheme is shown in Figure 3.

The 5/3 2-D DWT is a multilevel decomposition technique; that decomposes into four subbands such as HH, HL, LH and LL. The data flow of 5/3 2-D DWT based on lifting scheme can be derived and shown in Figure 4. The 5/3 discrete wavelet transform factoring into lifting scheme is represented as [10]:

$$\tilde{P}_{5/3}=\begin{bmatrix}1 & \alpha(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \beta(1+z) & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix} \quad (3)$$

3 The High-Efficient and Reconfigurable Architectures for 9/7 and 5/3 Lifting-Based 2-D DWT

The proposed reconfigurable architecture for 5/3 and 9/7 lifting based 2-D DWT including horizontal filter (HF) and vertical filter (VF) is shown in Figure 5. In this reconfigurable architecture, the architecture of horizontal filter and the architecture of vertical filter are shown in Figure 6 and 7, respectively. The proposed reconfigurable architecture for modified horizontal filter (HF) consists of eleven delay units, seventeen multiplexers and two processing elements (PEs). The PE(A/B/E) performs O1 for data output 5/3(1) and *PE*(*C/D/F*) performs O2 for data output

9/7(1). The architecture of *PE*(*A/B/E*) and the architecture of *PE*(*C/D/F*) are shown in Figure 8 and 9, respectively. The architecture of scaling normalization (SN) is shown in Figure 10. Filter coefficients of the biorthogonal 9/7 and 5/3 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware. In the proposed architecture, all multiplications are performed using shifts and additions after approximating the coefficients as a Booth binary recoded format (BBRF). The constant multiplier shown in Figure 11 consists of two carry-save-adders (CSA(4,2)) , a Carry Lookahead Adder (CLA) , and six hardwire shifters and replaces conventional multiplier (⊗) in *PE*(*A/B/E*), *PE*(*C/D/F*) and SN. Figure 12 shows architectures of line delays LD, LD1, LD2 and LD3 in vertical filter. We handle borders by the symmetric extension method [10]. Hence, the quality of reconstructed images can be improved.

The proposed reconfigurable architectures for 9/7 and 5/3 DWT reduce the critical path [13]-[19]. In $N \times N$ 2-D DWT, it requires $9J + 10N(1-\frac{1}{2^J}) + \frac{4}{3}N^2(1-\frac{1}{4^J})$ computation cycles (addition operations) with $N^2/4 + 9N$ memories to perform 9/7 2-D DWT, where J is number of levels. It requires $4J + 2N(1-\frac{1}{2^J}) + \frac{2}{3}N^2(1-\frac{1}{4^J})$ computation cycles (addition operations) with $N^2/4 + 3.5N$ memories to perform 5/3 2-D DWT, where J is number of levels. Both of two architectures are 100% hardware utilization [20-22].

4 Conclusion

Filter coefficients are quantized before implementation using the biorthogonal 9/7 and 5/3 wavelet. The hardware is cost-effective and the system is high-speed. The proposed architecture in 9/7 DWT reduces power dissipation by m compared with conventional architectures in m-bit operand (low-power utilization).

The proposed architecture in 5/3 DWT with 24-bit fixed point operations had been applied to 512×512 original images Lena is shown in Figures 13(a) and the reconstructed images Lena is shown in Figure 13(b), respectively. The PSNRs of the reconstructed images Lena is 32.554dB. Hence, the proposed reconfigurable architecture has been applied to image compression with great satisfaction.

In this paper, the high-efficient and low-power reconfigurable architecture for 2-D DWT has been proposed. The proposed reconfigurable architecture performs compression in $(9J + 10N(1-\frac{1}{2^J}) + \frac{4}{3}N^2(1-\frac{1}{4^J})) \cdot T_a$ computation time for 9/7 DWT and $(\frac{3}{2}N(1-\frac{1}{2^J}) + \frac{2}{3}N^2(1-\frac{1}{4^J})) \cdot T_a$ for 5/3 DWT, where the time unit (Ta is time of addition operation). The critical paths are $3T_a$ for 9/7 DWT and $2T_a$ for 5/3 DWT, and the output latency time are $49T_a$ for 9/7 DWT and $11T_a$ for 5/3 DWT. Buffer sizes are $N^2/4 + 9N$ for 9/7 DWT and $N^2/4 + 3.5N$ for 5/3 DWT. The control complexity is very simple.

The comparisons between previous works [14] [18] and this work are shown in Table 1 for 9/7 DWT and Table 2 for 5/3 DWT [14] [19].

The advantages of the proposed reconfigurable architecture are 100% hardware utilization and ultra low-power. The architecture has regular structure, simple control flow, high throughput and high scalability. Thus, it is very suitable for new-generation image compression systems, such as JPEG-2000. The proposed reconfigurable DWT is a reusable IP, which can be implemented in various processes and combined with an efficient use of hardware resources for the trade-offs of performance, area, and power consumption.

References:

[1] ITU-T Recommendation T.800. JPEG2000 image coding system – Part 1, ITU Std., July 2002. http://www.itu.int/ITU-T/.

[2] W. Sweldens, "The lifting scheme: A custom-design construction of biorthogonal wavelet," *Applied and Computational Harmonic Analysis*, vol. 3, 1996, pp. 186-200.

[3] D. L. Gall, A. Tabiatai, "Sub-band coding of digital images using symmetric short kernel filters and arithmetic coding techniques," *Proc. IEEE Int. Conf. Acoust., Speech, signal Process.*, 1988, pp.761-764.

[4] G. Beylkin, R. Coifman, V. Rokhlin, "*Wavelet in numerical analysis in Wavelets and their applications*," New York: Jones and Bartlett, 1992.

[5] A. N. Akansu, R. A. Haddad, "*Multiresolution signal decomposition: Transform, subbands and Wavelets,* " New York: Academic, 1992.

[6] I. Sodagar, H.-J. Lee, P. Hatrack, Y.-Q. Zhang, "Scalable wavelet coding for synthetic/natural hybrid images," *IEEE Trans. Circuits and*

Systems for Video Technology, Vol. 9, Mar. 1999, pp. 244-254.

[7] D. Taubman, "High performance scalable image compression with EBCOT," *IEEE Trans. Image Processing*, Vol. 9, 2000. pp. 1158-1170.

[8] R. Kronland-Martinet, J. Morlet, A. Grossman, "Analysis of sound patterns through wavelet transform," *Int. J. Pattern Recognit. Artif. Intell*., Vol. 1, No. 2, 1987, pp. 273-302.

[9] M. A. Stoksik, R. G. Lane, D. T. Nguyen, "Accurate synthesis of fractional Brownian motion using wavelets," *Electronic Letters*, Vol. 30, No. 5, Mar. 1994, pp. 384-284.

[10] T. Y. Sung, "Memory-efficient and high-performance parallel-pipelined architectures for 5/3 forward and inverse discrete Wavelet transform," *WSEAS Transactions on Electronics*, Volume 4, No.2, February 2007, pp.32-41.

[11] K. C. B. Tan, T. Arslan, "An embedded extension algorithm for the lifting based discrete wavelet transform in JPEG 2000," *IEEE International conference on acoustic, speech, and signal processing*, Vol.4, 2002, pp.3513-3516.

[12] K. Parhi, T. Nishitani, "VLSI architectures for discrete wavelet transforms," *IEEE Trans. VLSI Systems*, Vol. 1, No. 2, 1993, pp. 191-202.

[13] I. Daubechies, W. Sweldens., "Factoring wavelet transforms into lifting schemes," *J.Fourier Anal. Appl*., Vol.4, 1998, pp. 247-269.

[14] K. Andra, C. Chakrabarti, T. Acharya, "A VLSI architecture for lifting-based forward and inverse wavelet transform," *IEEE Trans. on Signal Processing*, Vol. 50, 2002, pp.966-977.

[15] C. Xiong, S. Zheng, J. Tian, J. Liu, "The improved lifting scheme and novel reconfigurable VLSI architecture for the 5/3 and 9/7 wavelet filters," *2004 IEEE International Conference on Communications, Circuits and Systems*, Vol. 2, 2004, pp. 728-732.

[16] T.-Y. Sung, Y.-S. Shieh, "A high-speed / ultra low-power architecture for 2-D discrete Wavelet transform," *2005 IEEE International Conference on Systems and Signals (ICSS-2005)*, Kaohsiung, Taiwan, April 28-29, 2005, pp. 326-331.

[17] T.-Y. Sung, C.-W. Yu, Y.-S. Shieh, H.-C. Hsin, "A high-efficient line-based architecture for 2-D lifting-based DWT using 9/7 Wavelet filters," *9th Joint Conference on Information Sciences (JCIS-2006)*, Kaohsiung, Taiwan, Oct. 8-11, 2006, pp.626-629.

[18] B.-F. Wu, C.-F. Lin, "A high-performance and memory-efficient pipeline architecture for the 5/3 and 9/7 discrete Wavelet transform of JPEG-2000 Codec," *IEEE Trans. Circuits and Systems for Video Technology*, Vol. 15, No. 12, Dec. 2005, pp. 1615-1628.

[19] J. S. Chiang, and C. H. Hsia, "An efficient VLSI architecture for 2-D DWT using lifting scheme," *IEEE International Conference on Systems and signals*, April, 2005, pp.528-531.

[20] T.-Y. Sung, "Low-power and high-performance 2-D DWT and IDWT architectures based on 4-tap Daubechies filters", *7th WSEAS International Conference on Multimedia Systems & Signal Processing*, 2007, pp.50-55.

[21] M. A. Farahani, M. Eshghi, "Implementing a new architecture of wavelet packet transform on FPGA", *8th WSEAS international conference on Acoustics & music: theory & applications*, 2007, pp.37-41.

[22] T.-Y. Sung, "Reconfigurable VLSI architecture for FFT processor", *WSEAS Transactions on Circuits and Systems*, Vol. 8, No. 6, 2009, pp.465-474.

Table 1 Comparison between previous works and this work (9/7 DWT architecture with single input, T_m: multiplication time, T_a:addition time and T_d: latency delay)

Architecture	Performance
Wu [18] 2005	Memory Size(bytes): $N^2/4+5.5N$
	Computation Cycle: $(22J+6N(1-\frac{1}{2^J})+\frac{4}{3}N^2(1-\frac{1}{4^J}))\cdot T_m$
	Border Handling: NO
	Hardware Utilization: $\approx 100\%$
Andra [14] 2002	Memory Size(bytes): N^2
	Computation Cycle: $T_d \cdot J+\frac{4}{3}N^2(1-\frac{1}{4^J})\cdot T_m$
	Border Handling: NO
	Hardware Utilization: $\approx 50\%$
This work [Sung, Hsin, 2010]	Memory Size(bytes): $N^2/4+9N$
	Computation Cycle: $(9J+10N(1-\frac{1}{2^J})+\frac{4}{3}N^2(1-\frac{1}{4^J}))\cdot T_a$
	Border Handling: YES
	Hardware Utilization: $\approx 100\%$

Table 2 Comparison between previous works and this work (5/3 DWT architecture with dual input, T_m: multiplication time and T_a:addition time)

Architecture	Performance
Chiang [19] 2005	Memory Size(bytes): $N^2/4+5N$
	Computation Cycle: $N^2 \cdot T_m$
	Border Handling: NO
	Hardware Utilization: $\approx 100\%$
Andra [14] 2002	Memory Size(bytes): $N^2/2+4N$
	Computation Cycle: $(\frac{N^2}{2}+2N)\cdot T_m$
	Border Handling: NO
	Hardware Utilization: $\approx 100\%$
This work [Sung, Hsin, 2010]	Memory Size(bytes): $N^2/4+3.5N$
	Computation Cycle: $(\frac{3}{2}N(1-\frac{1}{2^J})+\frac{2}{3}N^2(1-\frac{1}{4^J}))\cdot T_a$
	Border Handling: YES
	Hardware Utilization: $\approx 100\%$

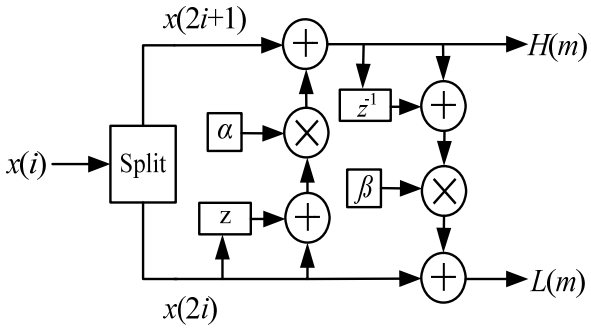


Fig. 1. The architecture of 9/7 1-D DWT based on lifting scheme($P1=\alpha(1+z)$, $U1=\beta(1+z^{-1})$, $P2=\gamma(1+z)$ and $U2=\delta(1+z^{-1})$)

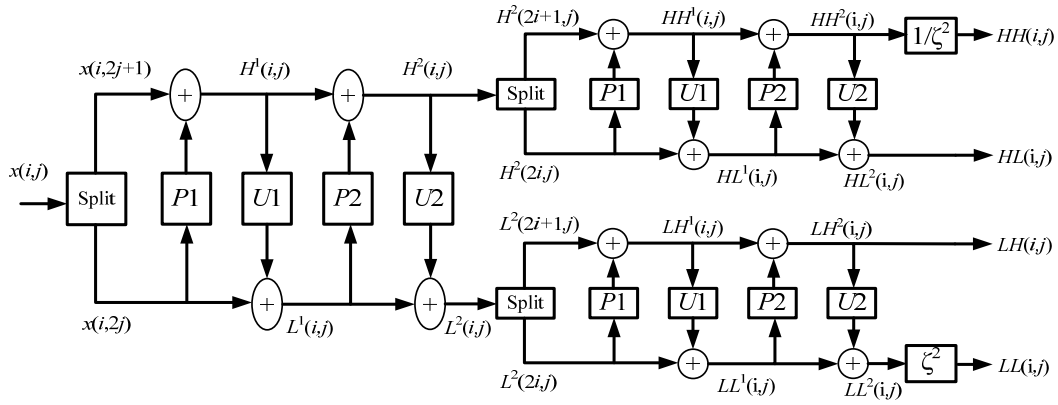


Fig. 2. The architecture of modified 9/7 2-D DWT based on lifting scheme

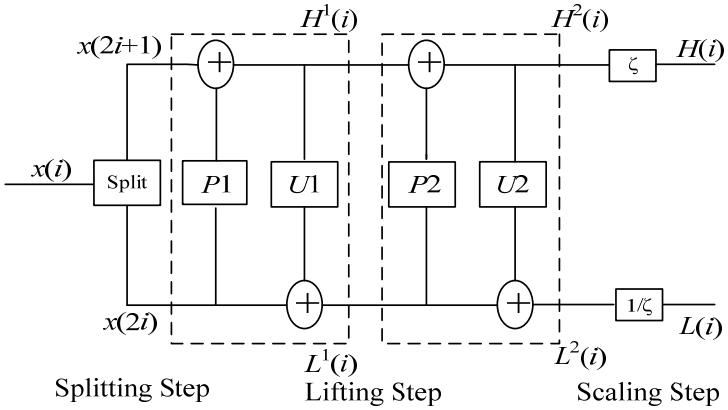


Fig. 3. The data flow of 5/3 1-D DWT based on lifting scheme

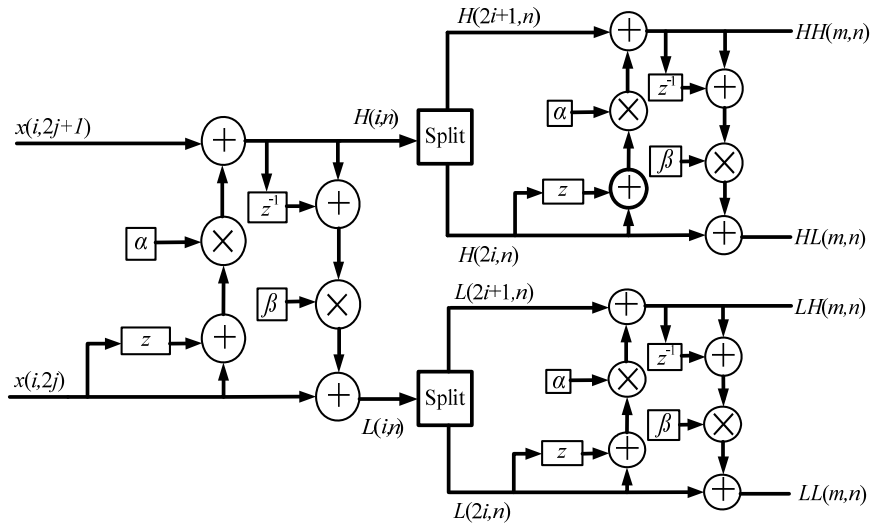


Fig. 4. The data flow of 5/3 2-D DWT based on lifting scheme

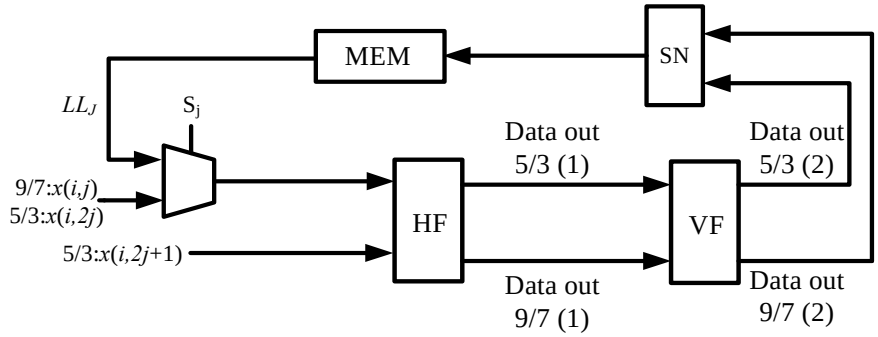


Fig. 5. The proposed reconfigurable architecture for 5/3 and 9/7 2-D DWT based on lifting scheme

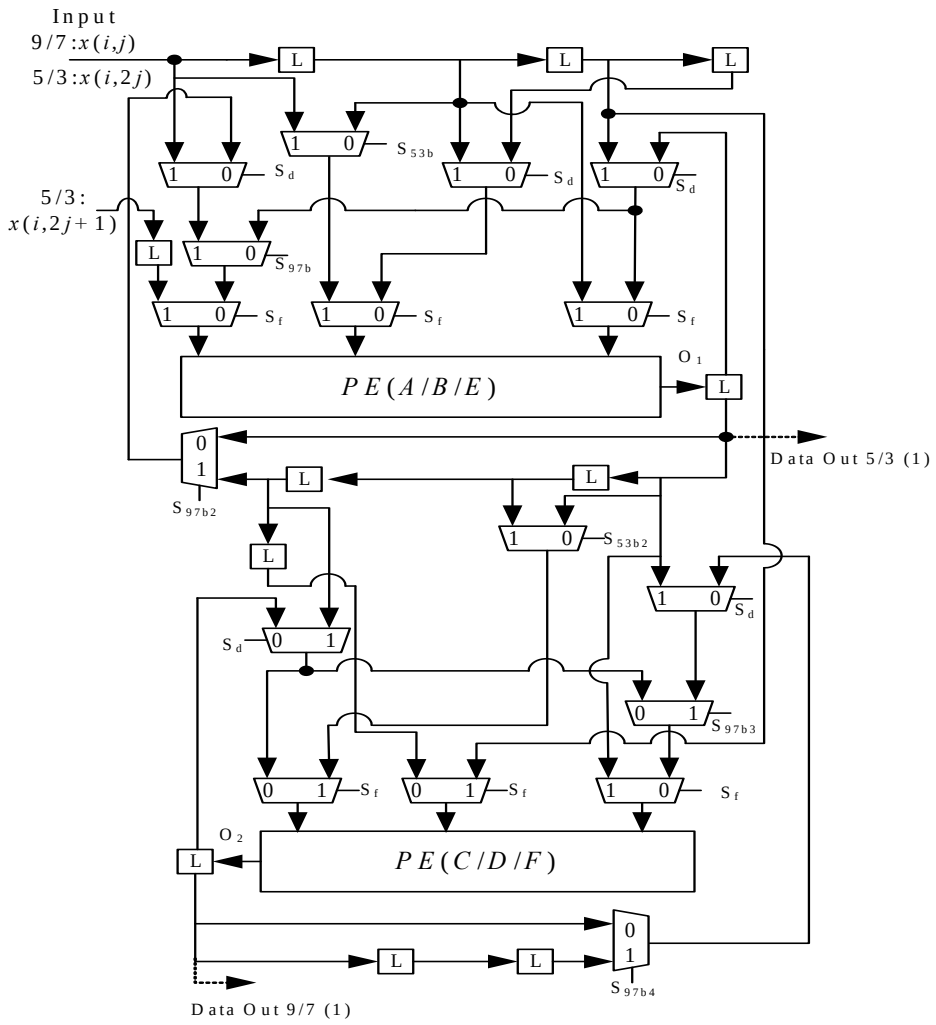


Fig. 6 The architecture of horizontal filter (HF) in the proposed reconfigurable architecture

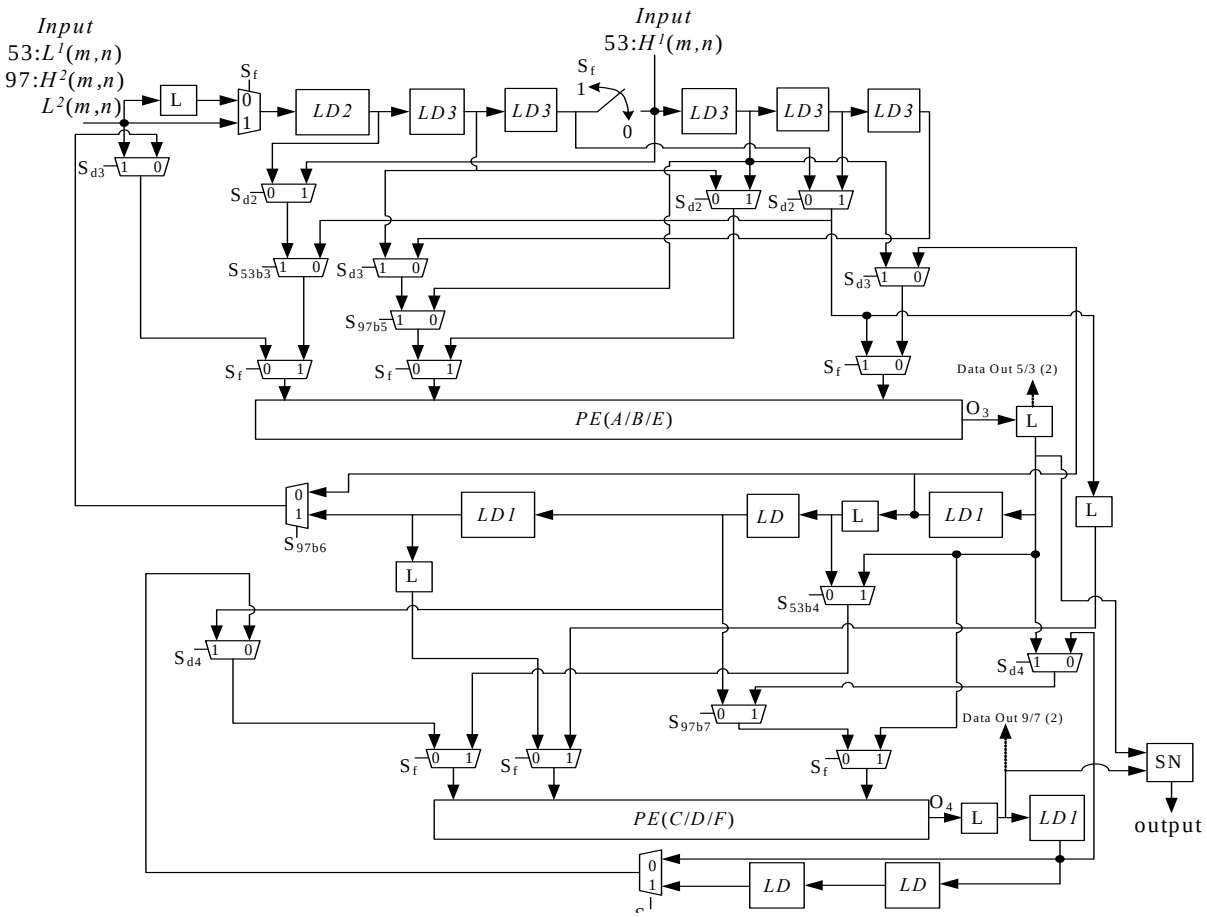


Fig. 7 The architecture of vertical filter (VF) in the proposed reconfigurable architecture

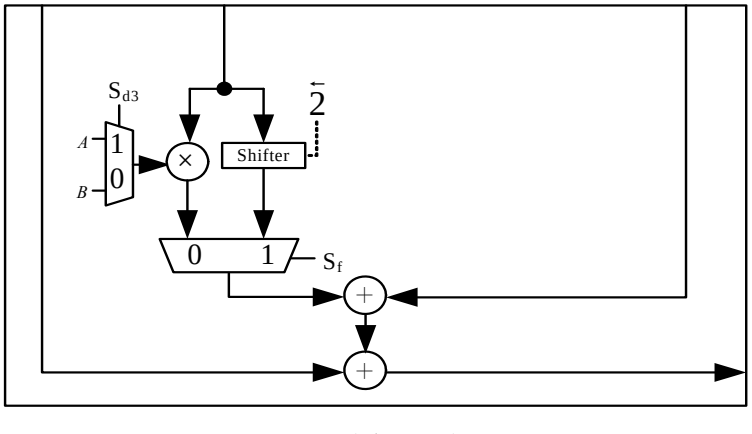
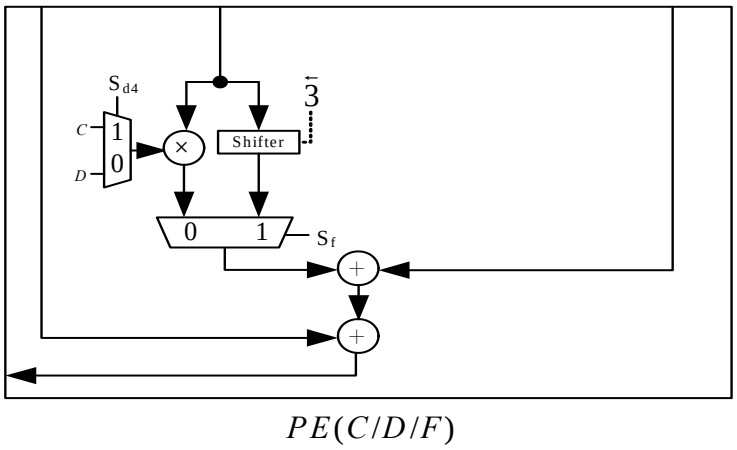


Fig. 8 The architecture of *PE*(*A/B/E*) in the proposed reconfigurable architecture



$PE(C/D/F)$

Fig. 9 The architecture of *PE*(*C/D/F*) in the proposed reconfigurable architecture

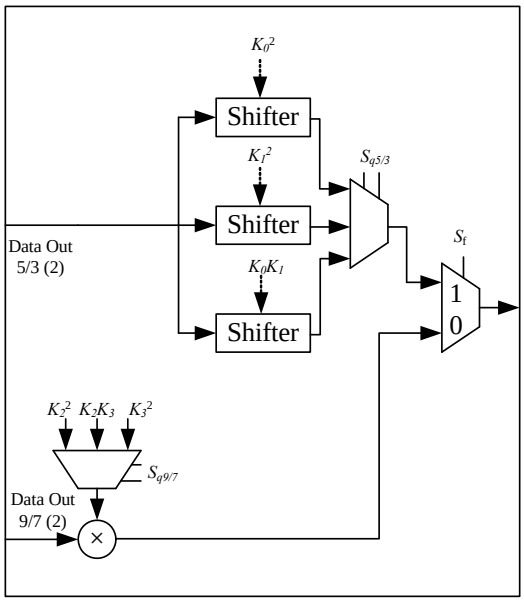


Fig. 10 The architecture of scaling normalization (SN) in the proposed reconfigurable architecture

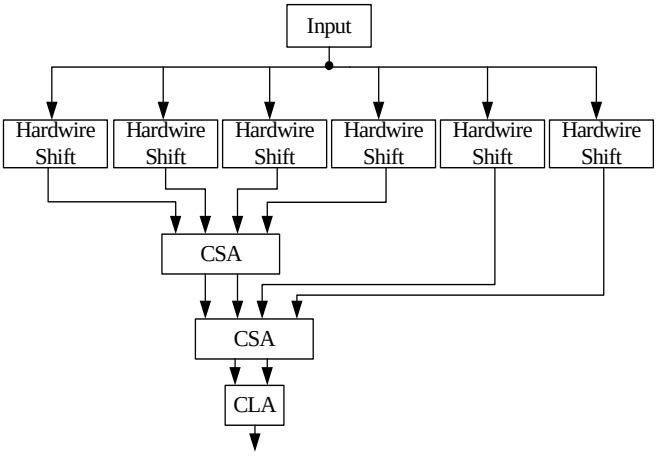


Fig. 11 The constant multiplier replaces conventional multiplier $(\otimes)$ in *PE*(*A/B/E*), *PE*(*C/D/F*) and SN

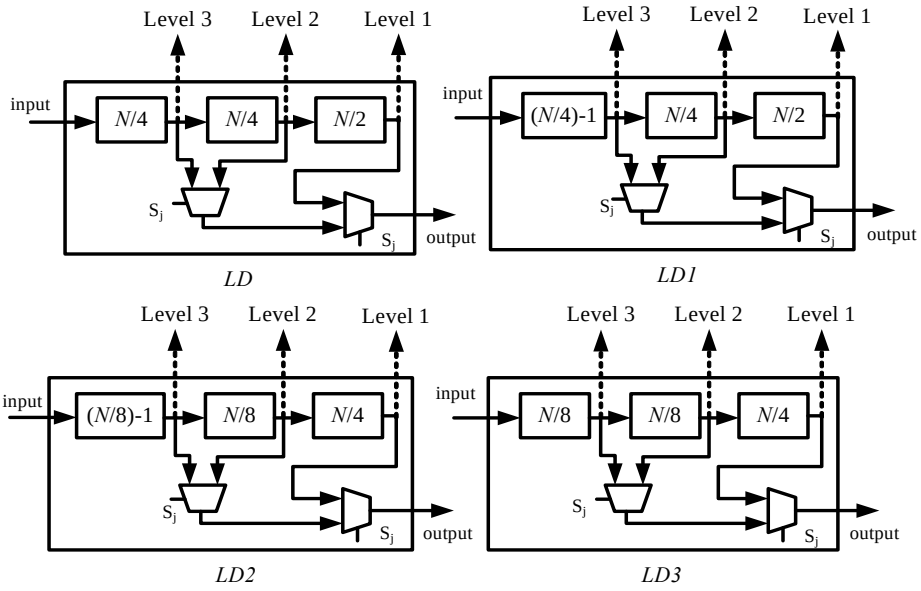
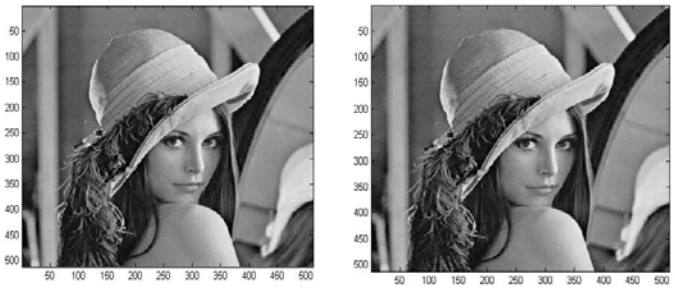


Fig. 12 The architectures of line delays *LD*, *LD1*, *LD2* and *LD3* in vertical filter



(a) (b)

Fig. 13 512×512 Lena (a) Original image (b) Reconstructed image (9/7 DWT with 5-level)