A Ring Oscillator with High Temperature Independency

MOHAMMAD HASSAN MONTASERI
ECE Department
Babol University of Technology
Shariaty St, Babol, Mazandaran
IRAN
mh.montaseri@yahoo.co.uk

Abstract: - A novel temperature independent Ring Oscillator is proposed in this paper. In order to accomplish temperature independency, different characteristics of several delay stages are gathered together in one circuit scheme. Using the temperature property of one kind of delay stage to cancel the other's, has made the proposed architecture show drastically low temperature sensitivity. The proposed architecture was simulated in 0.35μm CMOS technology where the temperature varied from 0 to 50 degrees Celsius, resulting in only 1% frequency deviations.

Key-Words: - Ring Oscillator, Voltage Controlled Oscillators, Ring Oscillators, Temperature Variations, Frequency Stability.

1 Introduction

High integration capability of Ring Oscillators has made them an integral part of many digital and analog systems [1-4]. These building blocks are used as beating heart of applications such as frequency synthesizers [5], clock recovery circuits for serial data communications [6], broad band frequency dividers [7], etc. Stable oscillation frequency is imperative in order to minimize interference in adjacent frequency bands, as far as many communications applications are concerned [8].

The deviation of simple CMOS inverter's oscillation frequency is directly proportional to temperature and supply voltage variations [9, 10]. Lin and Huang [11] proposed a circuit that has very low sensitivity to variations of temperature. Lee and Kim [12] used high speed inverters to alleviate the undesired effects of temperature. Bandgap references were used to bias delay cells independent of both, temperature and supply voltage deviations [13-15].

In this research we have focused on a modified ring oscillator structure which has a more stable oscillation frequency with respect to temperature variations. In this respect, some structures are studied, among which are Maneatis cell and Lee-Kim cell. Simulations clarify some interesting properties for these structures, making theme candidates of a new version.

The next parts of this paper deal with effective factors of oscillation frequency (deviation) in section 2, and some CMOS ring oscillator structures in section 3. The proposed architecture is presented in section 4, and finally section 5 gives a brief conclusion.

2 A Brief Review of Effective Factors of oscillation frequency

There are several elements in MOS transistors which vary with temperature variations including source/drain junction capacitances, threshold voltage, and channel mobility. The following lines investigate the subject briefly.

Researches on oscillation frequency of Ring Oscillators state that mentioned elements are contributors to the oscillation frequency. Therefore, studding the effect of temperature variations on such elements will do a lot good to our understanding of influential factors of frequency deviations.

2.1 Dependency of MOS Capacitances on Power supply

Drain/Source junction capacitances show a changing property with respect to temperature variation. As shown in fig.1, source/drain junction capacitance can be divided into three components: the bottom junction capacitance C_{jb}, the sidewall periphery junction capacitance C_{jpsw} (of the field oxide edge), and the gate-edge periphery junction capacitance C_{jpg}.

According to fig.1, the total source/bulk junction capacitance is:

$$C_{apbs} = C_{jbst} + C_{jbsswgt} + C_{jbsswt} \quad (1)$$

where C_{jbst} is the area capacitance of the source/bulk junction, $C_{jbsswgt}$ is the periphery capacitance of the source/bulk junction at the gate edge and C_{jbsswt} is the periphery capacitance of the source/bulk junction at the field oxide edge.

The area capacitance C_{jbst} can be calculated with

$$C_{jbst} = A_s.C_{jbs} \quad (2)$$

where C_{jbs} is the area capacitance per unit area, the equation of which will be given later in this section. $\boldsymbol{A_S}$ is the area of the source/bulk junction.

If the length of the periphery of the source/bulk junction $\boldsymbol{Ps}$ is larger than the effective channel width W_{eff}, $C_{jbsswgt}$ and C_{jbsswt} are [16]

$$C_{jbsswgt} = W_{eff}.C_{jbsswg} \quad (3)$$

$$C_{jbsswt} = \left(P_s - W_{eff}\right).C_{jbssw} \quad (4)$$

W_{eff} is the effective channel width without bias dependence [17], $\boldsymbol{P_S}$ is the length of the periphery of the source/bulk junction, C_{jbsswg} is the gate edge periphery junction capacitance per unit length, and C_{jbssw} is the field-oxide edge periphery junction capacitance per unit length. Expressions for these capacitances are given later in this section.

If $\boldsymbol{P_s} \leq W_{eff}$, only the gate edge periphery capacitance is considered and it is given by

$$C_{jbsswgt} = P_s.C_{jbsswg} \quad (5)$$

In this case, the total capacitance is given by

$$C_{abps} = A_s.C_{jbs} + P_s.C_{jbsswg} \quad (6)$$

Nine model parameters, $\boldsymbol{C_J}$, $\boldsymbol{P_B}$, $\boldsymbol{M_J}$, $\boldsymbol{C_{JSW}}$, $\boldsymbol{P_{BSW}}$, $\boldsymbol{M_{JSB}}$, $\boldsymbol{C_{JSWG}}$, $\boldsymbol{P_{BSWG}}$, and $\boldsymbol{M_{JSWG}}$ are introduced in the junction capacitance model. $\boldsymbol{C_J}$ is the unit area bottom capacitance at the zero bias, $\boldsymbol{P_B}$ is the built-in potential of the bottom junction, $\boldsymbol{M_J}$ is capacitance grading coefficient of the bottom junction, $\boldsymbol{C_{JSW}}$ is the unit length periphery capacitance at the field oxide edge at zero bias, $\boldsymbol{P_{BSW}}$ is the built-in potential of the sidewall junction at the field oxide edge, $\boldsymbol{M_{JSW}}$ is the capacitance grading coefficient of the sidewall junction at the field oxide edge, $\boldsymbol{C_{JSWG}}$ is the unit-length periphery capacitance at the gate edge at zero bias, $\boldsymbol{P_{BSWG}}$ is the built-in potential of the sidewall junction at the gate edge, and $\boldsymbol{M_{JSWG}}$ is capacitance grading coefficient of the sidewall junction at the gate edge.

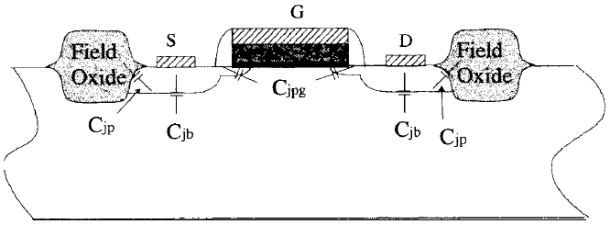


Fig.1 Capacitance components of the source/drain junctions.

Physically, ***CJ, CJSW,*** and ***CJSWG*** cannot be less than zero. If ***CJ, CJSW***, or ***CJSWG*** is not larger than zero, the corresponding total capacitance such as *Cjbst*, *Cjbsswt*, and *Cjbsswgt* is set to zero in the model implementation [18].

Equations set (7) describe Drain/Source junction capacitances. As it is implied by (7), these junction capacitances are also functions of bias voltages across them. The same equation format holds for *Cjbssw* and *Cjbsswg* if one changes the related subscripts with those of *Cjbs*.

$$\begin{aligned} C_{jbs} &= C_J\left(1 - \frac{V_{bs}}{P_B}\right)^{-M_J} : V_{bs} < 0 \\ C_{jbs} &= C_J\left(1 + M_J \frac{V_{bs}}{P_B}\right) : V_{bs} \geq 0 \end{aligned} \quad (7)$$

The drain-bulk capacitance is modeled with the same equations after substituting *s* with *d* in the subscripts.

Fig.2 shows an example of the calculated area junction capacitance per unit area as the bias changes. The bias dependence of the periphery junction capacitances is similar to this.

For the source/drain junctions in a MOSEFT, the temperature dependences of the saturation current and the junction capacitance at zero bias are important and need to be modeled.

It is known that the temperature dependence of the saturation current, *Is*, of a p-n junction is determined by the temperature dependence of the intrinsic carrier density, n_i , or the energy band gap of the material, E_g [19], [20], [21]. The temperature dependence of the zero-bias junction capacitance Cj_0 is determined by the temperature dependences of the dielectric constant of silicon material, ε_{Si}, and the junction built-in potential, V_{bi} [19], [21].

The temperature dependence of the source/drain junction capacitance is modeled by introducing the temperature-dependent zero-bias unit area/perimeter junction capacitances *Cj(T)*, *Cjsw(T)*, and *Cjswg(T)*, and junction built-in potentials *Pb(T)*, *Pbsw(T)*, and *Pbswg(T)*.

The temperature dependence of the zero-bias junction capacitance is modeled with the following

equations [22]:

$$\begin{aligned} C_j(T) &= C_J[1+T_{CJ}(T-TNOM)] \\ C_{jsw}(T) &= C_{JSW}[1+T_{CJSW}(T-TNOM)] \\ C_{jswg}(T) &= C_{JSWG}[1+T_{CJSWG}(T-TNOM)] \end{aligned} \quad (8)$$

where *Cj(T)*, *Cjsw(T)* and *Cjswg(T)* are zero-bias junction capacitance per unit area, the perimeter junction capacitance per unit length at the field-oxide edge, and the perimeter junction capacitance per unit length at the gate edge. $\boldsymbol{C_J}$, $\boldsymbol{C_{JSW}}$, and $\boldsymbol{C_{JSWG}}$ are the zero-bias capacitances at the nominal temperature $\boldsymbol{T_{NOM}}$. $\boldsymbol{T_{CJ}}$, $\boldsymbol{T_{CJSW}}$, and $\boldsymbol{T_{CJSWG}}$ are the model parameters for the temperature coefficients of C_j, C_{jsw}, and C_{jswg}.

The temperature dependence of the built-in potentials in the junction capacitances is modeled with the following equations [22]:

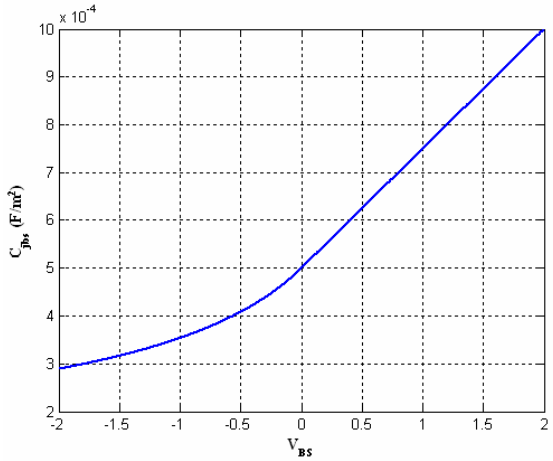


Fig.2 The area Capacitance in different bias conditions

$$\begin{aligned} P_b(T) &= P_B - T_{PB}(T-T_{NOM}) \\ P_{bsw}(T) &= P_{BSW} - T_{PBSW}(T-T_{NOM}) \\ P_{bswg}(T) &= P_{BSWG} - T_{PBSWG}(T-T_{NOM}) \end{aligned} \quad (9)$$

where *Pb(T)*, *Pbsw(T)*, and *Pbswg(T)* are the built-in potentials of the bottom junction, the periphery junction at the field-oxide edge, and the periphery junction at the gate edge at temperature $\boldsymbol{T}$ in Kelvin. $\boldsymbol{P_B}$, $\boldsymbol{P_{BSW}}$, and $\boldsymbol{P_{BSWG}}$ are the built-in potentials of the bottom junction, the periphery junction at the field-oxide edge, and the periphery junction at the gate edge at the nominal temperature $\boldsymbol{T_{NOM}}$. $\boldsymbol{T_{PB}}$, $\boldsymbol{T_{PBSW}}$, and $\boldsymbol{T_{PBSWG}}$ are the temperature coefficients of the built-in potentials.

C_{jbs}, the area capacitance of the source/bulk junction with temperature effects, is calculated by:

$$\begin{aligned} C_{jbs} &= C_j(T)(1-\frac{V_{bs}}{P_b(T)})^{-M_J} \rightarrow if: V_{bs} < 0 \\ C_{jbs} &= C_j(T)(1-M_J\frac{V_{bs}}{P_b(T)}) \rightarrow if: V_{bs} \geq 0 \end{aligned} \quad (10)$$

C_{jbssw}, the periphery capacitance of the source/bulk junction at the field oxide edge with temperature effects, and C_{jbsswg}, the periphery capacitance of the source/bulk junction at gate oxide edge with temperature effects, are calculated by the same naming rule. To do so it is sufficient to replace the subscripts of C_{jbs} with that of C_{jbssw} or C_{jbsswg}.

The equations for the temperature dependence of the drain/bulk junction are the same as the above except for the obvious change of the subscripts from "s" to "d" in (1) through (10).

Fig.3 shows the minor influence of temperature change on the junction capacitance.

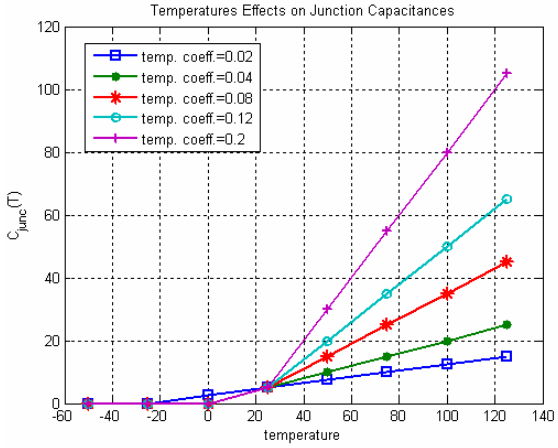


Fig.3 The junction capacitance at several temperatures.

2.2 The Dependency of Threshold Voltage on Temperature

Due to body effect V_{th} is a function of V_{bs} [23]. The following temperature model of V_{th} is used in our simulations. It can be proved that with body effect

$$V_{th} = V_{th_o} + \gamma\left(\sqrt{\left|2\Phi_F + V_{SB}\right|} - \sqrt{\left|2\Phi_F\right|}\right) \quad (11)$$

Where V_{th_o} is the threshold voltage without body effect considerations, Φ_F is the surface potential at threshold V_{th_o}, and γ denotes the body effect coefficient.

The following temperature model of V_{th} is used in BSIM3 [17], [24], [25]:

$$V_{th}(T) = V_{th}(T_{NOM}, L, V_{ds}) + (K_{T1} + \frac{K_{T1L}}{L} + K_{T2}V_{bs})(\frac{T}{T_{NOM}} - 1) \quad (12)$$

where $V_{th}(\boldsymbol{T_{NOM}}, L, V_{ds})$ is the threshold voltage value at $\boldsymbol{T_{NOM}}$. The expression for $V_{th}(\boldsymbol{T_{NOM}}, L, V_{ds})$ has been given in [23], [25], [26]. The parameters $\boldsymbol{K_{T1}}$, $\boldsymbol{K_{T1L}}$, and $\boldsymbol{K_{T2}}$ are extracted from the experimental data. $\boldsymbol{K_{T1}L/L}$ is a minor term introduced to improve the fitting accuracy. The following figure shows the impact of temperature variations on V_{th}.

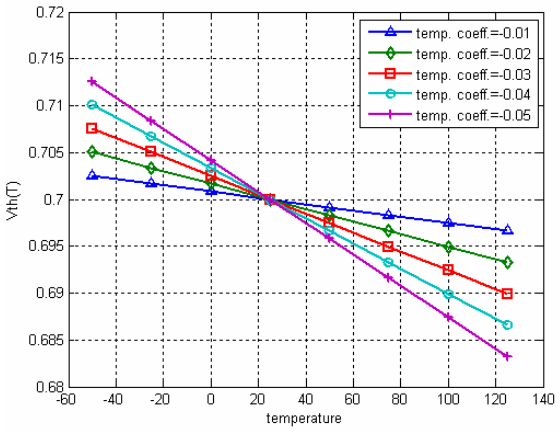


Fig.4 Variations of *Vth* in terms of temperature

2.3 Modeling the temperature dependence of mobility

Several empirical unified formulations have been suggested to describe the mobility as a function of process parameters and bias conditions [27-30]. However, all of them contain a quantity, E_{eff}, which is not readily available for circuit simulation. It has been shown that E_{eff} may be expressed simply as $(V_{gs}+V_{th})/(6T_{ox})$ [31]. The effects of V_{bs} and doping concentration are reflected in the V_{th} term. The following exponential equation is proposed by [32] to relate the temperature dependency of mobility.

$$\mu_{eff} = \mu_0 (T / T_{NOM})^{-K_1} \quad (13)$$

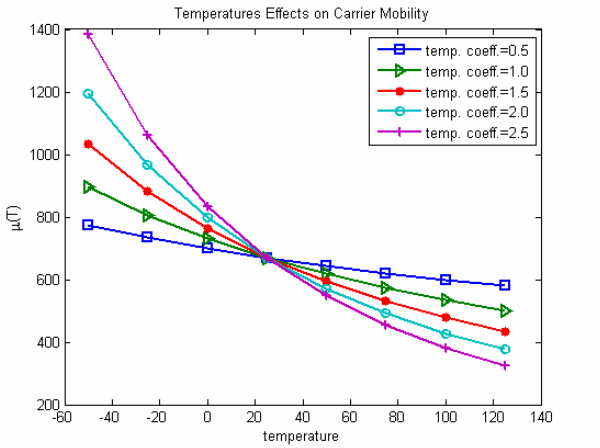


Fig.5 The mobility at several temperatures.

Fig.5 reveals the temperature dependency of carrier mobility. As can be seen from fig.5, temperature affects carrier mobility violently.

3 CMOS Ring Oscillator and Temperature Independent Architectures; A Brief Review

A ring oscillator is composed of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a dc inversion [9]. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the dc inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped. Examples of these two circuits are shown in fig.6.

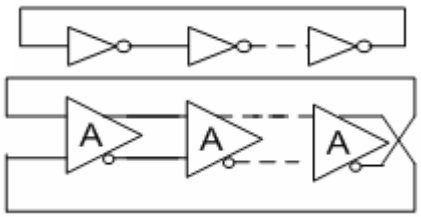


Fig.6 Single-ended and differential-ended ring oscillators

There are several types of inverter stages by which a ring oscillator can be realized [14]. Among a variety of ROs, CMOS inverter, Maneatis cell, and Modified Lee-Kim structures are of great importance. For the rest of this section, the foregoing cells are reviewed.

3.1 Simple CMOS Inverter

The very first practical topology used as RO is CMOS inverter. Its schematic is drawn in fig.7 and its coordinate of frequency vs. temperature is shown in fig.8. This structure uses no precision mechanism against temperature variation. Therefore, temperature variation affects the behaviour of the circuit in a direct manner [10, 11].

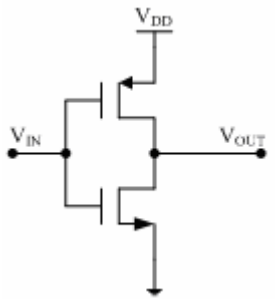


Fig.7 simple CMOS inverter

In fig.8 it is shown that sensitivity of oscillation frequency with respect to power supply variations is approximately 0.08. In this structure if temperature varies by 10 percent, oscillation frequency deviates by 8 percent, which is intolerable.

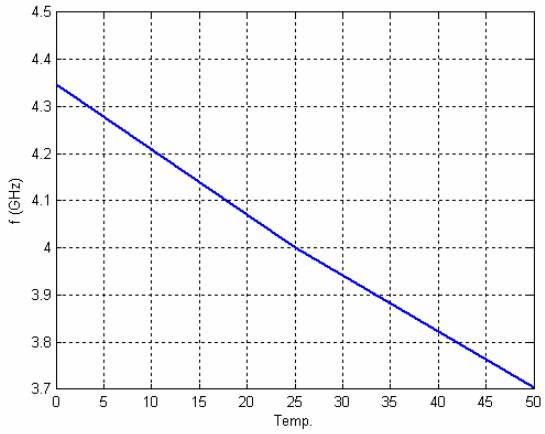


Fig.8 the effect of temperature variations on oscillation frequency

Simulations showed that in case of device scaling, sensitivity may change slightly. But variations were small enough to be ignored.

3.2 Maneatis Cell

Maneatis proposed to use differential Ring with symmetrical load like the one shown in fig.9. Apart from being completely symmetric, Maneatis used self-biasing concept. This way temperature, process, and any other deviations from desired frequency make the circuit back to the quiescent frequency.

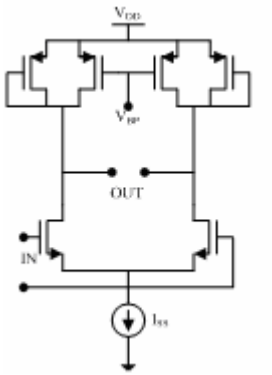


Fig.9 Maneatis delay cell

This is achieved through a combination of three bias circuits; a voltage reference, a current reference, and the replica bias. These circuits are shown in figures 10, 11, 12 respectively. These building blocks are described in more detail in references [33], [34] and [35].

The voltage reference develops a ΔV_{be} mismatch across a fixed resistance to generate a PTAT current. This current is then drawn through another resistor attached to the supply to give a reference voltage of

$$V_{ref} = V_{DD} - \frac{KT}{q}.\ln(X).\frac{R_2}{R_1} \quad (14)$$

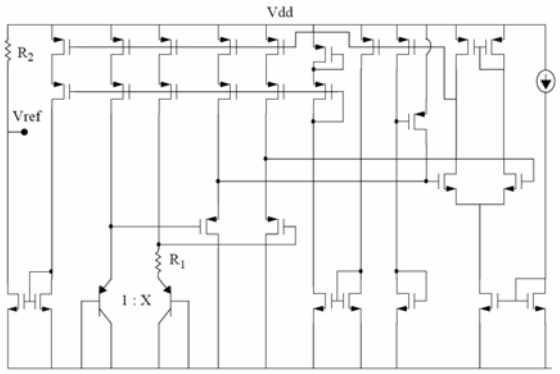


Fig.10 Voltage reference generator

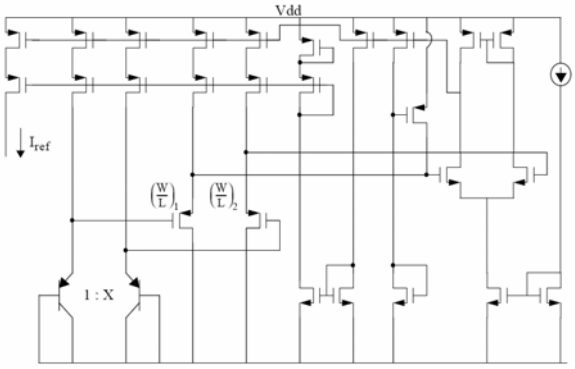


Fig.11 Current reference generator

where X is the ratio of the PNP device sizes. This reference voltage is used in the replica bias circuit to set the nominal DC output swing. The swing is therefore proportional to absolute temperature and is insensitive to the power supply variations. It depends on a ratio of resistances, which match reasonably well over process variations, and to a ratio of device areas.

$$V_{SW} = \frac{KT}{q}.\ln(X).\frac{R_2}{R_1} \qquad (15)$$

The current reference uses a feedback loop match ΔV_{be} a mismatch in pair of bipolar devices to a $\Delta(V_{GS} - V_{th})$ mismatch in a pair of MOS devices. The end result is a current that depends on the thermal voltage *kT/q*, device sizes, and device mobility.

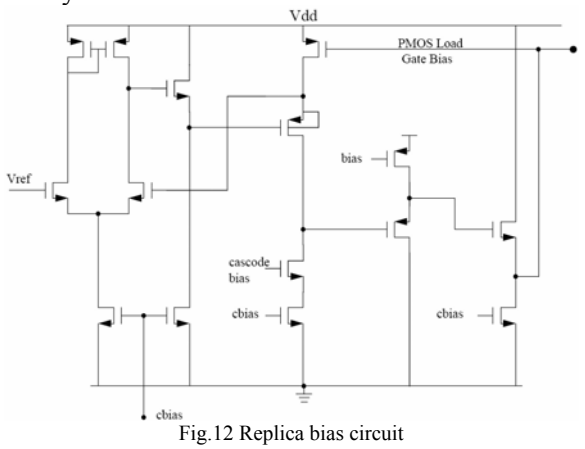


Fig.12 Replica bias circuit

Including the effects of temperature on device mobility, this current has a net temperature dependence of somewhere between $T^{1/2}$ and T^{1}. Therefore, the time delay per stage has a net temperature dependence that is between $T^{1/2}$ and constant.

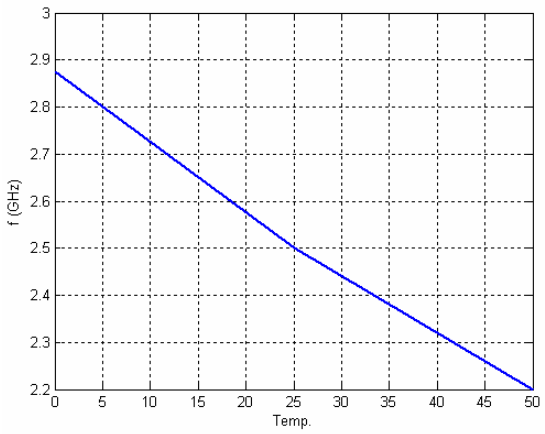


Fig.13 effect of temperature variations on oscillation frequency of Maneatis cell

3.3 Modified Lee-Kim Cell

Using the method proposed by Lee-Kim and a little bit modification of the circuit results in the following structure which has been proved to be drastically independent of temperature variations.

The proposed delay cell, illustrated in figure 14, is based on a differential NMOS input pair with an active load. This load consists of a cross-coupled PMOS pair, connected to the control transistor, in parallel with two resistors directly connected to the supply voltage. The PMOS pair is equivalent to a negative resistance. While the gate voltage of the control MOS increases, the injected current decreases so the negative resistance becomes less negative. Then the total load resistance of the input pair increases, thereby lowering the frequency of the oscillation.

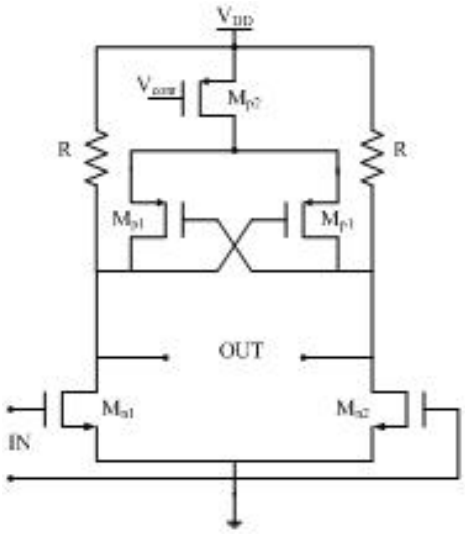


Fig.14 modified Lee-Kim cell

Using the Barkhausen criteria, we obtain the oscillation frequency of the RO [36]:

$$f = \frac{1}{2\pi}\sqrt{\frac{g^2{}_{mn1} - (1/R - g_{mp1})^2}{(C + C_{gdp1})^2 - C^2{}_{gsn1}}} \qquad (16)$$

According to frequency equation mentioned before, the oscillation frequency directly depends on the transconductance of the NMOS transistor Mn1 and the PMOS cross coupled one Mp1. Now, these two kinds of transistors have different temperature behavior. According to [37], If K_1 is chosen to be (-1.5) temperature dependent channel mobility, (13), will be

$$\mu(T) = \mu_o\left(\frac{T}{T_o}\right)^{-1.5} \qquad (17)$$

As shown in (18), $g_{mn}(T)$ and $g_{mp}(T)$ depends both on the mobility and on the threshold voltage. Let us

plot in the same graph the temperature behavior of each transconductance g_{mn_1} and g_{mp_1}.

$$g_{mn} = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th}) \qquad (18)$$

As shown in figure 15, each transconductance doesn't exhibits the same variation in temperature. We can note here that the g_m variation of the transistors M_{n1} and M_{p1} depends both on their own temperature dependence and on the variation versus temperature of the control current provided by $M_{p2\text{-}p4}$. Since the oscillation frequency is expressed as a function of the difference of g_{mn_1} and g_{mp_1}, the resulting output value presents significant temperature drift (1291ppm! 0 C).

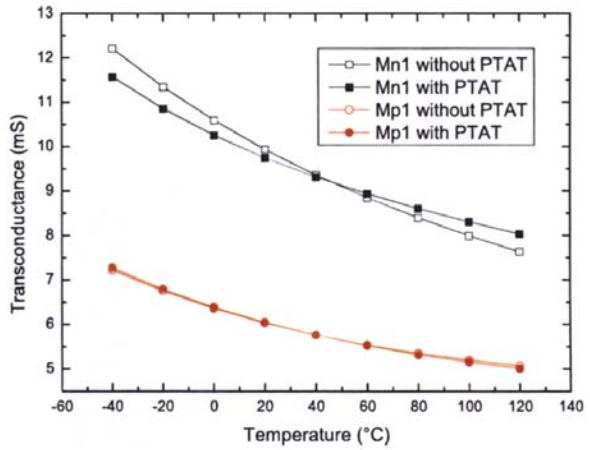


Fig.15. The RO transistors transconductance versus temperature

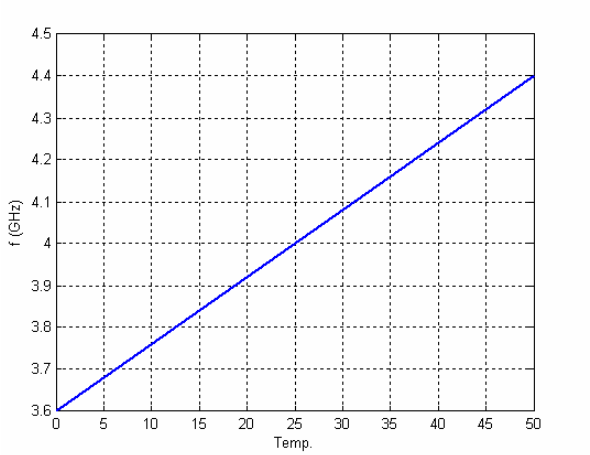


Fig.16 frequency deviations vs. temperature variations for modified Lee-Kim delay cell

4 The proposed structure

As shown in figures 8, 13, 15, all structures output frequency suffers from temperature variations which doesn't meet most of telecommunication systems specifications and must be compensated for.

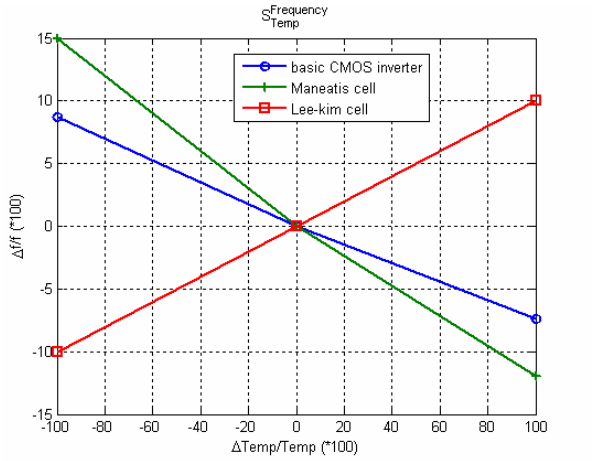
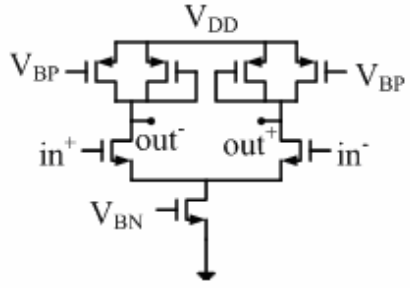


Fig.17 temperature behaviour of mentioned delay cells

By analysing curves, it is apparent that normalized frequency deviations in terms of temperature variations for Maneatis and Modified Lee-Kim cells change oppositely. From this, the idea is to make oscillators independent of temperature by combining the mentioned building blocks as a new oscillator. The definition of what was explained is sketched in the frame of temperature behaviour curves in Fig. 17. This figure gives some insight into behaviour of different delay stages. Most importantly is that of Maneatis and Lee-Kim. Taking into consideration the opposite slope characteristics of the relative frequency deviations in terms of temperature variations of the mentioned inverters , we can conclude that, it is reasonable to design a ring oscillator composed of cascade chain of inverters.

So based on the above idea and considering the profiles in fig. 17, the proposed structure is shown in fig 18. Since temperature behaviour of Maneatis and Lee-Kim cells differ only in sign, the proposed structure uses these structures in the loop for complete compensation. And to exactly eliminate the effect of each stage, even number of stages have been used.



(a)

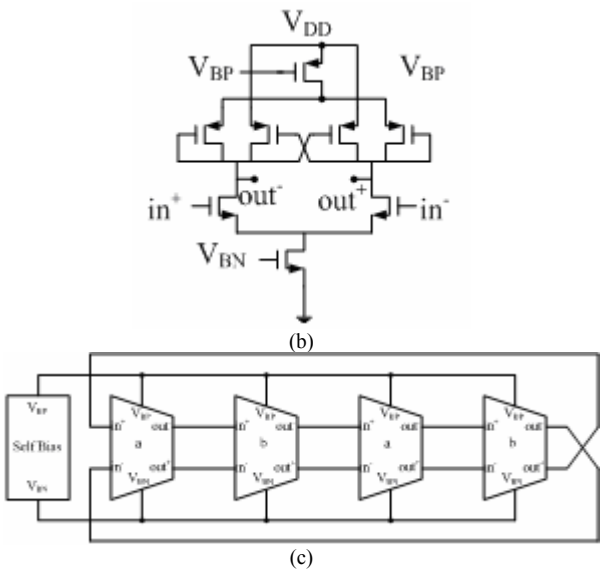


Fig.18 The proposed ring oscillator structure

Our proposed structure is composed of four stages. Two of them are Maneatis cell and the other two are modified Lee-Kim cell. As mentioned before, since the desired cells behave oppositely with respect to temperature variations, these cells neutralize each other. Hence the total frequency deviation with respect to temperature variations is theoretically zero. Simulation results show that the proposed oscillator has a more stable frequency in terms of temperature variations than previous had, as shown in Fig.20.

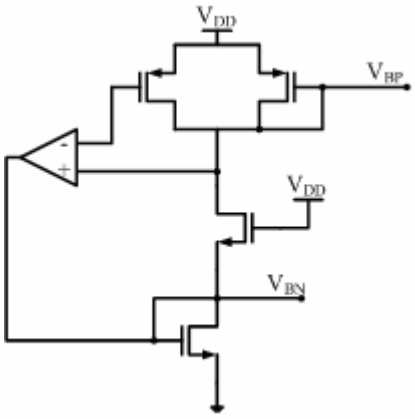


Fig.19: Self-bias circuit

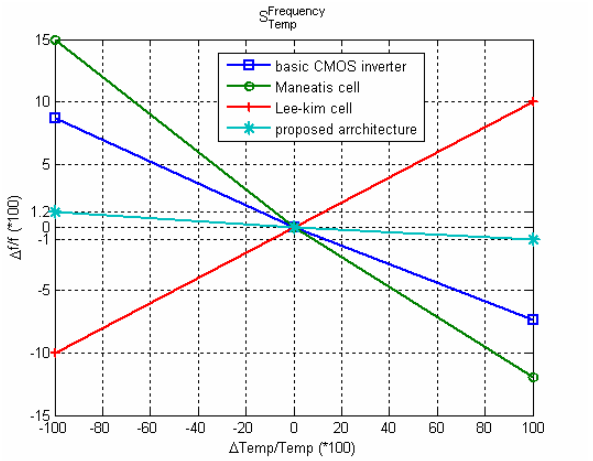


Fig.20: Relative frequency deviations in terms of temperature variations of the ring

Simulations were performed in HSpice BSMI4 model. As mentioned in [35] Maneatis cell has the property of reduced oscillation frequency characteristic. We have used (0.5/5) µm channel length/width for Maneatis cell to achieve higher frequencies. For the case of Lee-Kim cell the same dimensions as Maneatis cell were used. For CMOS inverter circuits (0.5/50) µm channel length/width has been used. During simulation, device dimensions kept constant, or else different characteristics would have been achieved.

Frequency variations were normalized to the center frequency of each ring oscillator to make comparison easier.

5 Conclusion

In this paper we considered dependency of different ring oscillators' output frequency upon temperature variations. Finally, simulation results showed that the proposed method increased the frequency stability of ring oscillator in terms of temperature variations. For more research we intend to derive analytical equation to descry.

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