A Ring Oscillator of Remarkable Power Supply Independent Characteristic

MOHAMMAD HASSAN MONTASERI
ECE Department
Babol University of Technology
Shariaty St., Babol, Mazandaran
IRAN
mh.montaseri@yahoo.co.uk

Abstract: - A highly power supply independent Ring Oscillator architecture is proposed in this paper. The proposed architecture is achieved using the advantages of best previous techniques. Making use of opposite characteristics of the delay cells along with power supply isolation and self-biasing have resulted in a nearly 1% sensitivity; a record better than all previous architectures. To accomplish such robustness, different delay stages with different characteristics have been used in the proposed architecture. Simulations based on 0.5µm CMOS technology confirm robustness of the proposal.

Key-Words: - Ring Oscillator, Voltage Controlled Ring Oscillator, Power Supply Variation, Frequency Stability.

1 Introduction

A Ring Oscillator (RO) in the frame of Voltage Controlled Oscillator (VCO) is one of the most important basic building blocks in analog and digital circuits [1-4]. There are many different implementations of ROs. The main reason of ring oscillator's popularity is a direct consequence of its easy integration. Due to this, ring oscillators have become integral part of many digital and communication systems. These building blocks are used in applications such as frequency synthesizers [2], clock recovery circuits for serial data communications [3], broad band frequency dividers [4]. The performance of the mentioned systems highly depends on the robustness of the oscillation frequency [5]. So the oscillation frequency should not be sensitive to variation of power supply and temperature; a problem that oscillators naturally suffer from. It has been shown that the oscillation frequency of simple CMOS inverters is varying in direct proportion to supply variations [6, 7]. These all show the necessity for designing new robust architectures.

To this end several works have been performed on making oscillators more robust against variations of power supply. To increase frequency stability of simple ring oscillator, Jovanović and Stojčev have proposed to use a combination of the simple inverter and current starved delay cell. The reported results show 4.2% variation of oscillation frequency. Maneatis has used the concept of self-biasing in combination with negative feedback with a 3% variation of oscillation frequency [8]. Lee and Kim proposed high speed delay cells and deduce that this decreases the oscillation frequency dependency upon power supply. They reported a 6% variation in oscillation frequency [9]. However, high performance systems need more robust oscillators than above mentioned proposals [5]. In this paper, combining the previous techniques, we try to reach more robust oscillators. In the proposed architecture in some stages only one of the mentioned techniques is implemented and in some other another, so delay stages of the proposed architecture are not the same.

The rest of the paper is organised as follows. Section 2 deals with an introduction to effective factors of oscillation frequency deviations. In section 3 a brief description of ring oscillators is given. Afterwards, some MOS RO implementations are reviewed. The proposed architecture is presented in section 4. In section 5, performances of different structures are compared. Finally conclusions and some offers are given in section 6.

2 A Brief Review of Effective Factors of Oscillation Frequency

There are several elements in MOS transistors which vary with power supply variations including intrinsic capacitances, extrinsic capacitances, and threshold voltage. The following lines investigate the subject briefly.

Researches on oscillation frequency of Ring

Oscillators state that mentioned elements are contributors to the oscillation frequency. Therefore, studding the effect of power supply on such elements will do a lot good to our understanding of influential factors of frequency deviations.

2.1 Dependency of MOS Capacitances on Power Supply

One of the most widely used gate capacitance models is Meyer model. Fig.1 shows the capacitances defined by this model. As it is apparent from Fig.5, there is one capacitance between each pair of two terminals of MOSFET transistor.

Let us have a glance at capacitance equations in different working regions [10], [11]. This will lead to make a better judgment about varying property of capacitances. As one knows, there are three operating regions for MOSFETs: Strong Inversion consisting of saturation region, and linear region, Weak Inversion, and Accumulation. According to the mentioned regions different equations are presented as below.

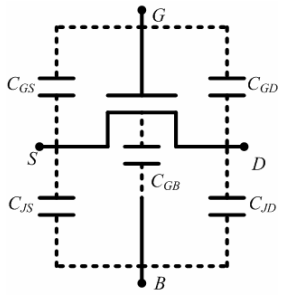

Fig.1 An illustration of the capacitances presented by the Meyer capacitance model.

$$C_{GS} = \frac{2}{3} WLC_{ox} \tag{1}$$

(1) Gives information about capacitances in saturation region where C_{ox} is the gate oxide capacitance per unit area. There is a physical explanation for C_{GD} being zero in the saturation region. In the saturation region, the channel is pinched off at the drain end of the channel. This electrically isolates the channel from the drain so that the charge on the gate is not influenced by a change in the drain voltage, and the capacitance C_{GD} vanishes.

$$C_{GS} = \frac{2}{3} WLC_{ox}\left[1 - \frac{(V_{gd} - V_{th})^2}{(V_{gs} - V_{th} + V_{gd} - V_{th})^2}\right] \tag{2}$$

$$C_{GD} = \frac{2}{3} WLC_{ox}\left[1 - \frac{(V_{gs} - V_{th})^2}{(V_{gs} - V_{th} + V_{gd} - V_{th})^2}\right] \tag{3}$$

$$C_{GB} = 0 \tag{4}$$

V_{gs} is the gate to source voltage and V_{th} is threshold voltage, Remembering that $V_{gd} = V_{gs} - V_{ds}$.

It is to be expected that C_{GB} is zero in strong inversion since the inversion layer in the channel from the drain to the source shields the gate from the bulk and prevents any response of the gate charge to a change in the substrate bias, V_{bs}. This is approximately true in the strong inversion case. However, C_{GB} can not be considered zero in the weak inversion and accumulation regions.

In weak inversion, (5)-(7), the charge in the inversion layer can be ignored compared with the depletion charge, so

$$C_{GS} = 0 \tag{5}$$

$$C_{GD} = 0 \tag{6}$$

$$C_{GB} = \frac{WLC_{ox}}{\sqrt{1 + \frac{4}{\gamma^2}(V_{gb} - V_{FB})}} \tag{7}$$

where γ is the body effect coefficient and V_{FB} is the flat band voltage. It is the gate voltage at which the surface potential is zero, the surface electric field is zero, and the entire substrate is charge neutral [12]. With a description of accumulation region, (8), the story of gate capacitances is finished.

$$C_{GB} = C_{ox} \;\&\; C_{GS} = C_{GD} = 0 \tag{8}$$

In all foregone equations, C_{GS}, C_{GD}, and C_{GB} are Gate-Source, Gate-Drain, and Gate-Bulk capacitances respectively. Figures 2-4 show varying property of these capacitances with respect to power supply variations.

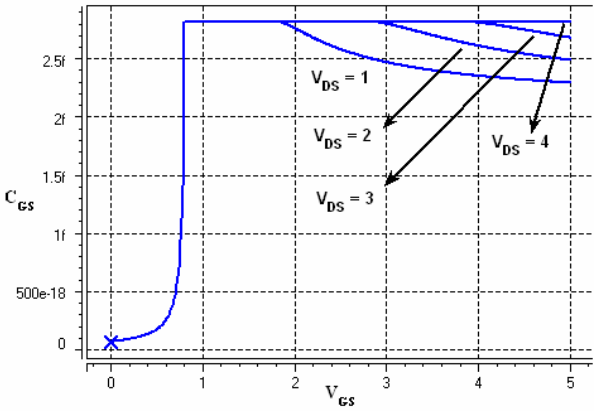

Fig.2 varying property of gait-source capacitance with power supply

Figure 2 profiles C_{GS} behaviour in different

working regions. In fact this plot consists of 3 regions. Region one is the values for which V_{GS} is less than V_{th}, called sub-threshold region. The second part points to the saturation region where $V_{DS} \geq V_{GS} - V_{th}$. Finally appears triode region where $V_{DS} \leq V_{GS} - V_{th}$. As is obvious from this figure, the only interval for which C_{GS} is independent of power supply is saturation region.

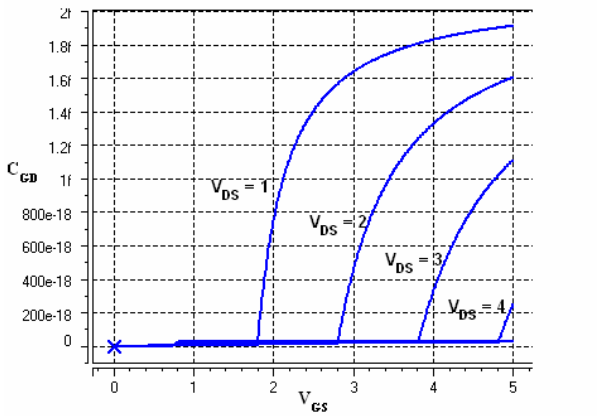

Fig.3 functionality of gait-drain capacitance with respect to power supply

The same explanations as C_{GS} hold for C_{GD}. Figure 3 shows three working regions. Parts one and two show, where $V_{DS} \geq V_{GS} - V_{th}$, that as V_{GS} increases C_{GD} varies slightly. As soon as transistor enters triode region, C_{GD} starts to show off itself.

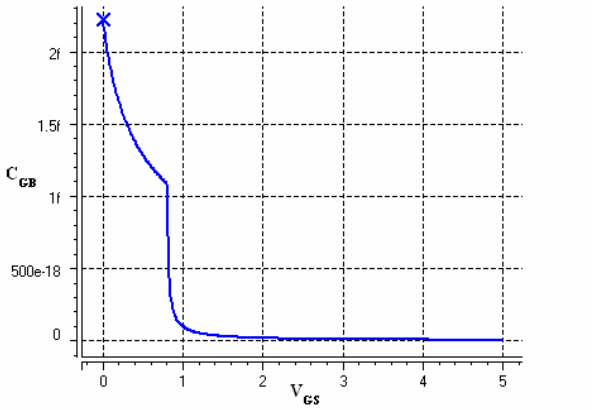

Fig.4 varying nature of gait-bulk capacitance with power supply

Figure 4 does emphasise what equation (8) implies. As the transistor reaches the on-condition, C_{GB} drops to zero.

Besides gate capacitances, Drain/Source junction capacitances show off as well. As shown in Fig.5, source/drain junction capacitance can be divided into three components: the bottom junction capacitance C_{jb}, the sidewall periphery junction capacitance C_{jpsw} (of the field oxide edge), and the gate-edge periphery junction capacitance C_{jpg}.

According to Fig.5, the total source/bulk junction capacitance is:

$$C_{apbs} = C_{jbst} + C_{jbsswgt} + C_{jbsswt} \quad (9)$$

where C_{jbst} is the area capacitance of the source/bulk junction, $C_{jbsswgt}$ is the periphery capacitance of the source/bulk junction at the gate edge and C_{jbsswt} is the periphery capacitance of the source/bulk junction at the field oxide edge.

The area capacitance C_{jbst} can be calculated with

$$C_{jbst} = A_s.C_{jbs} \quad (10)$$

where *Cjbs* is the area capacitance per unit area, the equation of which will be given later in this section. $\boldsymbol{A_S}$ is the area of the source/bulk junction.

If the length of the periphery of the source/bulk junction $\boldsymbol{Ps}$ is larger than the effective channel width W_{eff}, $C_{jbsswgt}$ and C_{jbsswt} are [13]

$$C_{jbsswgt} = W_{eff}.C_{jbsswg} \quad (11)$$

$$C_{jbsswt} = (P_s - W_{eff})C_{jbssw} \quad (12)$$

W_{eff} is the effective channel width without bias dependence [14], $\boldsymbol{P_S}$ is the length of the periphery of the source/bulk junction, C_{jbsswg} is the gate edge periphery junction capacitance per unit length, and C_{jbssw} is the field-oxide edge periphery junction capacitance per unit length. Expressions for these capacitances are given later in this section.

If $\boldsymbol{P_s} \leq W_{eff}$, only the gate edge periphery capacitance is considered and it is given by

$$C_{jbsswgt} = P_s.C_{jbsswg} \quad (13)$$

In this case, the total capacitance is given by

$$C_{abps} = A_s.C_{jbs} + P_s.C_{jbsswg} \quad (14)$$

Nine model parameters, $\boldsymbol{C_J}$, $\boldsymbol{P_B}$, $\boldsymbol{M_J}$, $\boldsymbol{C_{JSW}}$, $\boldsymbol{P_{BSW}}$, $\boldsymbol{M_{JSB}}$, $\boldsymbol{C_{JSWG}}$, $\boldsymbol{P_{BSWG}}$, and $\boldsymbol{M_{JSWG}}$ are introduced in the junction capacitance model. $\boldsymbol{C_J}$ is the unit area bottom capacitance at the zero bias, $\boldsymbol{P_B}$ is the built-in potential of the bottom junction, $\boldsymbol{M_J}$ is capacitance grading coefficient of the bottom junction, $\boldsymbol{C_{JSW}}$ is the unit length periphery capacitance at the field oxide edge at zero bias, $\boldsymbol{P_{BSW}}$ is the built-in potential of the sidewall junction at the field oxide edge, $\boldsymbol{M_{JSW}}$ is the capacitance grading coefficient of the sidewall junction at the field oxide edge, $\boldsymbol{C_{JSWG}}$ is

the unit-length periphery capacitance at the gate edge at zero bias, P_{BSWG} is the built-in potential of the sidewall junction at the gate edge, and M_{JSWG} is capacitance grading coefficient of the sidewall junction at the gate edge.

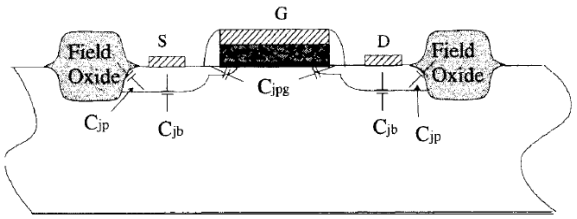

Fig.5 Capacitance components of the source/drain junctions.

Physically, ***CJ, CJSW,*** and ***CJSWG*** cannot be less than zero. If ***CJ, CJSW***, or ***CJSWG*** is not larger than zero, the corresponding total capacitance such as *Cjbst*, *Cjbsswt*, and *Cjbsswgt* is set to zero in the model implementation [12].

Equations set (15) describe Drain/Source junction capacitances. As it is implied by (15), these junction capacitances are also functions of bias voltages across them. The same equation format holds for *Cjbssw* and *Cjbsswg* if one changes the related subscripts with those of *Cjbs*.

$$C_{jbs} = C_J(1-\frac{V_{bs}}{P_B})^{-M_J} : V_{bs} < 0$$
$$C_{jbs} = C_J(1+M_J\frac{V_{bs}}{P_B}) : V_{bs} \geq 0 \quad (15)$$

The drain-bulk capacitance is modeled with the same equations after substituting *s* with *d* in the subscripts.

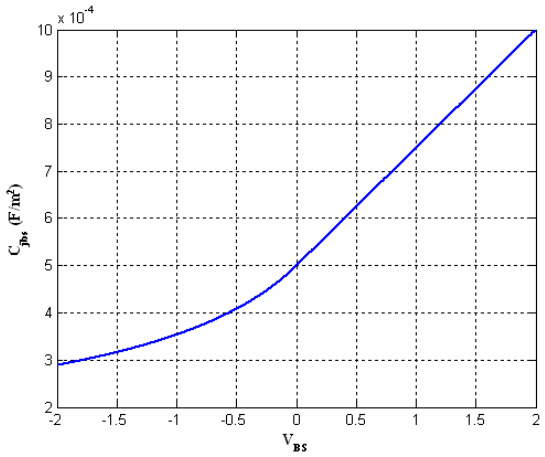

Fig.6 The area Capacitance in different bias conditions

Fig.6 shows an example of the calculated area junction capacitance per unit area as the bias changes. The bias dependence of the periphery junction capacitances is similar to this.

2.2 The Dependency of Threshold Voltage on Power Supply

Due to body effect V_{th} is a function of V_{bs} [7]. The following temperature model of *Vth* is used in our simulations. It can be proved that with body effect

$$V_{th} = V_{th_o} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right) \quad (17)$$

Where V_{tho} is the threshold voltage without body effect considerations, Φ_F is the surface potential at threshold V_{tho}, and γ denotes the body effect coefficient.

3 CMOS Ring VCO and Supply Independent Architectures; A Brief Review

A ring oscillator is composed of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a dc inversion [6]. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the dc inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped. Examples of these two circuits are shown in fig.7.

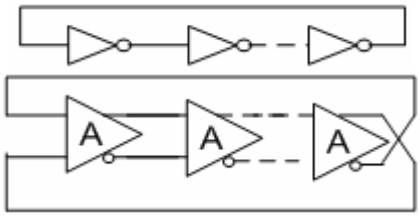

Fig.7 Single- and differential-ended ring oscillators

There are several types of inverter stages by which a ring oscillator can be realized [15]. Some of the most widely used structures are Simple CMOS inverter, Current Starved delay cell, Maneatis cell, and Lee-Kim cell. In the following subsections these fundamental structures will be explained briefly.

3.1 Simple CMOS Inverter

The first practical topology used as RO is CMOS inverter. Its schematic is drawn in fig.8 and its

frequency vs. power supply is shown in fig.11. Since it directly is coupled with power supply, it's oscillation frequency deviates in direct proportion to the variations of power supply voltage [6, 7].

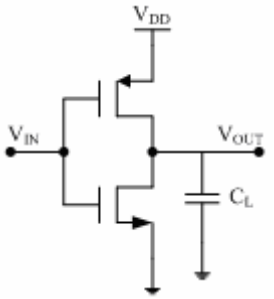

Fig.8 Simple CMOS inverter

Having a glance at propagation delay of this delay cell will give further information for later comparison. Although propagation delay is computed in different manner, we have just considered one part of a whole. To start with, let us assume that the circuit output is in the transient from high to low. It is obvious that the n-channel device is on while p-channel one is off. Writing KCL for the output node yields:

$$C_L \frac{dV_{out}}{dt} + I_n(t) = 0 \qquad (18)$$

where C_L can both be effective parasitic and/or external capacitance. Subscript "n" refers to n-channel device. Since it helps to gain an insight into the effect of power supply variations on frequency deviations as easily as possible, the device is approximately assumed to be in saturation region during discharging, although it is not correct in general. Therefore

$$I_n(t) = k_n(V_{in} - V_{tn})^2 \qquad (19)$$

The key simplification to solve the above equation is unit step function i.e., $V_{in} = U(t)$.

To work out the propagation delay, an ideal square wave is supposed to stimulate the input. Due to capacitive characteristic of the output node, it takes some time for this node to reach the bounds. Fig.9 shows the input and output waveforms.

As mentioned in fig.8 above, the delay time is composed of two different delay times, t_{pHL} and t_{pLH}, each of which is due to one of the MOS transistors. When the input switches to high the output travels from the high level to low level. This means the NMOS device is on, where PMOS device is off. This means t_{pHL} depends on the characteristics of the n-channel device. On the other hand, when the input switches from high to low, the output starts to increase from the low level to high level. This means that, t_{pLH} is dependent upon p-channel device characteristics.

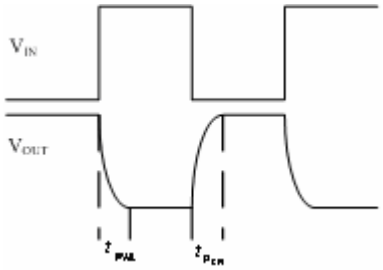

Fig.9 input and put waveforms of simple CMOS inverter

With the above information, it seems logical to separate the circuit for each part of delay time. Hence, to calculate the t_{pHL}, the following circuit will help.

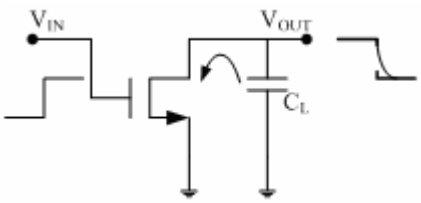

Fig.10 to calculate the t_{pHL} this part of the circuit is required to be analysed.

Now it is sufficient to solve the output differential equation for the saturation region.

$$t_{p_{HL}} = \frac{C}{k_n}\left(\int_{V_{DD}-V_{tn}}^{V_{DD}} \frac{dv_o}{(V_{DD}-V_{tn})^2}\right) = \frac{C}{k_n}\frac{V_{tn}}{(V_{DD}-V_{tn})^2} \qquad (20)$$

$$k_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} \qquad (21)$$

By the same token, charging C_L is done through p-channel device. Then

$$t_p = \frac{C_L}{k_p}.\frac{|V_{tp}|}{(V_{DD}-|V_{tp}|)^2} \qquad (22)$$

According to the mention terminologies, oscillation frequency is

$$f_{osc} = \frac{1}{t_d} \qquad (23)$$

$$t_d = \frac{t_p + t_n}{2} \qquad (24)$$

As seen from (20) and (22) one implies that power supply effects delay time directly. i.e., any change in power supply voltage will affect the propagation delay and, in turn, oscillation frequency is affected.

Below is sketched oscillation frequency vs. power supply for simple inverter based ring oscillator. As is apparent sensitivity of output frequency with respect to power supply variations is 0.681 which is considerably high. This value has the meaning of a 6.81 percent deviation of frequency in case of 10 percent of power supply variation.

Simulations showed that in case of device scaling, sensitivity may change slightly. But variations were small enough to be ignored.

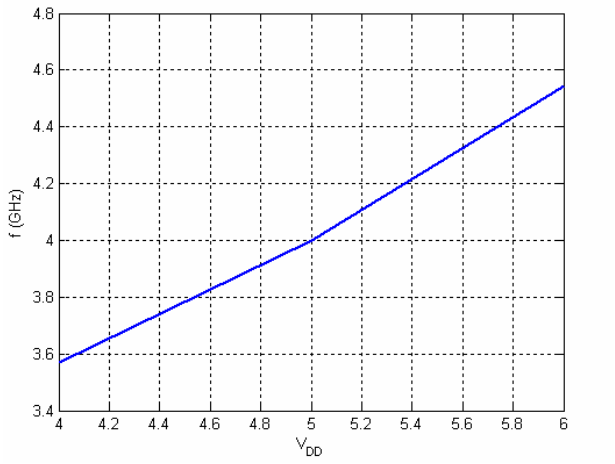

Fig.11 frequency deviations vs. power supply deviations for CMOS inverter

3.2 Current Starved Delay Cell

Shown in fig.12 is one of the most interesting delay stages for supply independent ROs called Current Starved delay cell. In this type, the current of output capacitor is limited by a bias circuit.

As can be seen from figure 12, the voltage controlled delay element is implemented as a one-stage inverter. MOSFETs M_1 and M_2 are constituents of the inverting property, while transistors M_3 and M_4 form the bias circuit which is independent of power supply. In fact these transistors operate as sink and source currents, respectively, for the inverter stage. For push–pull type elements such as inverters, the delay can be changed by changing the rate at which the output capacitance, C_L, is charged. Adjusting sink current one can vary the delay. The capacitor C_L is charged during the rising and is discharged during the falling edge of the pulse generated at the output of the mentioned stage. Control voltages V_{BP} and V_{BN} define currents of transistors M_3 and M_4, respectively.

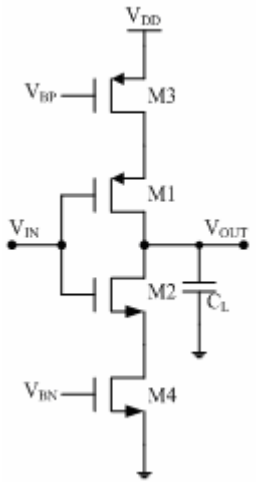

Fig.12 current starved delay cell

As for simple CMOS inverter it is worthy to mention delay time; it gives a good insight. Following the same rule as before, we have:

$$t_n = \frac{C}{k_n}\left(\int_{V_{DD}-V_{tn}}^{V_{DD}} \frac{dv_o}{(V_{DD}-V_{tn})^2}\right) = \frac{C}{k_n}\frac{V_{tn}}{(V_{BN}-V_{tn})^2} \qquad (25)$$

and

$$t_p = \frac{C}{k_p}\frac{|V_{tp}|}{(V_{BP}-|V_{tp}|)^2} \qquad (26)$$

Now from (25) and (26) one deduces that current starved delay cell with output switch is less sensitive to power supply compared to simple inverter. Fig.13 shows the frequency vs. power supply variations for a starved delay cell.

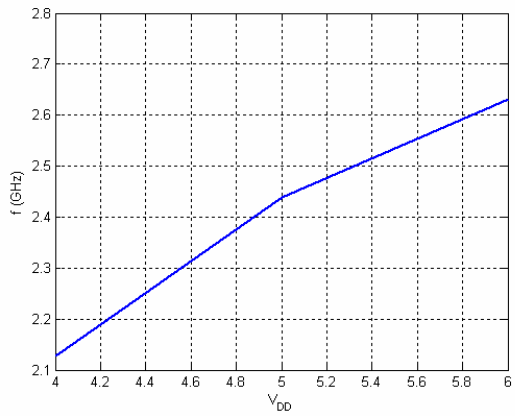

fig.13 frequency deviation in terms of power supply variations for current starved cell

It is shown that in ROs based on starved delay cell, the sensitivity of output frequency with respect to power supply variations is 0.395. Compared to the simple CMOS inverter, an improvement has been achieved using current starved cell. It can be implied that if power supply varies by 10 percent, the frequency deviation would be as much as 3.95 percent of its nominal value.

Simulations showed that in case of device scaling, sensitivity may change slightly. But variations were small enough to be ignored.

3.3 Maneatis Cell

Maneatis proposed to use differential Ring with symmetrical load like the one shown in fig.14. Using symmetrical load with replica feedback biasing, decreases the sensitivity of the oscillator to supply and substrate noise. Apart from being completely symmetric, Maneatis used self-biasing concept. This way isolation from power supply and any other deviations from desired frequency make the circuit back to the quiescent frequency. This is achieved through a combination of three bias circuits; a voltage reference, a current reference, and the replica bias. These building blocks are described in more detail in references [16], [17] and [18].

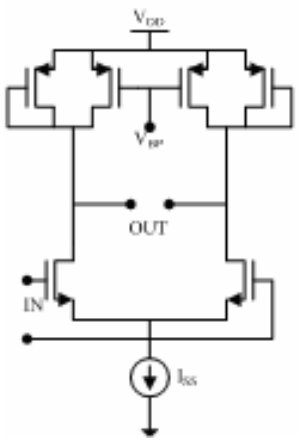

Fig.14 Maneatis delay cell

The replica bias circuit and voltage reference also ensure a swing which is relatively independent of process variations, another important consideration.

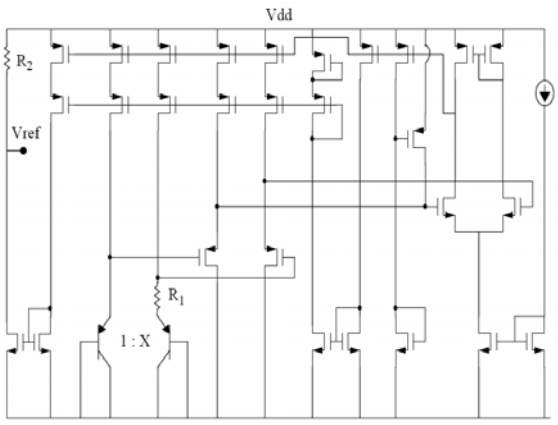

Fig.15 Voltage reference generator

The voltage reference develops a ΔV_{BE} mismatch across a fixed resistance to generate a PTAT current. This current is then drawn through another resistor attached to the supply to give a reference voltage of

$$V_{ref} = V_{DD} - \frac{KT}{q}.\ln(X).\frac{R_2}{R_1} \quad (27)$$

where X is the ratio of the PNP device sizes. This reference voltage is used in the replica bias circuit to set the nominal DC output swing. The swing is therefore proportional to absolute temperature and is insensitive to the power supply variations. It depends on a ratio of resistances, which match reasonably well over process variations, and to a ratio of device areas.

$$V_{SW} = \frac{KT}{q}.\ln(X).\frac{R_2}{R_1} \quad (28)$$

The current reference uses a feedback loop match ΔV_{be} a mismatch in pair of bipolar devices to a $\Delta(V_{GS} - V_{th})$ mismatch in a pair of MOS devices. The end result is a current that depends on the thermal voltage *kT/q*, device sizes, and device mobility. This current is supply independent, so the time delay per stage is independent of supply voltage, to first order, as well. There are some second order effects, such as the variation in some of the load capacitance parasitics with supply voltage, but the net effect is a circuit which is resilient to variations in supply and temperature. The replica bias circuit and voltage reference also insure a swing which is relatively independent of process variations, another important consideration.

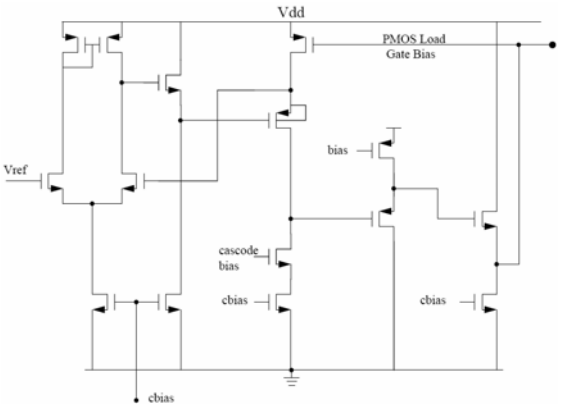

fig.16 Replica bias circuit

Shown below is the frequency deviation of Maneatis cell in terms of power supply deviations. To our surprise, this method proposes a sensitivity of almost nearly -0.3. A 10 percent power supply variation leads to a -3 percent frequency variation.

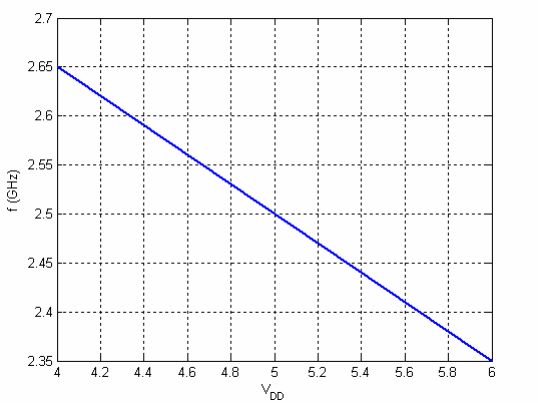

fig.17 frequency deviations vs. power supply variations for the case of Maneatis cell

3.4 Lee-Kim Cell

Lee-Kim Cell is the same as Maneatis, except for that a positive feedback has been applied to improve the output swing. Fig.18 shows the Lee-Kim cell.

The basic delay cell consists of six transistors. The cross-coupled PMOS transistors, M_3 and M_4, guarantee the differential operation of the delay cell without a tail-current bias. Auxiliary PMOS transistors, M_5 and M_6, control the oscillation frequency.

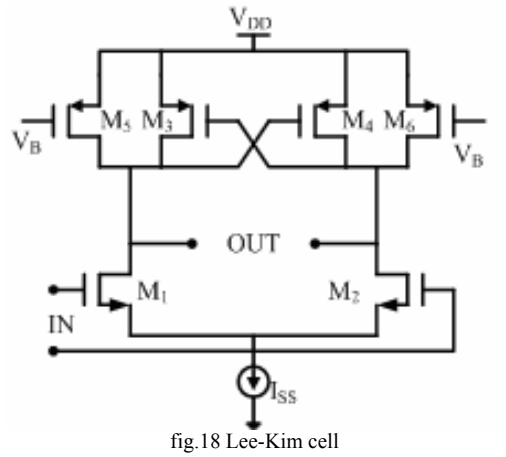

fig.18 Lee-Kim cell

This structure shows a sensitivity of nearly 0.6, expressing 6 percent out of nominal working conditions with respect to 10 percent of power supply variation. Fig.19 visualises what was mentioned above.

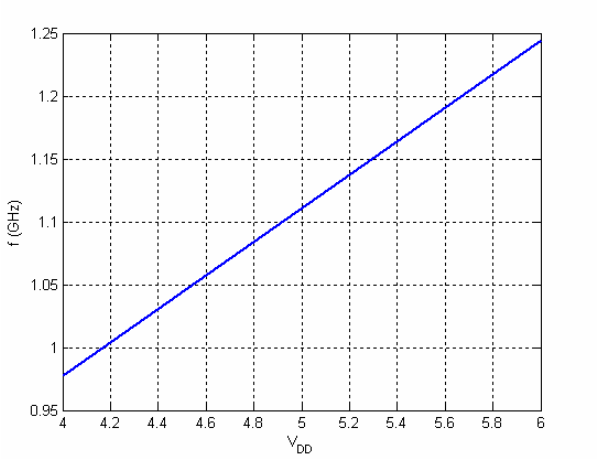

fig.19 Lee-Kim's frequency deviations vs. power supply variations

4 The Proposed supply independent Voltage Controlled Ring Oscillator

In previous section, it was shown that how supply deviations affect the performance of each system. CMOS inverter stages suffer mostly due to direct coupling to supply. (20) Emphasises this. It shows that frequency changes in direct proportion to power supply. Due to this, as an isolation mechanism, in Fig. 12, one transistor is embedded between the main inverter and the supply. To achieve more robustness in terms of power supply instability, another MOS device has been embedded between main inverter and ground [6]. By the help fig 13 and eq (25) it can be deduced that frequency deviation decrease by nearly 2%. In fact, what makes such improvement is high output impedance of load and tail transistors, creating a power supply isolation impression. Maneatis used the isolation mechanism

which interacts with self biasing mechanism [8]. In the self biasing mechanism, as shown in Fig.20, we directly cancel the supply variations to keep oscillation frequency fixed. Here a structure with negative feedback is used to reproduce new robust supply for inverters. As mentioned above, Lee and Kim made the delay cells swing rapidly. Maneatis strategy made the cell a bit slow. This was compensated in Lee-Kim by positive feedback. Fig.17 shows, Maneatis architecture has the best behavior against variations of supply voltage. Current starved is the second in this respect, and Lee-Kim and simple inverter have the weakest behavior.

As mentioned above self-biasing is used to produce a robust supply. Self-bias consists of two stages. As shown in Fig.20, a circuit replica of current source is equipped with negative feedback mechanism. In case of any supply deviation, negative loop changes in indirect proportion to the occurred variation. As a result self-bias mechanism compensates for supply variations.

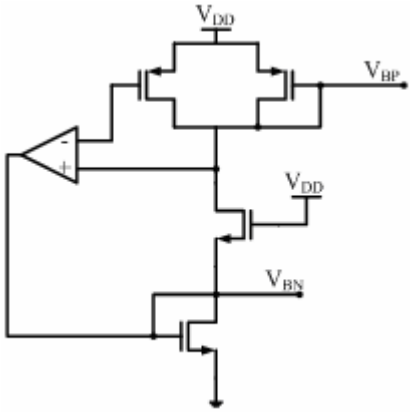

Fig.20 Self-bias circuit

As Fig.17 shows, in Maneatis architecture frequency varies with supply with a negative slope while for the rest, frequency varies with positive slope.

It is reasonable to conclude that a ring oscillator which is composed of cascade chain of different inverters can be designed to build a more robust oscillator. This way, the relative frequency deviation in term of supply voltage can be efficiently reduced. A solution of 3-stage ring oscillator with reduced sensitivity is given in Fig.21.

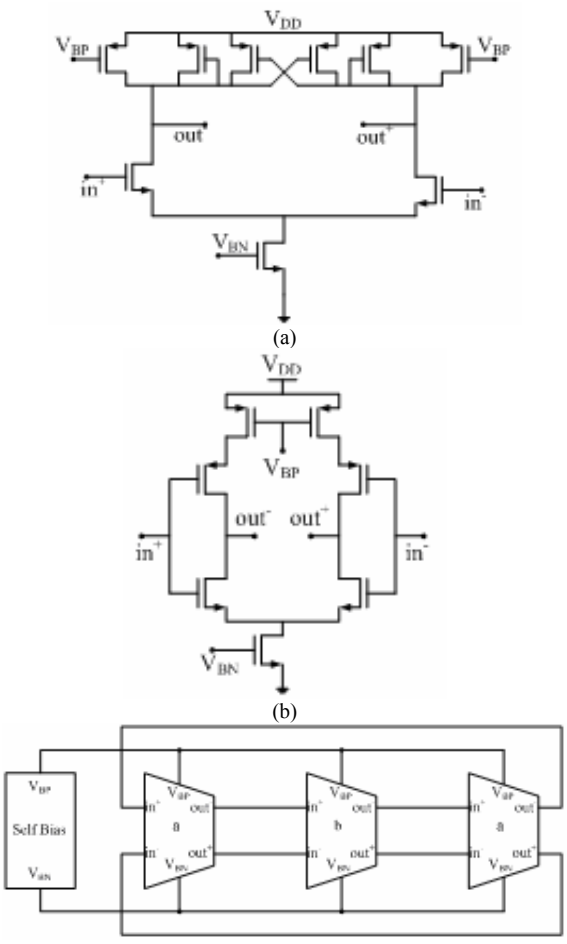

Fig.21: Propose RO structure, a) first last stage of proposed RO, b) middle stage of proposed RO, c) complete structure of the proposed architecture composed of self-bias block, combination of Maneatis and Lee-Kim, and current starved delay stages.

To describe the circuit, it should be noted that, Maneatis delay cell is combined with Lee-Kim delay cell structured as fig.21.a. This way, in addition to power supply rejection, high frequency compensation is achieved. Then, it is followed by current starved delay cell (Fig.21.b) to compensate for decreased deviation slope. Self-biasing can be added to the circuit optionally. Shown in Fig.22 is simulation result of proposed Ring oscillator.

From figure 22, it can be seen that for the worst case sensitivity is 0.12. While power supply changes by 10 percent the proposed structure changes only by 1.2 percent.

As fig.17 shows, Maneatis cell has a negative characteristic with respect to power supply variations. On the other hand other structures show a positive property in terms of power supply deviations. Using Maneatis cell with one of other structures in the chain of ring oscillator makes the architecture robust against power supply variation. To achieve simplicity as well as robustness, Current

starved delay cell were used as the complementary mechanism.

As far as descriptive equations of ring oscillators are concerned, V_{DD} affects current starved cell and Maneatis cell in an indirect manner. Indeed power supply variations affect such structures through bias mechanism, eq (25). Addition of self bias mechanism will lead to a better performance. This is due to the way such a system provides bias, eq(27). Therefore, high supply rejection is achieved by proposed architecture.

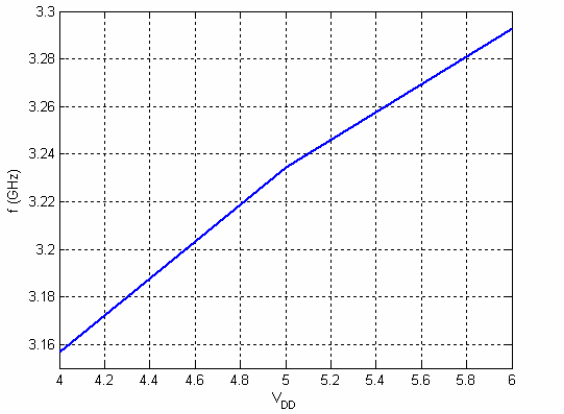

Fig.22 Relative frequency deviation in terms of supply voltage variation for proposed ring oscillator

5 Comparison of Proposed Architecture with Previous Works

To make comparison, frequency deviations of all mention structures are shown in one coordinate plane. In representing the results, frequency variations were normalized to the center frequency of each ring oscillator to make comparison easier. By analysis, it is apparent that the sensitivity of proposed ring oscillator, from Fig.23, is less than 1.2% while for the best case, i.e. Maneatis, it is about 3%.

Simulations were performed in HSpice BSIM4 model. As mentioned above Maneatis cell has the property of reduced oscillation frequency characteristic. (0.5/5) µm channel length/width has been used for Maneatis cell to achieve higher frequencies. For the case of Lee-Kim cell the same dimensions as Maneatis cell were used. For other circuits (0.35/35) µm channel length/width has been used. During simulation, device dimensions kept constant, or else different characteristics would have been achieved.

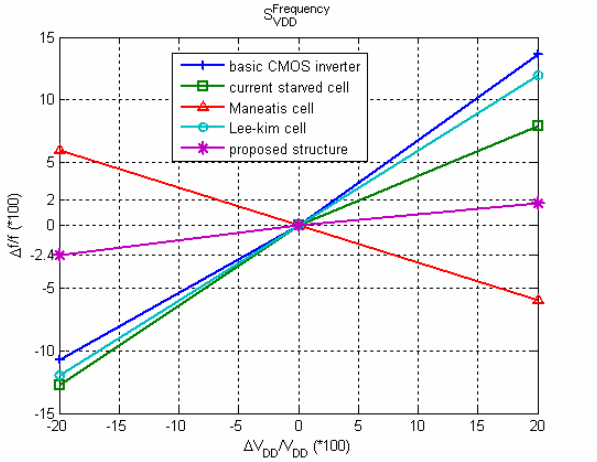

fig.23 sensitivity of proposed structure compared to previous works

6 Conclusions

A robust (Voltage Controlled) Ring oscillator was designed in this paper that was almost independent of supply voltage variations. It has been shown that compared to Maneatis and Lee-Kim delay cells, its relative frequency deviations in terms of supply voltage deviations is improved, i.e. 1.2% whereas for the Maneatis, it is about 3%. For more research one can derive analytical equations relating frequency to supply and consequently optimize the mentioned structures.

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