Adiabatic and Standard CMOS Interfaces at 90 nm Technology

MS. NEHA ARORA, PROF. B.P.SINGH, MS. TRIPTI SHARMA, MR. K.G. SHARMA
Electronics and Communication
Faculty of Engineering and Technology
MITS (Deemed University), Rajasthan
INDIA
neha.241986@gmail.com, bpsingh@ieee.org, tripsha@gmail.com, sharma.kg@gmail.com

Abstract - Adiabatic circuits and standard CMOS logic are widely employed in Low power VLSI chips to achieve high system performance. The power saving of adiabatic circuit can reach more than 90% compared to conventional static CMOS logic. The clocking schemes and signal waveforms of adiabatic are different from those of standard CMOS circuits. This paper investigates the design approaches of low power interface circuits in terms of energy dissipation. Several low power interface circuits that convert signals between adiabatic logic and standard CMOS circuits are presented. With BSIM3v3 90nm CMOS technology, the energy consumption of proposed interface circuits has relatively large power saving over the wide range of frequencies. This paper also investigates the different power delay product over the wide range of supply voltages. Power dissipation has been calculated for different values of temperature. The proposed circuits are showing the best results on various ranges of temperature. Simulation has been done on tanner EDA tool at BSIM3v3 90nm technology.

Key Words – Standard CMOS logic, adiabatic circuit, Interfaces, Low power, Power delay Product, Energy dissipation, Power Dissipation.

1 Introduction

With the development of VLSI technology power dissipation is increasing dramatically. Low power has become one of the crucial design constraint, especially for portable and battery operated systems. In standard CMOS logic circuits, each switching event causes an energy transfer from the power supply to the output node or from the output node to ground. Compared with the conventional low power approaches, power dissipation can be significantly reduced by using the adiabatic computation. By properly mixing the ideas derived for adiabatic and static CMOS circuits one can achieve very low power dissipation in the circuit. Adiabatic logic circuits utilize AC voltage supplies (power-clocks) to recycle the energy of circuit nodes. During recovery phase, the energy of the circuit nodes is recovered to the power source instead of being dissipated as heat. In the adiabatic circuits, circuit nodes are charged and discharged by AC voltage supplies, thus their output signals are clocked AC signals (adiabatic signals). Since, the AC supplies controls the working rhythm of the circuits, they are also called power-clocks. As is well known, a DC power supply and rectangle-wave clocks are used in the standard CMOS circuits, thus the outputs of the standard CMOS circuits are typical rectangle-wave signals (CMOS signals). In order to utilize the strengths of various low power approaches, we consider that both adiabatic logic and standard CMOS circuits co-exist on a single chip.

2 Adiabatic CMOS Interface Circuits

The Adiabatic CMOS Interfaces can be implemented using two approaches. One is based on peak sampling techniques and the other is based on comparators. At 90nm technology the peak sampling technique is inferior because it shows high energy dissipation compared with other techniques. This paper investigates the comparison between interfaces at 90 nm technology.

2.1 Peak Sampling based Technique

The logic value of the adiabatic signal can be sampled and then held using a master-slave flip-flop to attain a standard CMOS output. Fig.1 shows an adiabatic-CMOS interface based on the peak sampling. A positive edge triggered C^2MOS flip-flop

with a master-slave configuration is used to sample the peak voltage of the adiabatic signal. The pc signal is the rectangle-wave clock that comes from the synchronous Power-clock generator. The sampling operation should be switched in the proper phase, i.e. only when the adiabatic signal inclk is at the hold state.

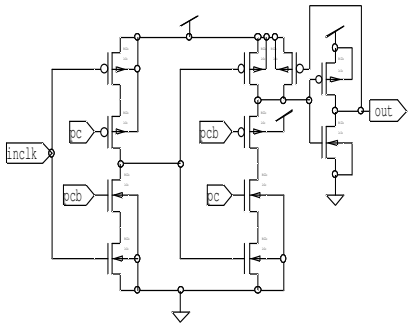

Fig 1 Peak Sampling based Interface

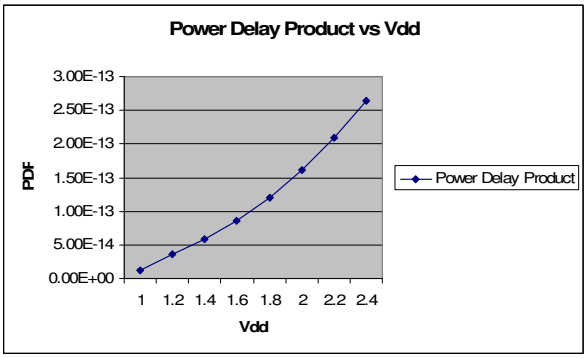

Fig. 2 Power delay product of peak sampling based interface at different values of Vdd

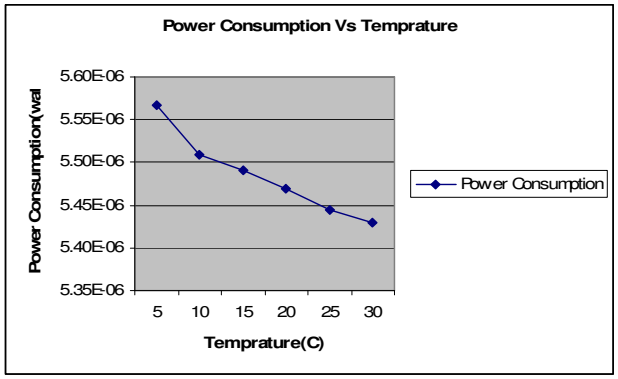

Fig. 3 Power Consumption Vs temperature for peak sampling based interface

Fig. 2 shows the values of power delay product at different values of Vdd. As it is prominent from the graph as we are increasing the value of Vdd the PDP is also increasing. Delay remains constant for all the values of Vdd. This interface does not show appreciable power saving over a range of frequencies at 90nm technology and provides static CMOS output. Fig 3 shows the power consumption over the range of temperatures. Figure reveals that as temperature is increasing power consumption is decreasing.

2.2 Comparator Based Techniques

The adiabatic-CMOS interface can also be realized by using comparators. A Schmitt inverter has been used for the adiabatic-CMOS interface. The schematic is shown in Fig. 4.

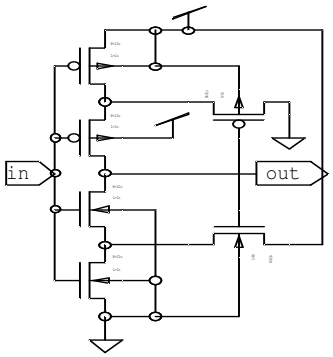

Fig 4 Schmitt Inverter based Interface

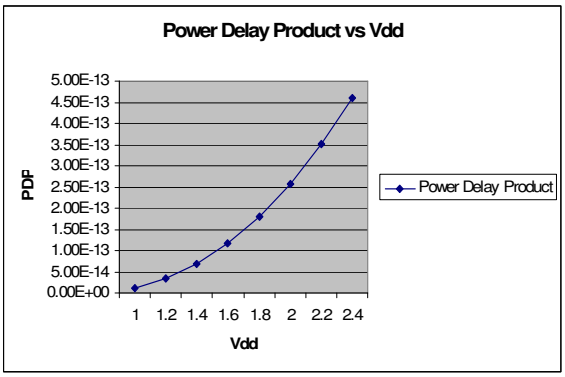

Fig. 5 Power delay product of Schmitt inverter based interface at different values of Vdd

The Schmitt circuit responds to a slowly changing input waveform with a fast transition at the output terminal. Thus, the short-circuit loss of the next-stage circuit can be reduced, while itself has larger short- circuit current because of its positive-feedback configuration. The circuit is simulated using 90nm CMOS technology. At 90nm technology

this circuit shows more power dissipation compared to peak sampling based technique. Fig.5 is depicting the power delay product at various values of Vdd. For all the values of Vdd delay remains constant and power dissipation is increasing as Vdd increases.

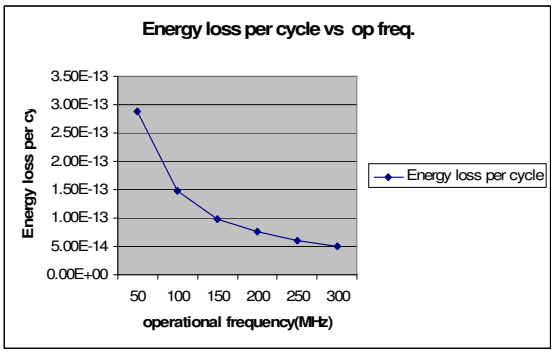

Fig.6 Energy loss per cycle vs. operational frequency

Fig. 6 depicts the energy loss per cycle (joules) over a wide range of frequencies. This circuit provides dynamic CMOS output. Fig. 7 shows the power consumption on different values of temperature. Graph reveals that power consumption for Schmitt inverter is inversely proportional to temperature.

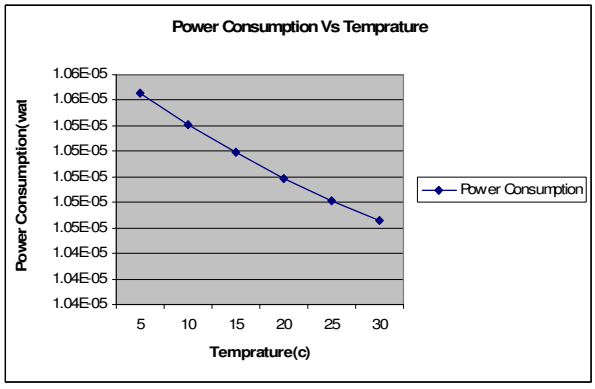

Fig. 7 Power Consumption Vs temperature for Schmitt inverter based interface

Inverter itself is a comparator. It can be used as an Adiabatic CMOS interface circuit as shown in Fig.8. The second stage of inverter can be used to shaping the outputs. Fig. 9 shows the curve between power delay products at different supply voltages. The delay remains constant for all the supply voltages and power dissipation advances as the supply voltages increases. Fig. 10 depicts the energy loss per cycle at different operational frequency. At the maximum operational frequency, the circuit shows the minimum energy loss per cycle. Fig. 11 shows the relation of power consumption with temperature.

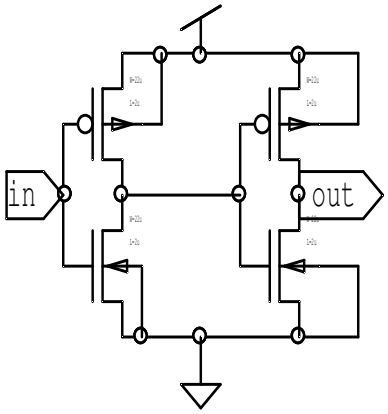

Fig.8 CMOS Inverter based Interface circuit.

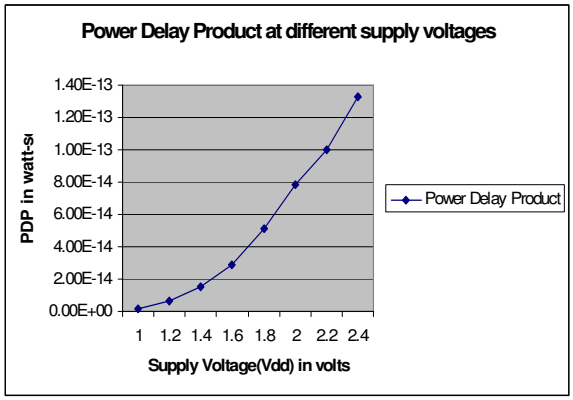

Fig.9 Power delay product at different supply voltages

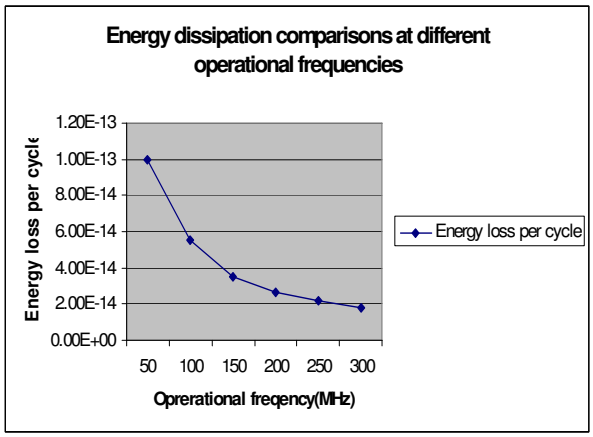

Fig. 10 Energy loss per cycle at different operational frequencies

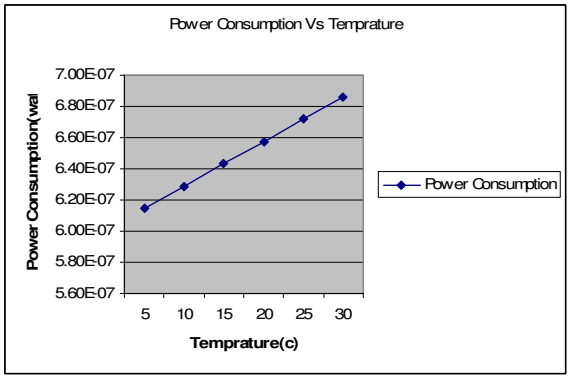

Fig. 11 Power Consumption Vs temperature for CMOS Comparator based interface

The above two circuits have large short-circuit current, because of the gradually rising and falling adiabatic signal. For eliminating the short circuit current a power clocked CMOS (PC^2MOS) inverter is shown in Fig. 12. The second-stage inverter is used for shaping of the output signal. The structure of PC^2MOS is similar to clocked CMOS circuits, but the gate of the P-type and N-type transistors is controlled by the power-clock instead of the rectangle-wave clock used in CMOS circuits. The PC^2MOS has only charging current for the output node *A* when the input signals (*in)* falls. The introduction of the power-clock *clk* doesn't add large energy loss because it operates in a fully adiabatic manner for the gate of the transistors.

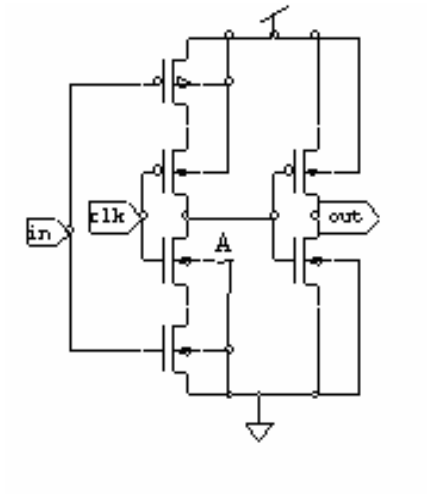

Fig. 12 Power clocked CMOS Comparator based interface circuit.

It is verified that the interface based on the PC^2MOS comparator has low energy loss because the short-circuit dissipation has been completely eliminated. This circuit provides dynamic CMOS output. Fig. 13 shows the power delay product at different values of Vdd. For all the values of Vdd delay remains constant. Power dissipation gradually increases with the increase in Vdd.

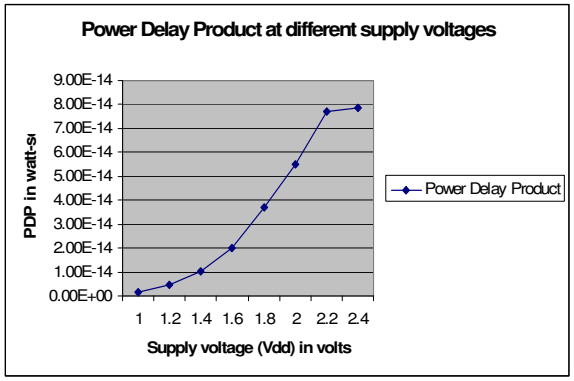

Fig. 13 Power delay product at different supply voltages

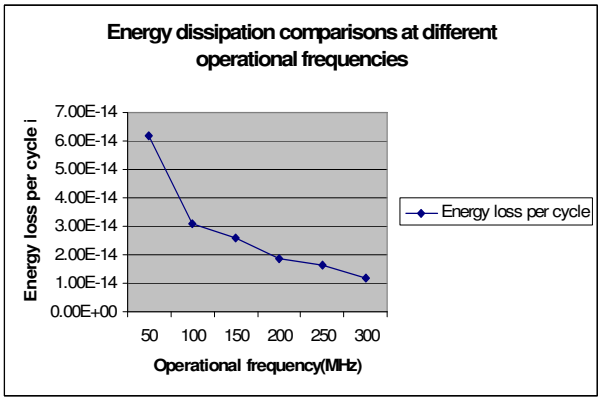

Fig. 14 Energy loss per cycle at different operational frequencies

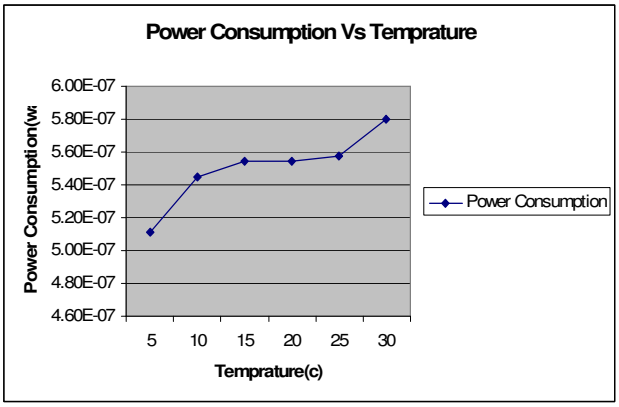

Fig. 15 Power Consumption Vs temperature for Power clocked CMOS based interface

Fig 14 shows the energy loss per cycle over a wide range of frequencies. Energy loss per cycle is decreasing as the Operational frequency is increasing. This circuit provides dynamic CMOS output. Fig 15 shows the relation of power consumption with temperature. Temperature is directly proportional to power consumption.

In order to convert the adiabatic signal into a static CMOS one, an improved power-clocked CMOS (IPC^{2}MOS) inverter is shown in Fig. 16. The second-stage inverter is used for shaping of the output signal. The power-clocks *clk*0, *clk*3, and *clk*2 drive the gates of the transistors, and they are used to avoid the short-circuit current and control the comparison time of the IPC^{2}MOS inverter. The IPC^{2}MOS inverter doesn't have short-circuit current. A standard static CMOS signal can be obtained, because the comparison is only carried during the peak of the adiabatic signal.

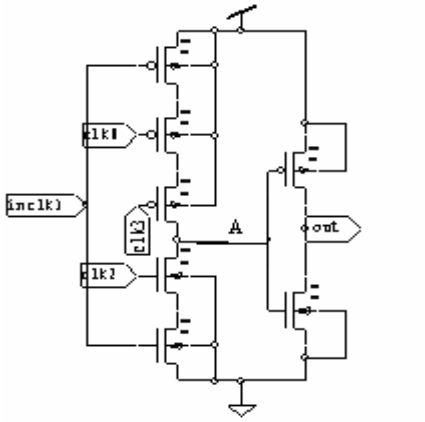

Fig.16 Improved power-clocked CMOS (IPC^{2}MOS) Comparator

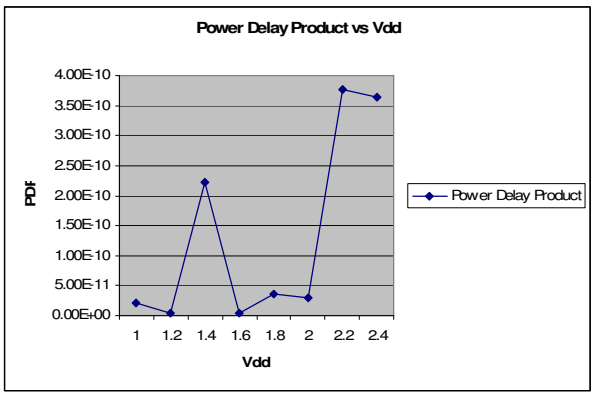

Fig.17 Power delay product of IPC2MOS inverter based interface at different values of Vdd

Although this circuit provides very good results at 180 nm TSMC technology but this circuit provides the worst results at 90nm technology. As it is prominent in Fig. 17 and 18 it shows very high power dissipation and energy loss per cycle. So, some modifications to this circuit have been done to achieve lower power dissipation. Fig. 19 reveals that As we are increasing the operating temperature power consumption is also increasing.

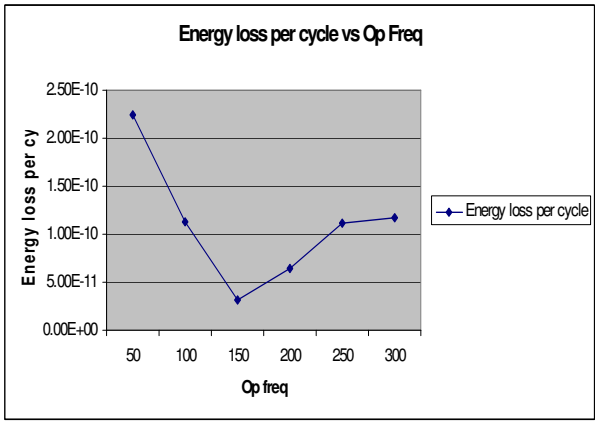

Fig.18 Energy loss per cycle at different operational frequencies

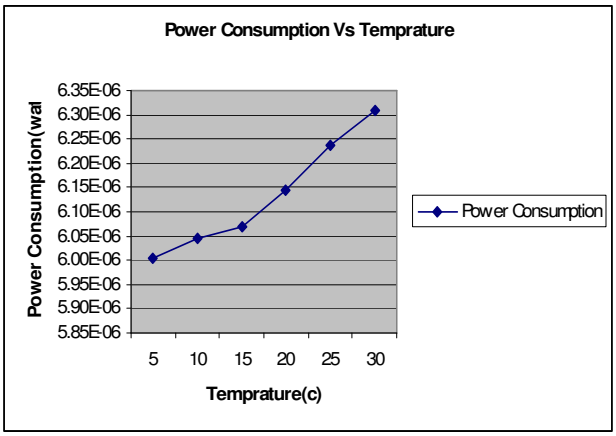

Fig. 19 Power Consumption Vs temperature for IPCCMOS based interface

In the proposed circuit some different clocking schemes are applied to the improved power clocked CMOS inverter reported in literature. This circuit does not show any short circuit current dissipation. The proposed design shows the best results at 90nm technology. A proposed IPC^{2}MOS interface is shown in Fig.20. Fig.21 shows the power delay product at different values of Vdd.

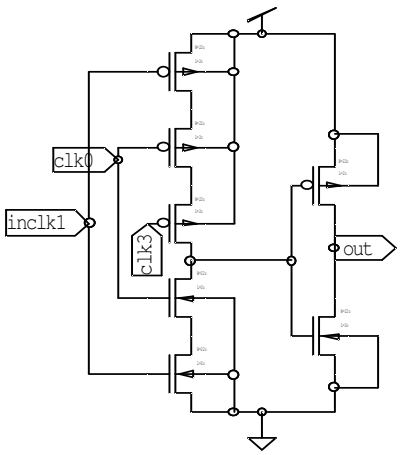

Fig 20 Proposed circuit for adiabatic-CMOS interface

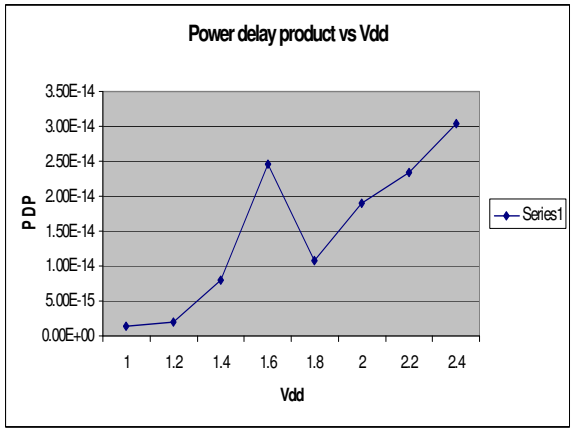

Fig.21 Power delay product of proposed interface at different values of Vdd

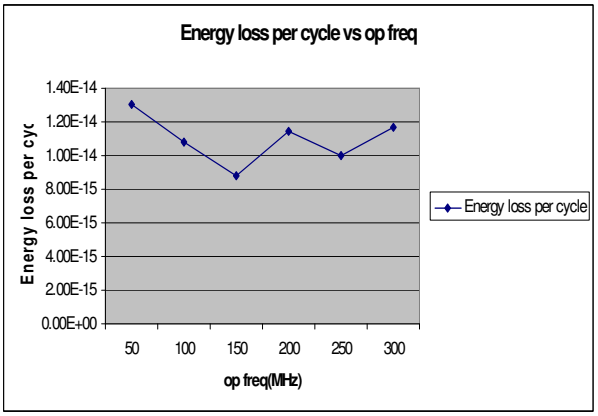

Fig.22 Energy loss per cycle vs. operational frequency

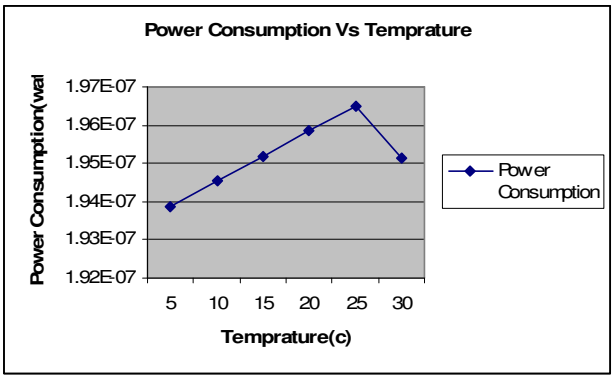

Fig. 23 Power Consumption Vs temperature for proposed interface

As it is depicting in the figure this proposed circuit shows the least power dissipation. Fig. 22 shows the energy loss per cycle over a wide range of frequencies. This circuit shows the least energy loss per cycle. Fig 23 shows the Power Consumption Vs Temperature for proposed interface.

3 CMOS -Adiabatic Interface Circuits

Numbers of CMOS-adiabatic interface circuits are shown in Figs. 24, 28 and 32. The first CMOS-adiabatic interface consists of a signal converter, a CMOS edge-triggered flop-flop, and the two CMOS inverters. The signal converter converts the signals (*in*clk0 and *inb*clk0) to the adiabatic signals (*out* and *outb*).

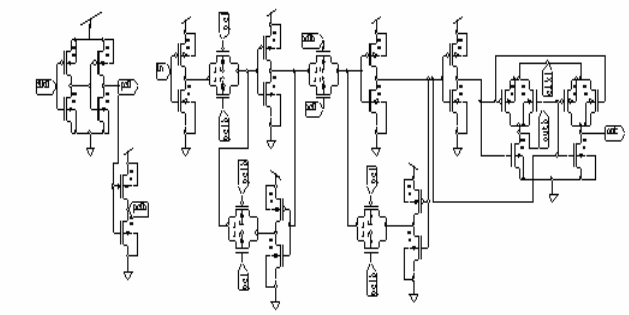

Fig. 24 CMOS-adiabatic interface based on static flip-flop and comparator using two CMOS inverters.

In order to avoid the deformation of the adiabatic signals, the input signals (*in*clk0 and *inb*clk0) of the converter should been only switched during wait states, thus a flip-flop is used to synchronize. The rectangle-wave clock (*pc*0) is generated by using the CMOS inverter comparing *clk*0 with *V*DD/2. Thus, the outputs of the flip-flop

are only switched during wait states to make the inputs of the converter to have the proper phase. This circuit has been simulated at 90 nm technology. Power delay product at various values of Vdd is shown in Fig. 25.

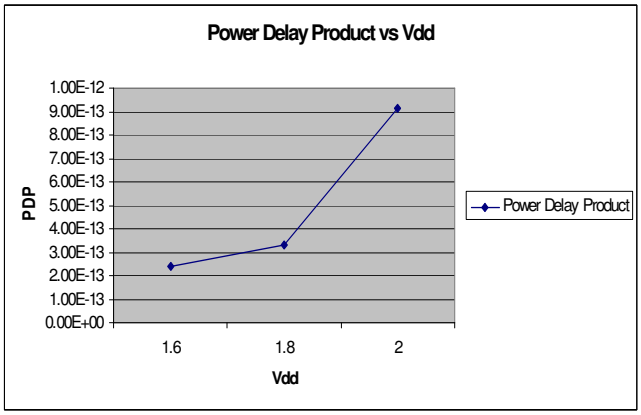

Fig. 25 Power delay product of CMOS-Adiabatic interface at different values of Vdd

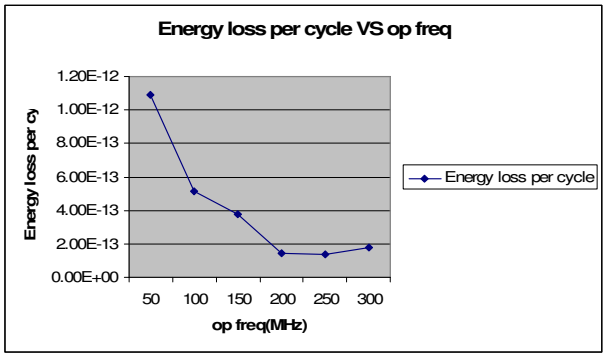

Fig.26 Energy loss per cycle vs. operational frequency

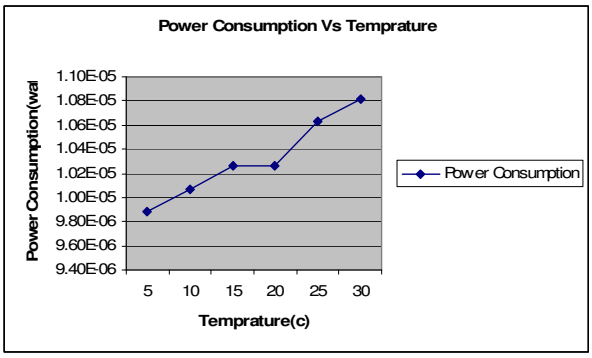

Fig. 27 Power Consumption Vs temperature for CMOS inverter based CMOS-Adiabatic interface

Energy loss per cycle over a wide range of frequencies is shown in Fig.26. This circuit as compared to other interfaces depicts comparatively more energy loss. Fig 27 shows the power consumption at various values of temperature. Power consumption for this circuit increases as the temperature increases. This circuit shows comparatively higher power dissipation compared to other CMOS-Adiabatic interfaces.

One source of energy loss occurs from the comparator's large short-circuiting dissipation. The interface based on Power clocked CMOS inverter is shown in fig.28. The rectangle-wave clock is generated using the PC^{2}MOS is to reduce short-circuit current. The signal converter uses the buffer to reduce the input capacitances of the signal converter.

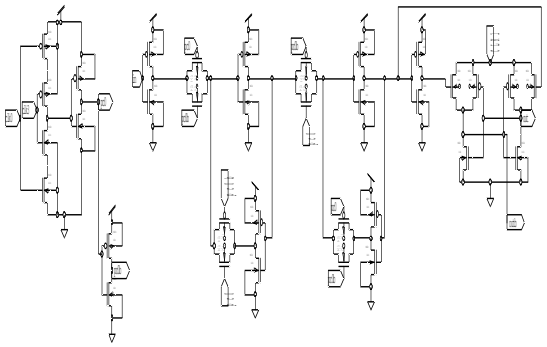

Fig. 28 CMOS-adiabatic interface based on static flip-flop and comparator using power-clocked CMOS (PC2MOS)

The simulations reveal that this circuit also shows a large power saving over a wide range of frequencies at 90nm technology as shown in Fig.30. Fig. 31 shows that the power consumption for this circuit is inversely proportional to temperature.

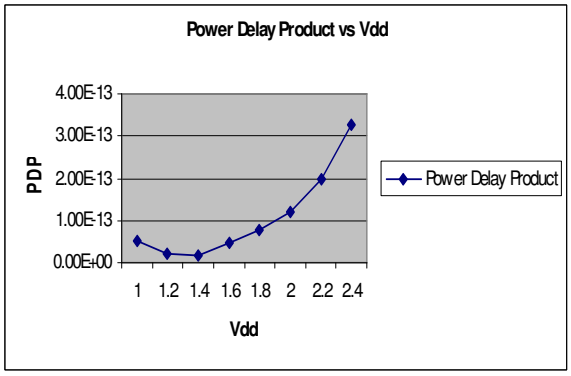

Fig.29 Power delay product of CMOS- Adiabatic Interface at different values of Vdd

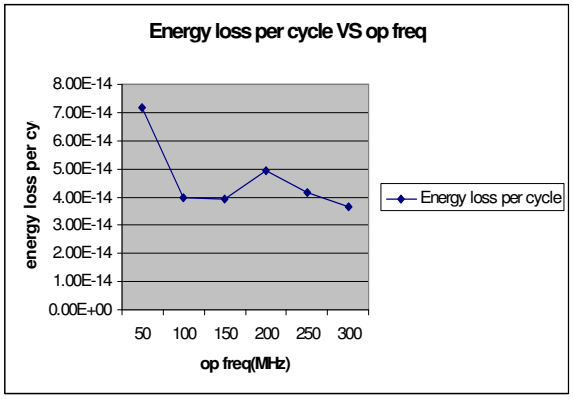

Fig. 30 Energy loss per cycle vs. operational frequency

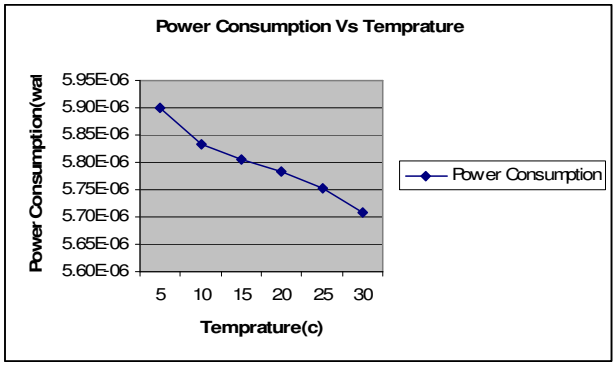

Fig. 31 Power Consumption Vs temperature for CMOS inverter based CMOS-Adiabatic interface

The CMOS flip-flop used in the CMOS-adiabatic interfaces has large energy loss compared with adiabatic circuits, because it doesn't operate in an adiabatic manner.

A power-clocked flip-flop (PCFF) to reduce its energy loss is shown in Fig 32. The interface consists of a FPAL buffer that converts CMOS signal to adiabatic one, and a PCFF that is used to synchronize. The structure and operation of PCFF are similar to CMOS transmission-gate flip-flops with a master-slave configuration except that it uses 4-transisor transmission gates that are driven by power-clocks instead of rectangle wave clocks. Energy loss per cycle over a wide range of frequencies for the above interface is shown in Fig.34. Because the above interface doesn't need the comparator and the energy of its clock input capacitances can be well recovered, lower energy dissipation can be expected and this circuit shows large power saving at 90 nm technology.

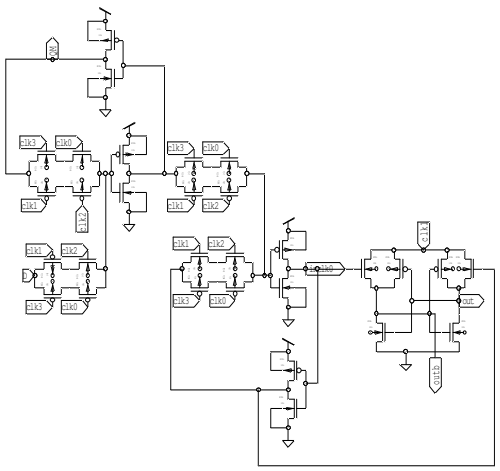

Fig.32 CMOS-adiabatic interface based on power-clocked flip-flop

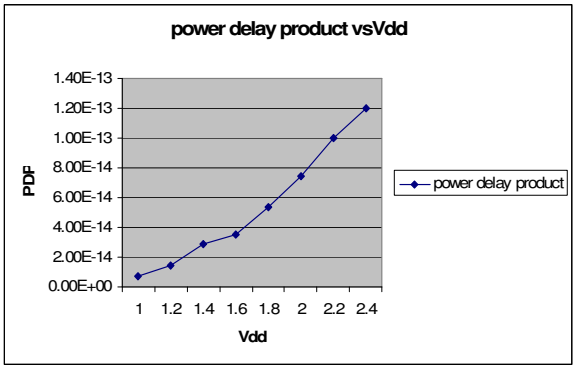

Fig 33Power delay product of CMOS-adiabatic interface at different values of Vdd.

Fig. 35 Shows Power Consumption Vs temperature for Power clocked flips flop based CMOS-Adiabatic interface.

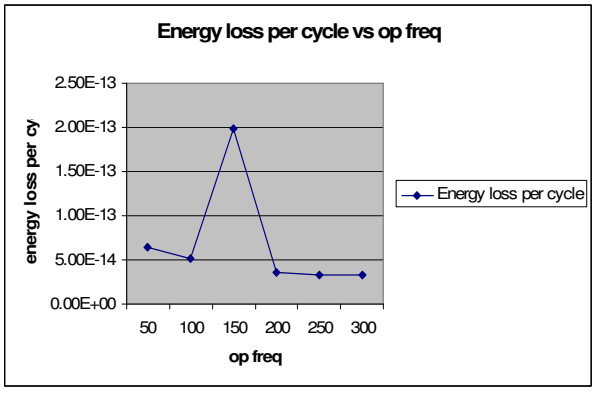

Fig.34. Energy loss per cycle vs. operational frequency

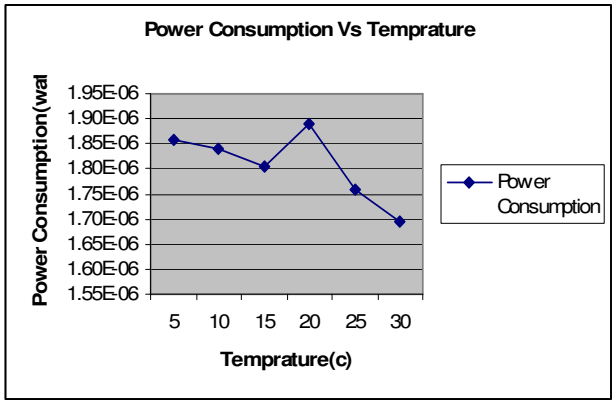

Fig. 35 Power Consumption Vs temperature for PCFF based CMOS-Adiabatic interface

4 Comparisons of Energy Dissipations

In terms of types of converted output signals, the adiabatic-CMOS interfaces can be classified into two types..

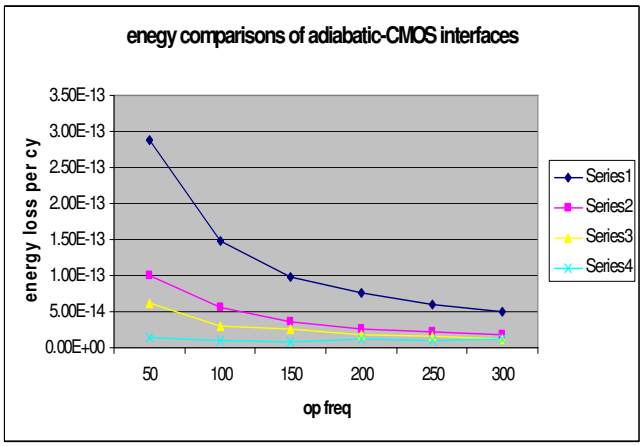

Fig.36 Energy dissipation comparisons of various adiabatic-CMOS interfaces

Series1-Schmitt inverter based interface
Series2-CMOS inverter based interface
Series 3-power clocked CMOS inverter based interface
Series 4-Proposed Interface at 90 nm technology

First type of interfaces can obtain a standard static CMOS output (Fig. 1, Fig.16, and Fig.20), while another type of interfaces only obtains a clocked CMOS output (Fig. 4, Fig. 8, Fig. 12). For the interfaces with static CMOS outputs, the proposed IPC^{2}MOS adiabatic-CMOS interface attains energy savings from 50 to 300MHz, as compared to implementation using a C^{2}MOS flip-flop. For the interfaces with a clocked CMOS output, the PC^{2}MOS adiabatic-CMOS interface attains energy savings as compared to the other two implementations over a range of frequencies, respectively. Among the three CMOS adiabatic interfaces, the circuit of Fig. 32 has low energy dissipation. The interface based on the power-clocked flip-flop attains energy savings clock rates ranging from 50 to 300MHZ

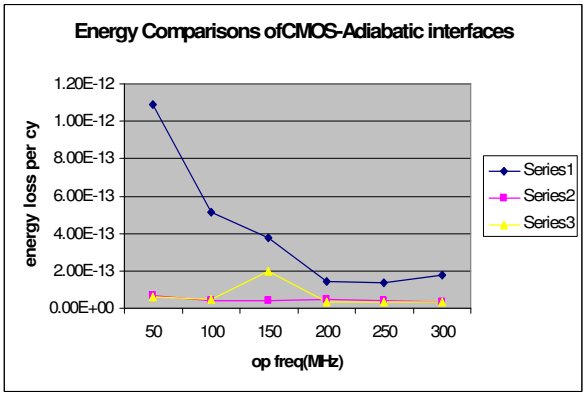

Fig. 37 Energy dissipation comparisons of various CMOS -adiabatic interfaces

Series1- CMOS-adiabatic interface based on static flip-flop and comparator using two CMOS inverters.
Series 2- CMOS-adiabatic interface based on static flip-flop and comparator using power-clocked CMOS (PC2MOS).
Series 3- CMOS-adiabatic interface based on power-clocked flip-flop.

5 Power delay Product Comparisons

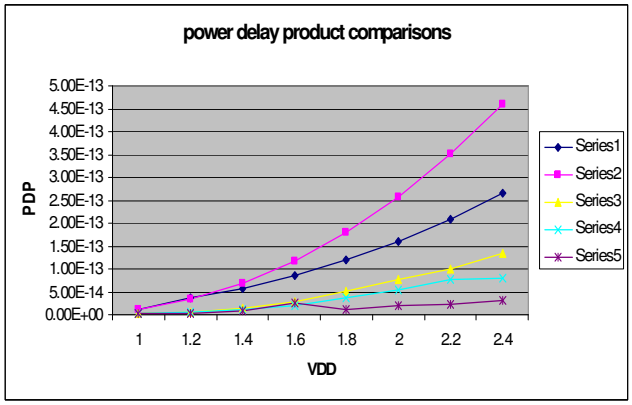

Fig. 38 Power Delay Product comparisons of adiabatic-CMOS interfaces

Series1-Peak sampling based interface
Series2-Schimitt inverter based interface
Series3-CMOS inverter based interface
Series4-Power clocked CMOS inverter based interface
Series5-Proposed interface at 90nm technology

It is evident from fig. 38 that the power delay product of proposed circuit is least among all the Adiabatic-CMOS Interfaces. Fig. 39 shows that the power delay product of interface circuit based on power clocked flip flop produces the best results among all the CMOS-Adiabatic interfaces.

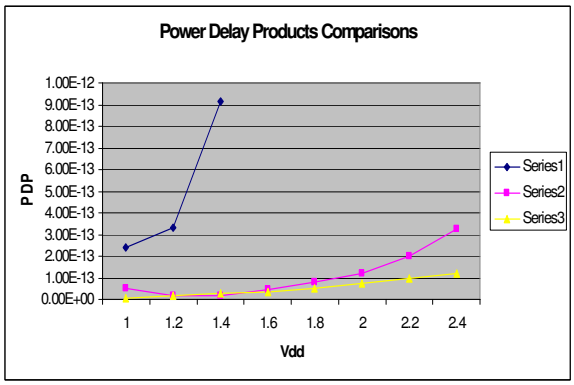

Fig. 39 Power Delay Product comparisons of adiabatic-CMOS interfaces

Series1- CMOS-adiabatic interface based on static flip-flop and comparator using two CMOS inverters.
Series 2- CMOS-adiabatic interface based on static flip-flop and comparator using power-clocked CMOS (PC2MOS).
Series 3- CMOS-adiabatic interface based on power-clocked flip-flop.

6 Power Consumption for interfaces at Various values of Temperature

Fig. 40 shows the comparison of power dissipation at various values of temperature for peak sampling based interface, Schmitt comparator based interface and Improved power clocked CMOS based interface. Among all the three Adiabatic-CMOS interfaces the peak sampling based interface shows the least power consumption.

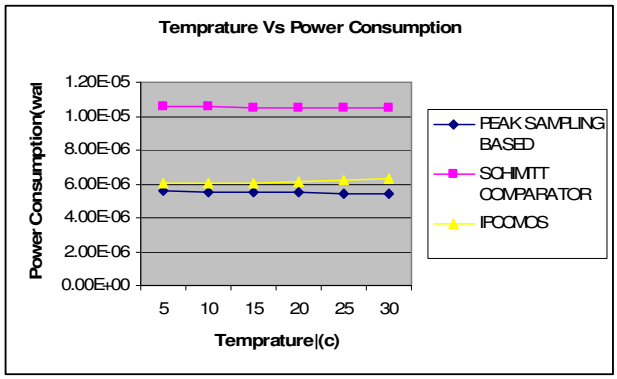

Fig.40 Temperature Vs Power Consumption

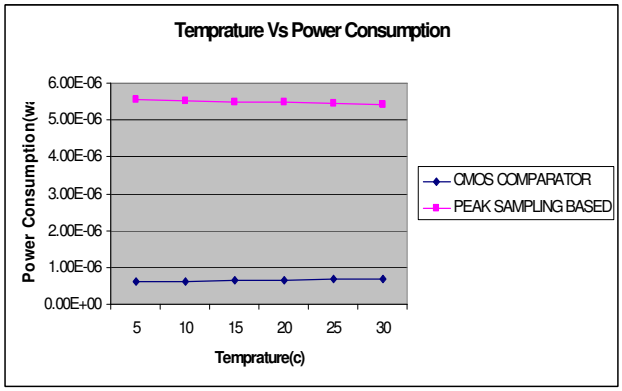

Fig.41 Temperature Vs Power Consumption

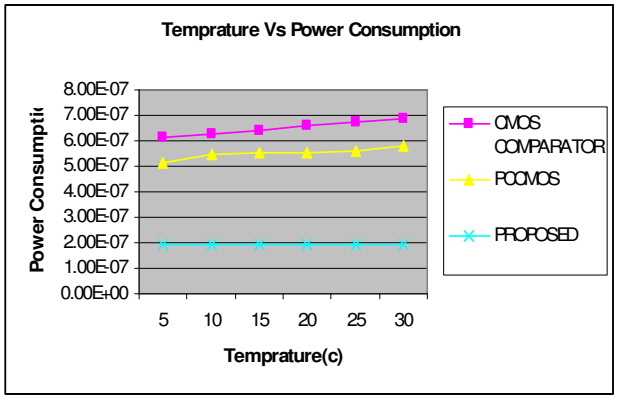

Fig.42 Temperature Vs Power Consumption

Fig. 41 shows the comparison of CMOS comparator based interface and peak sampling based interface. As it is evident from figure that CMOS comparator consumes negligibly small power in comparison with peak sampling based interface. Fig.42 shows the comparison of proposed circuit with CMOS comparator based interface and Power clocked CMOS based interface. The proposed circuit shows

the remarkable power saving over a wide range of temperatures. The proposed circuit shows the best results among all the Adiabatic-CMOS interfaces.

Fig. 43 shows the power dissipation comparison of various CMOS-Adiabatic interfaces. CMOS-adiabatic interface based on power-clocked flip-flop shows the best results among all the other interface circuits.

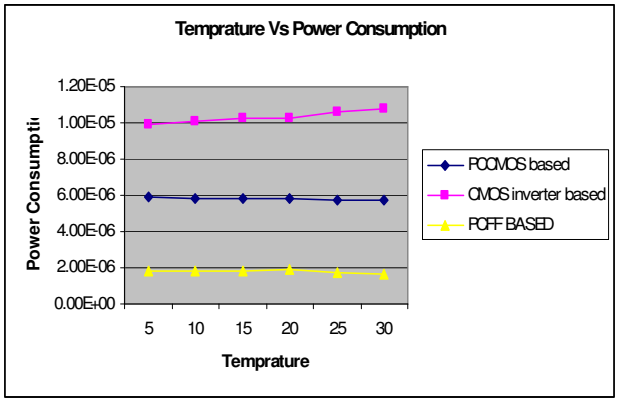

Fig.43 Temperature Vs Power Consumption

7 Conclusion

Integrated circuits can be designed with both adiabatic and conventional CMOS logic on the same chip. There were different types of interface circuits available in the literature. Power-clocked CMOS (PC^2MOS) comparator shows relatively large power savings over a wide range of frequencies, for clocked CMOS output. Proposed Improved Power-clocked CMOS (IPC^2MOS) comparator with different clocking schemes shows relatively large power savings over a wide range of frequencies, for static CMOS output. CMOS-adiabatic interface based on power-clocked flip-flop and CMOS-adiabatic interface based on static flip-flop and comparator using power-clocked CMOS (PC2MOS) shows the best performance among the all other reported circuits in terms of energy dissipation over a wide range of frequencies. The proposed adiabatic-CMOS interface shows the least power consumption over the wide range of operating temperatures. The CMOS-Adiabatic interface based on Power clocked Flip Flop shows the large power saving over the wide range of temperatures. They are more suitable for low power embedding systems, where both adiabatic logic and standard CMOS circuits are co-existed on a single chip to attain ultra low-power design. These all interface circuits are simulated at BSIM3V3 90 nm technology in tanner EDA tool.

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