Efficient Interconnect Design with Novel Repeater Insertion for Low Power Applications

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Abstract: Length of interconnect and number of repeaters are increasing with the advancement in VLSI Technology. Requirement of repeaters is increasing as the length of interconnect is increasing. The power delay product and frequency of operation plays significant role in designing of repeater. Performance of earlier conventional repeater with the proposed sub-threshold grounded body (STGB) bias repeater for various lengths of interconnects is analyzed. The simulation results shown in the paper indicates that the STGB bias repeater circuit operates in medium frequency range with better power-delay product as compared with the previous repeater. The temperature sustainability and performance with the variation of aspect ratio is also better for STGB bias repeater. Reduction of overall delay, power dissipation as well as operation of the repeater at higher frequencies can lead to the better performance of the VLSI chip in sub-threshold region.

Key words: VLSI, Interconnect, Sub-threshold, Repeater, Buffer, novel approach, conventional buffer, portable applications.

1. Introduction

In VLSI design, power and delay are the figure of merit during the selection and implementation of a device in chip fabrication. With the advancement in VLSI technology, the transistor count per chip is rapidly growing. Due to the rise in transistor count, routing complexity of interconnect is increasing, which is increasing the length of interconnect. More the length of interconnect; more the numbers of repeaters are required. The designing of repeaters thus becomes significant in the VLSI chip design. The requirements in the designing of the chip are lower delay, low power consumption and ability to operate at higher frequency ranges. The repeater should be able to dissipate less power as well as introduce less delay for better performance of a chip. Repeater should be also able to operate at higher frequencies.

RLC line method is proposed by Ismail and Friedman [1] in repeater insertion process and showed that on-chip inductance could decrease the delay, area, and power of the repeater insertion process as compared to an RC line model. Increasing complexity of interconnects leads to increased length of interconnects. The long interconnections lead to prohibitively high propagation delays. Buffers are required to drive high capacitive loads in order to keep pace with the required speed. Single buffer is not sufficient, hence number of buffers are required to be inserted at regular intervals of distance in interconnect for the proper detection and reconstruction of the signal, which are termed as repeaters [2]. In the medium performance, medium power consumption designs numerous optimization efforts have been made [3]-[5].Well known methods include voltage scaling [6], [7], switching activity reduction [8], [9], and logic optimization [10], [11]. However, these methods are not sufficient in many applications such as portable computing gadgets, medical electronics etc., where ultra-low power consumption with medium frequency of operation is the primary requirement.

Over the past decade, considerable research is devoted to the development of energy-efficient VLSI circuit and systems for portable systems. To achieve portability, the system must have a miniaturized power supply. A portable system must be designed for low power consumption. An effective way to reduce power consumption is

supply voltage scaling. However, threshold voltage cannot be scaled down with the same rate. Thus for low power applications, sub-threshold operation is a better option. Low power systems are slower ones, because of trade-off between power and speed. Thus the repeater circuit operating in sub-threshold region at medium frequencies is a better option. The sub-threshold logic operates with the power supply V_{dd} less than the threshold voltage V_{th} of the transistor. In this paper the Sub-threshold grounded-body biasing technique is proposed, having both NMOS and PMOS bodies grounded and simulation and calculation ensures the better performance than the conventional repeater. In this paper emphasis is on the lower delay and ability to operate at higher frequencies without compromising with the power dissipation in sub-threshold region. The STGB bias design of the repeater works at higher frequencies and having lower delay, which in turn reduces power-delay product.

2. Design of the Repeater

The conventional repeater is used as a repeater circuit, after every fixed length of interconnect, to reproduce the original signal. In earlier Interconnect designs, conventional repeater is used and in this paper the performance of it is compared with the STGB bias repeater.

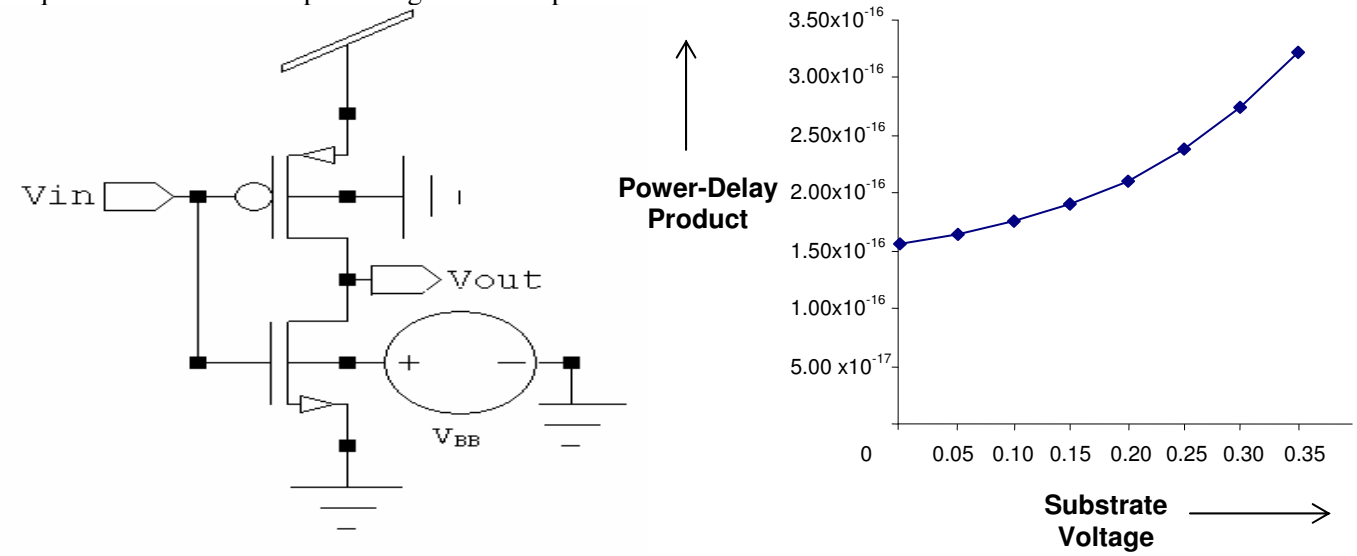

Fig. 1(a) Schematic of inverter with PMOS body at ground, 1(b) variation of power-delay product with NMOS substrate voltage keeping PMOS body at ground.

V_{BB}	Delay	Power	PDP
0.00	5.41×10^{-7}	2.76×10^{-10}	1.49×10^{-16}
0.05	5.42×10^{-7}	2.84×10^{-10}	1.54×10^{-16}
0.10	5.42×10^{-7}	2.74×10^{-10}	1.49×10^{-16}
0.15	5.43×10^{-7}	3.05×10^{-10}	1.66×10^{-16}
0.20	5.43×10^{-7}	3.40×10^{-10}	2.04×10^{-16}
0.25	5.44×10^{-7}	3.75×10^{-10}	2.04×10^{-16}
0.30	5.45×10^{-7}	4.45×10^{-10}	2.42×10^{-16}
0.35	5.46×10^{-7}	5.33×10^{-10}	2.91×10^{-16}
0.37	5.47×10^{-7}	5.76×10^{-10}	3.15×10^{-16}

Table 1. Delay, power and power-delay product variation with NMOS body bias V_{BB}.

The effect of varying the NMOS body bias voltage V_{BB} on delay, Power and Power-delay product keeping the body of PMOS at ground can be shown figure 1. The supply and input voltages are fixed at 0.37V and frequency of the applied signal is 1 KHz. figure 1(a) shows the schematic diagram of the buffer. The body bias voltage of NMOS is varied, and figure 1(b) shows the variation of power delay product with V_{BB}. The delay is found almost constant but the average power dissipation is increasing with the increase of V_{BB}. Table 1 shows the Power delay product for varying the NMOS body bias keeping the PMOS body at V_{DD}, which indicates as the NMOS body bias is increased, the power-delay product also increases. Thus choosing the repeater having both NMOS and PMOS bodies

at ground will give better power delay product. Keeping this thing in mind the STGB bias repeater is proposed, in which NMOS and PMOS bodies are connected to ground.

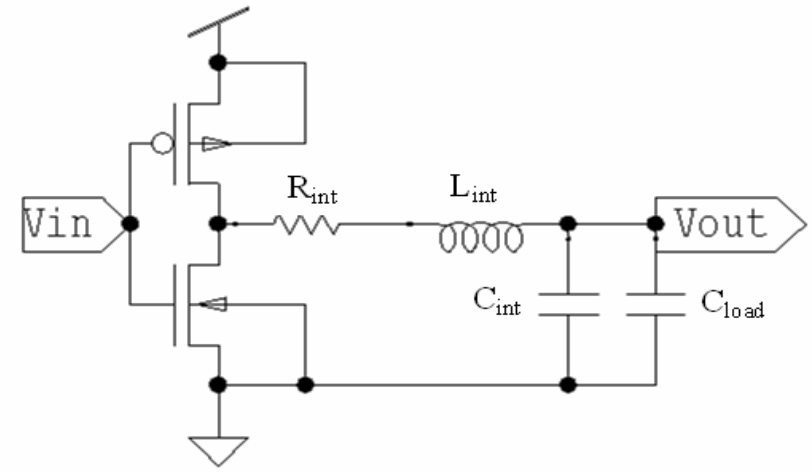

Fig. 2 Conventional repeater circuit with interconnect.

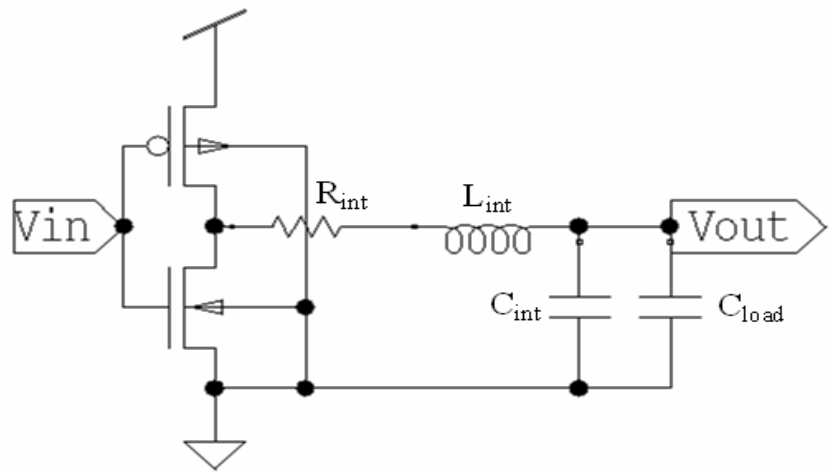

Fig. 3 STGB bias repeater circuit with interconnect.

Figure 2 shows the conventional repeater with interconnect and output load capacitor. In the conventional repeater, the substrate bias voltage is zero for both the NMOS and PMOS. Figure 3 shows the grounded body bias repeater with interconnect having capacitive load. In the STGB bias repeater substrate bias voltage for the NMOS is set to zero but for the PMOS it is not at zero value, thus the threshold voltage of the PMOS changes with applied voltage, while in case of the conventional repeater threshold voltage of PMOS and NMOS are not depending upon the change of the applied input voltage. Because of this change in threshold voltage of the repeater in STGB techniques, the frequency range of operation is increased, which produces a various advantages over the conventional repeater.

3. Simulation and Analysis

The repeater circuits, conventional repeater and STGB bias repeater, are simulated by taking various lengths of interconnects in 180nm technology. During simulation, the input voltage and the power

supply voltage $V_{dd,}$ both are kept below V_{dd} so that the device always operates in sub-threshold region. R_{in}, C_{in}, and L_{in} are the resistance, capacitance and inductance parameters of the interconnect line chosen according to the technology. The output or load capacitance is chosen to be 50fF.

The formula used for calculating the parameters of interconnect are as follows -

$$R_{\text{int}} = \frac{\rho.l}{W_{\text{int}}.T} \tag{1}$$

$$C_{\text{int}} = (\varepsilon_{ox}.l).[(\frac{W_{\text{int}}}{H}) + C_1 + C_2] \tag{2}$$

Where,

$$C_1 = 2.22(\frac{S}{S+0.7H})^{3.19} \tag{2.1}$$

and

$$C_2 = 1.17(\frac{S}{S+1.51H})^{0.76} \times (\frac{T}{T+4.53H})^{0.12}] \tag{2.2}$$

and,

$$L_{\text{int}} = (\frac{\mu_0.l}{2\pi})[\ln(\frac{2l}{W_{\text{int}}+T}) + 0.5 + 0.22(\frac{W_{\text{int}}+T}{l})] \tag{3}$$

Where,

l = Length of the interconnect
ρ = Resistivity
T = Thickness of interconnect
W_{int} = Width of interconnect
H = Height of metal layer from the substrate
S = Spacing between the signal and ground line

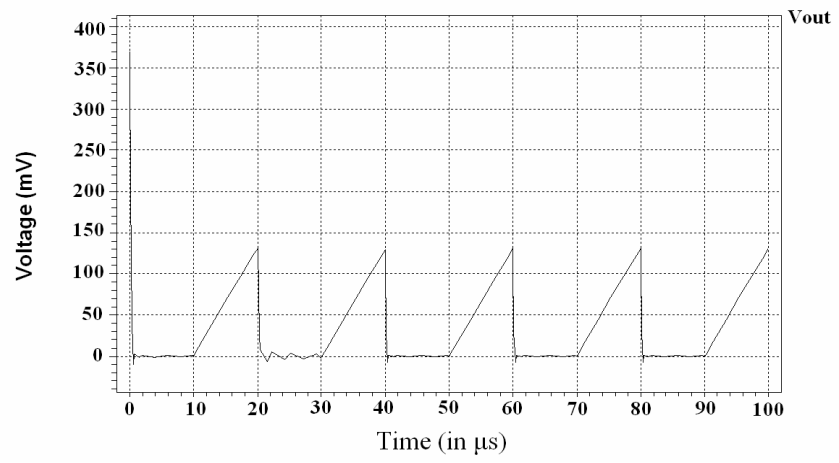

Fig. 4 Conventional repeater output for 10mm interconnect at 50 KHz.

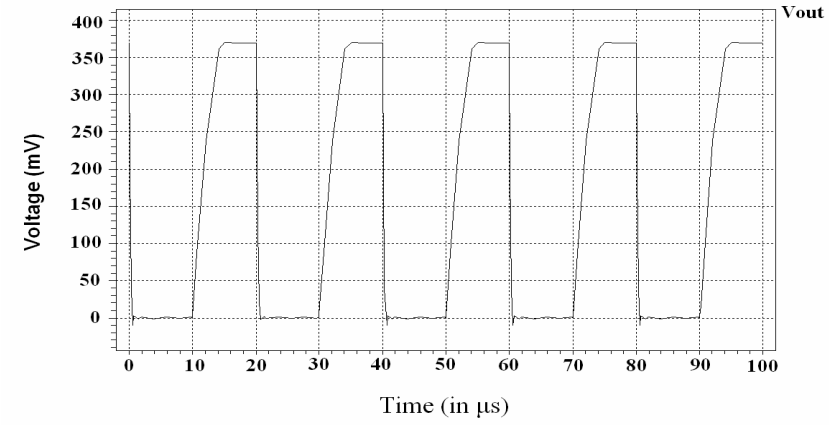

Fig. 5 STGB bias repeater output for 10mm interconnects at 50 KHz.

frequency (KHz)	Delay (in μs)					
	Conventional Repeater			STGB bias Repeater		
	10mm	5mm	1mm	10mm	5mm	1mm
0.5	1014	1008	1002	1002	1001	1000
1	514.3	507.6	502.2	501.5	500.8	500.2
2	264.3	257.6	252.2	251.5	250.8	250.2
5	114.3	107.6	102.2	101.5	100.8	100.2
1	64.3	57.6	52.2	51.5	50.8	50.2
20	39.2	32.6	27.2	26.5	25.8	25.2
50	N/A	17.6	12.2	1.15	10.8	10.22
100	N/A	N/A	7.2	6.47	5.79	5.22
200	N/A	N/A	4.7	3.98	3.29	2.72

Table 2. Delay in conventional and STGB bias repeater at various frequencies for various interconnect lengths.

Figure 4 and 5 shows the conventional and STGB bias repeater output for 10mm interconnect at 50 KHz. From the figures it can be well understood that the performance of the STGB bias repeater is better than that of the conventional repeater for medium frequency operation. Simulation results reveal that the STGB bias repeater even shows good performance in medium frequency range.

Table-2 shows 50% delay produced in conventional repeater and STGB bias repeater circuit for various lengths of interconnect at various frequencies. Delay produced by the conventional repeater for 10mm interconnect at 50 KHz, 100 KHz and 200 KHz and for 5mm interconnects at 100 KHz and 200 KHz is not calculated as the repeater output is below the 50% reference level. From the table it is clear that the delay produced by the STGB bias repeater is less than the conventional repeater for 10mm interconnect. For 5mm and 1mm interconnect also the delay produced by the STGB bias repeater is less than that of conventional repeater in the frequency range of 0.5 – 200 KHz. It is also found that the delay is very less affected by the increase of the length of interconnect in STGB bias repeater.

Figure 6 shows the average power dissipation in STGB bias buffer for different lengths of interconnects at various frequencies at 180nm technology. The average power dissipation increases non-linearly but for 10mm interconnects; it increases rapidly with increasing frequency. This figure shows obvious results that the average power dissipation increases with increasing the length of interconnect. Now the comparison of the results of different parameters such as average power dissipation of LVSB and STGB bias buffer is taken up.

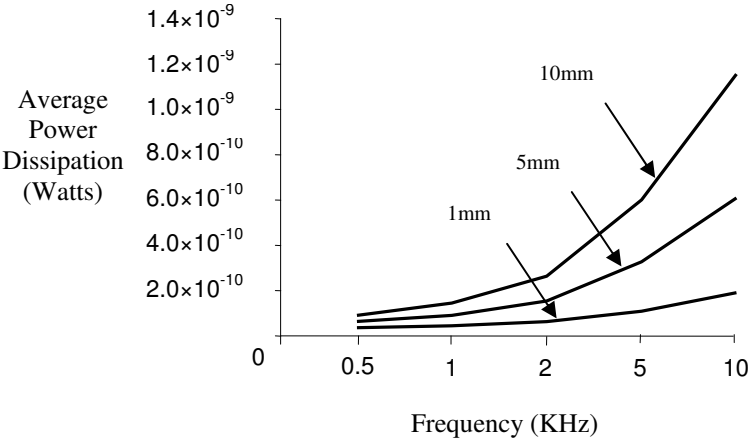

Fig. 6 Average power dissipation in STGB bias repeater for different lengths of interconnects at various frequencies.

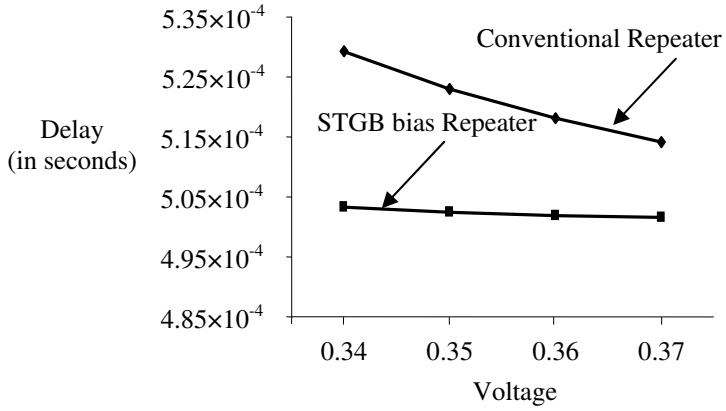

Fig. 7 Delays in conventional and STGB bias repeater at various voltages for 10mm interconnect at 1 KHz frequency.

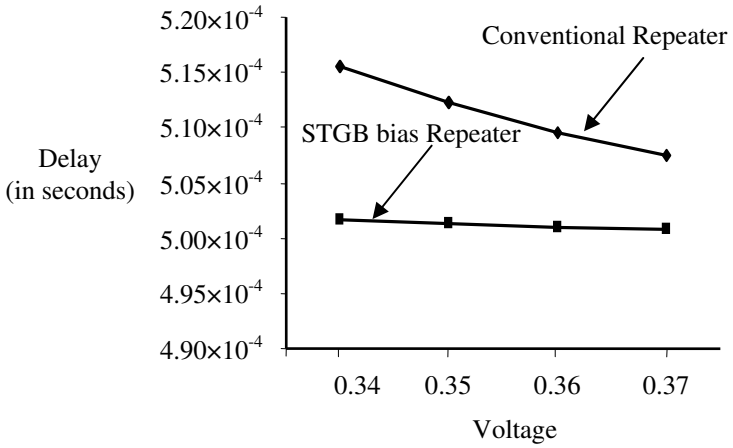

Fig. 8 Delays in conventional and STGB bias repeater at various voltages for 5mm interconnect at 1 KHz frequency.

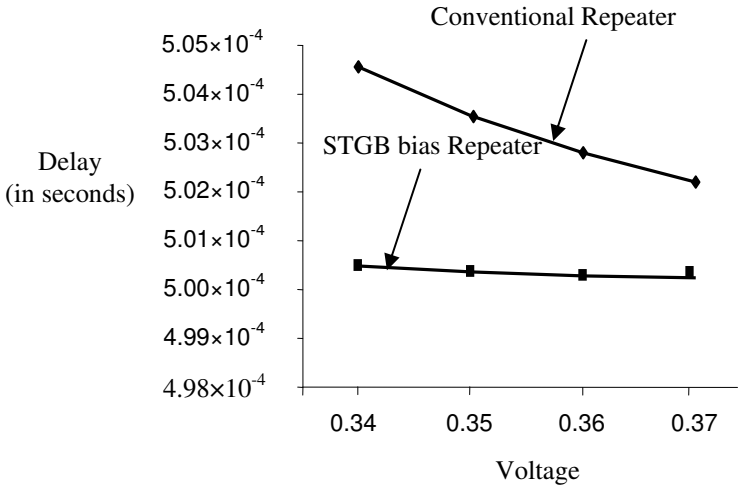

Fig. 9 Delays in conventional and STGB bias repeater at various voltages for 1mm interconnect at 1 KHz frequency.

Figure 7, 8 and 9 shows the delays produced in the STGB bias and conventional repeater at various supply voltages for three different lengths of interconnects, viz., 10mm, 5mm, and 1mm. These figures indicate that the delay produced by the STGB bias repeater at various voltages and for various lengths of interconnects are less than that of the conventional repeater. Also the effect of the voltage variation is less in STGB bias repeater, thus STGB bias repeater can be used at lower voltages in sub-threshold region, which in turn also decreases average power dissipation.

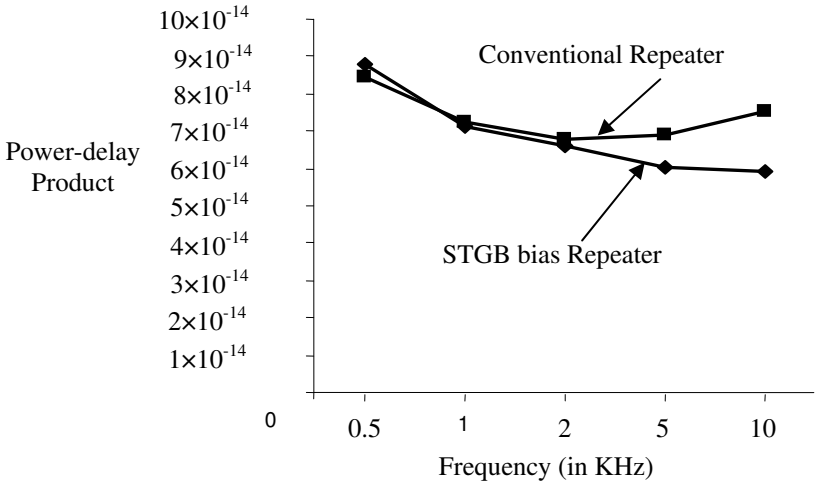

Fig. 10 Power-delay product in conventional and STGB bias repeater at various frequencies for 10mm interconnects.

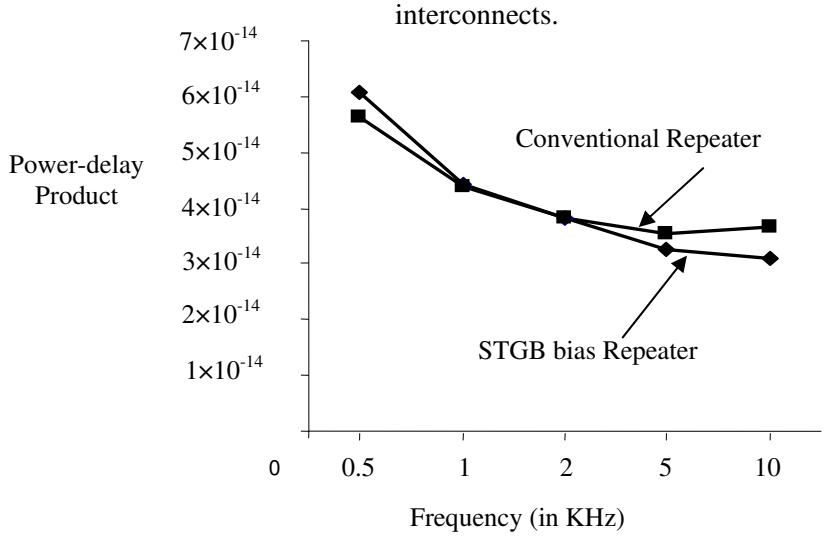

Fig. 11 Power-delay product in conventional and STGB bias repeater at various frequencies for 5mm interconnects.

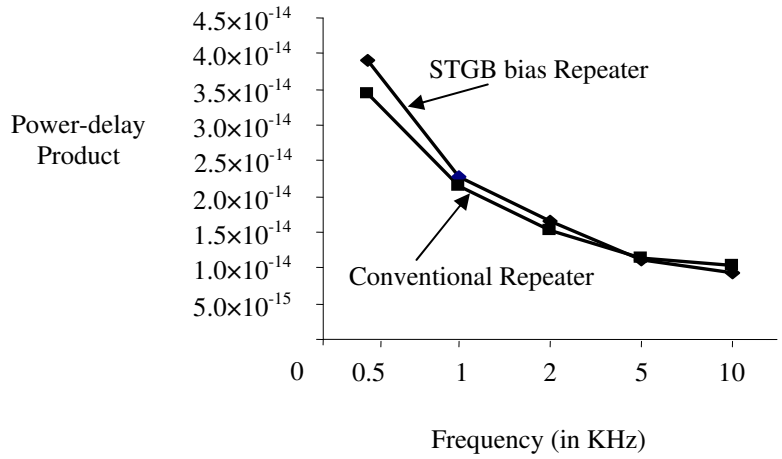

Fig. 12 Power-delay product in conventional and STGB bias repeater at various frequencies for 1mm interconnects.

Figure 10, 11 and 12 shows the power-delay product in the STGB bias and conventional repeater at various voltages for three different lengths of interconnects. From the figures it is clear that the power-delay product of the conventional repeater is better for low frequency operation but for high frequency operation power-delay product of the STGB bias repeater is better and power-delay product improves as the length of the interconnect increases. Also delay in conventional repeater is not calculated for high frequency so for the frequencies more than 5 KHz, STGB bias repeater is a better option to work as a repeater.

Aspect Ratio	Conventional Repeater		STGB bias Repeater	
	Power	Delay	Power	Delay
1	$1.176x10^{-9}$	$6.426x10^{-5}$	$1.154x10^{-9}$	$5.147x10^{-5}$
2	$1.160x10^{-9}$	$5.938x10^{-5}$	$1.120x10^{-9}$	$5.065x10^{-5}$
5	$1.158x10^{-9}$	$5.459x10^{-5}$	$1.090x10^{-9}$	$4.984x10^{-5}$
10	$1.155x10^{-9}$	$5.235x10^{-5}$	$1.042x10^{-9}$	$4.970x10^{-5}$
20	$1.151x10^{-9}$	$5.120x10^{-5}$	$1.133x10^{-9}$	$4.978x10^{-5}$

Table 3. Delay and Power in conventional and STGB bias repeater at various aspect ratios.

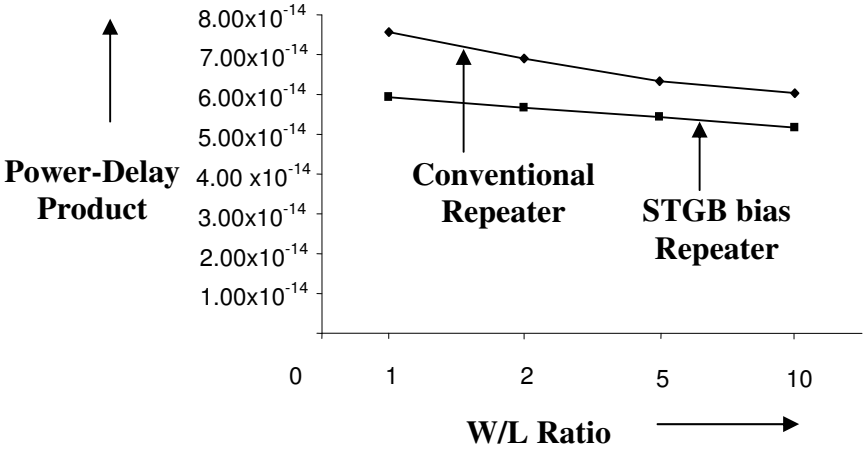

Fig. 13 Power-delay product in conventional and STGB bias repeater at various aspect ratios.

Table 3 shows the power and delay variation and Figure 13 shows the variation of power-delay product with aspect ratio of conventional and STGB bias repeater. The aspect ratio of NMOS and PMOS are changed and the effect is analyzed on delay and power. The delay and power values and thus power-delay product can be reduced by increasing the aspect ratio. But power-delay product of STGB bias repeater shows almost 21% better performance than the conventional one.

Temprature	Conventional Repeater		STGB bias Repeater	
	Power	Delay	Power	Delay
25	$1.18x10^{-9}$	$6.43x10^{-5}$	$1.15x10^{-9}$	$5.15x10^{-9}$
35	$1.18x10^{-9}$	$6.36x10^{-9}$	$1.16x10^{-9}$	$5.15x10^{-9}$
45	$1.19x10^{-9}$	$6.30x10^{-9}$	$1.17x10^{-9}$	$5.15x10^{-9}$
55	$1.20x10^{-9}$	$6.24x10^{-9}$	$1.18x10^{-9}$	$5.16x10^{-9}$
65	$1.21x10^{-9}$	$6.19x10^{-9}$	$1.20x10^{-9}$	$5.16x10^{-9}$
75	$1.22x10^{-9}$	$6.15x10^{-9}$	$1.21x10^{-9}$	$5.16x10^{-9}$

Table 4. Delay and Power in conventional and STGB bias repeater at various temperatures.

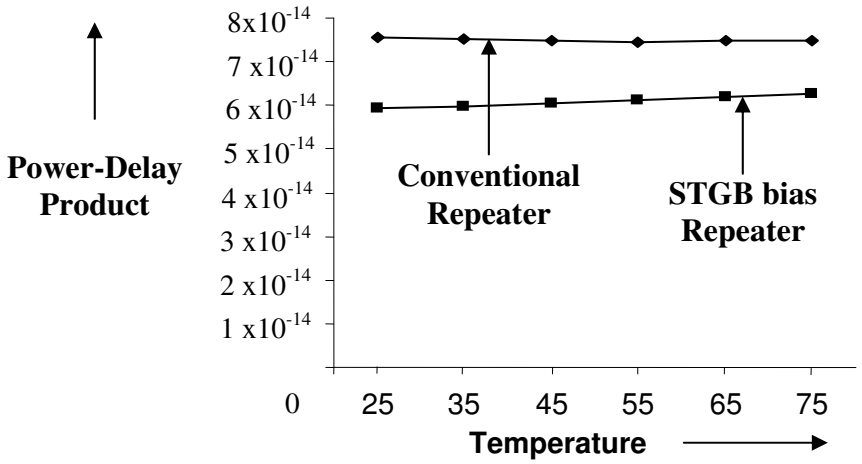

Fig. 14 Power-delay product in conventional and STGB bias repeater at various temperatures.

The power, delay and power-delay product of conventional and STGB bias repeater are analyzed by varying the temperature values. From the table-4 and figure-14, there is 20% improvement in the power delay product if the STGB bias repeater is used in place conventional repeater in interconnect design.

4. Conclusion

For low frequency operation conventional repeater is better in terms of average power dissipation. Since STGB bias buffer operates at higher frequencies speed of the STGB bias repeater is better. It is also found that delay is almost constant for various voltages, thus in sub-threshold region STGB bias repeater can operate at lower value of input and supply voltages and thus the power-delay product becomes is improved. The increase in the aspect ratio improves the performance of both the repeaters but power-delay product is less for STGB bias repeater. The temperature sustainability of the STGB bias repeater is also better than the STGB bias repeater. Thus in a nutshell STGB bias repeater is a better choice in sub-threshold region for low level and high frequency signals.

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