A Novel Design for Evaluating Simultaneous Switching Noise within an Enhanced IBIS Model

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Abstract: Simultaneous switching noise (SSN) is a major cause of power integrity (PI) degradation that causes circuits to become unstable and experience errors. As modern ICs operate at higher speeds with higher density and lower voltages, SSN has become a serious issue that must be addressed to ensure system stability during the short rise- and fall-times of the logic transient states. Most traditional designs have generally used decoupling capacitors to reduce SSN. As these capacitors become equivalent series inductances when the system operates at high frequencies, such a technique works against reducing SSN. Therefore, we propose a methodology called the enhanced IBIS model that effectively alleviates the problem of SSN using an evaluation based on the enhanced I/O buffer information specification (IBIS) model with decoupling capacitors and a high-frequency low-impendence circuit. In this study, we showed that SSN from 452 mV, 290 mV, 163 mV, and 301 mV, of IBIS, traditional decoupling capacitors, IBIS with a high-frequency low-impendence circuit, and HP Simulation Program with Integrated Circuit Emphasis (HSPICE) methodologies, respectively, was effectively reduced by 121 mV of our enhanced IBIS mode as measured by the peak-to-peak value. That is, our new method reduces noise by more than 73.2%, 58.3%, 25.7%, and 59.8% compared to other four methodologies, respectively.

Key Word: Simultaneous Switching Noise (SSN), Power Integrity (PI), I/O Buffer Information Specification (IBIS), HSPICE, High-frequency low-impedance (HFLI) circuit.

1. Introduction

Modern integrated circuits (ICs) contain several million transistor cells on a single die. Under high-speed, high-density, low-voltage conditions, ICs can make perfectly controlled timing changes within a single die. Simultaneous switching noise (SSN) is a major source of noise that affects system stability, and is much more significant than crosstalk, reflection-talk, and

electromagnetic interference (EMI) [2], [5], [20], [34], [35].

The system-on-a-chip (SoC) packaging technology uses a single wafer process to integrate many types of semiconductors, such as complementary metal-oxide semiconductors (CMOS), and passive resistance, inductance, and capacitive (RLC) components into a single IC die [3], [7], [21]. The system-in-package (SiP) technology combines many different wafer process dies on a single IC in two dimensions (horizontal) to connect two pins, or in three dimensions (vertical) to stack two chips [21]. Examples of this combination of IC technologies have been described elsewhere. Therefore, the development of new SiPs with smaller ICs means that ensuring PI and signal integrity (SI) will become increasingly complicated [4], [30]. SiP components are connected to power terminals by wire bonds, flip-chips, and vias so that systems can operate at high frequencies with short transient rise- and fall-times on the order of several picoseconds [7], [4]. Such complicated systems will cause packaging parasitism effects between the power and ground terminals, including stray and parasitic capacitance. As the power planes supply energy to each component through vias, SSN also influences the signal quality of the components.

Decoupling capacitors have generally been used in most traditional designs to reduce SSN in single IC chips [5], [11], [16], [31], [34]. These become equivalent series inductances (ESLs) when the system operates at high frequencies, as this method uses the capacitor characteristics of equivalent series resistance (ESR) and equivalent series inductance (ESL) to absorb SSN [2], [5]. As such behavior works against reducing SSN, decoupling capacitors cannot effectively suppress SSN, and thus simply take up space [13], [17], [34]. An alternative design for reducing SSN is to integrate noise reduction circuitry into the IC chip to provide high-quality PI.

The I/O Buffer Information Specification (IBIS) model was first developed by Intel, and has subsequently been widely adopted by other IC design companies [1]. This model is commonly used for describing and simulating the behavior of ICs [32]. The HP Simulation Program with Integrated Circuit Emphasis (HSPICE; Synopsis Inc.) model works at the transistor level to describe the schematic of an IC. IBIS falls short in describing PI in the transistor-level model as it does not consider SSN. Increasing attention has been focused on PI as ICs reach higher densities, and operate at higher speeds and lower voltages. One study examined ways to reduce SSN, which is the major source of noise that degrades PI [5], [6], [34], [35].

IC designers also often add decoupling capacitors to the HSPICE model to reduce SSN at the transistor level but this has limited effectiveness due to the ESL characteristics of the capacitors at high frequencies [28]. Therefore, we propose a methodology that effectively alleviates the problem of SSN using an enhanced IBIS model with decoupling capacitors and a high-frequency low-impendence circuit. Our earlier paper discussed the SSN issue [34]. Our proposed design can effectively reduce SSN in the minimum state and obtain better performance than traditional decoupling capacitors, IBIS with a high-frequency low-impendence circuit, HSPICE, and IBIS methodologies.

The remainder of this paper is organized as follows. The basic principles are described in Section II. Our proposed method is introduced in Section III and the simulation results are described in Section IV. Section V discusses the results of the tapered buffer design applications. Finally, our conclusions are presented in Section VI.

2. Basic concept

Four basic concepts, the IBIS structure, SSN, the characteristics of the decoupling capacitors, and the principles of SSN in IBIS, are discussed in this section.

2.1 Structure of the IBIS model

The IBIS model was first developed by Intel, and is now widely used by IC design companies [1], [28], [8]. Although IBIS does not describe the internal function of an IC, it can still produce faster and more precise simulation results than the HSPICE model. Moreover, it can also protect the intellectual property (IP) of IC design companies more effectively than other methods. IBIS operation is similar to the behavior of a circuit model showing the relationship between current and voltage (*I–V* curve), or between current and timing (*V–T* ramp). These two relationship curves are used in IBIS to represent the pin electrical characteristics for the inputs and outputs of digital ICs. Moreover, the inputs and outputs of a digital IC can be described using pure ASCII text, which was first used for this purpose in 1990, and then became standardized as ANSI/EIA-656 and IEC-62014-1 [1], [28].

The major purpose of IBIS is to provide the necessary information to simulate the circuit under consideration. This model can describe the electronic characteristics of IC pin definitions in detail. The necessary parameters are the *I–V* curves, *V–T* ramps, die equivalent capacitance, packaging equivalent resistance, packaging equivalent capacitance, and packaging equivalent inductance [8]. Moreover, using an IBIS with PI simulation systems involves three models: the driver terminal (output), receiver terminal (input), and the transmission line [26], [1]. Generally, a basic IBIS contains the following necessary information: four equivalent *I–V* curves ("*Pull_Up*," "*Pull_Down*," "*Power_Clamp*," and "*Gnd_Clamp*"), the die equivalent capacitance (C_{comp}), three packaging equivalent components (inductor L_{PKG}, resistance R_{PKG}, and capacitance C_{PKG}), an output packaging pad (*PKG_OUT*), and an input packaging pad (*PKG_IN*) as shown in Fig. 1(a) [29], [26], [32]. Let *Pull_Up*, *Pull_Down*, *Power_Clamp*, and *Gnd_Clamp* denote their equivalent circuit *I–V* curves. However, if a pin is in the input buffer model, it will not contain *Pull_up* and *Pull_down* as shown in Fig. 1(b). In IBIS, the *I–V* curve describes the impedance characteristics of the IC, and the *V–T* curve describes the voltage-to-time relationship in the voltage transition state from "H" (high state) to "L" (low state) or "L" to "H" [29], [26], [28].

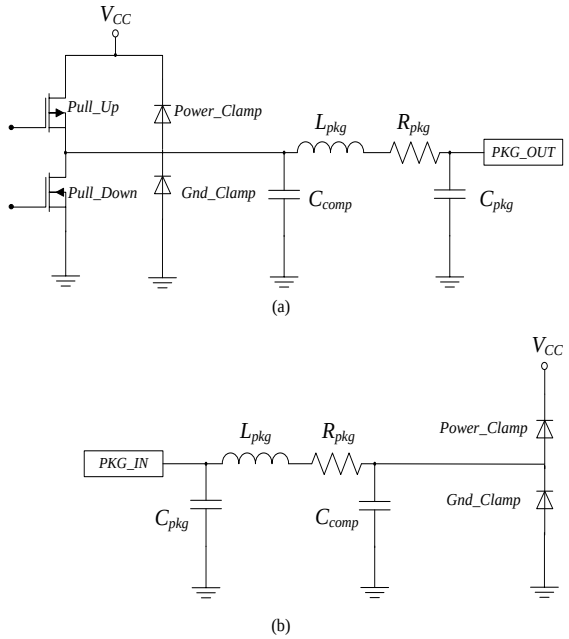

Fig. 1. (a) IBIS output buffer model. (b) IBIS input buffer model.

2.2 Simultaneous switching noise

An IC may have many I/O buffers and internal logic circuits. Modern ICs have clock frequencies of more than several GHz. Thus, the *H* to *L* or *L* to *H* transient states will last for at most several picoseconds [23], [22].

Moreover, since IC packaging has a side effect that is equivalent to a capacitor in parallel with an inductor, for operation at such high

frequencies, SSN is caused by the packaging parasitic effect between the die wire bonds and their pads. This causes the reference voltage of the power and ground terminals to bounce, making them unstable [25], [23]. The equivalent circuit of this packaging parasitism consists of a parallel inductor and capacitor (LC) in series with the power and ground terminals of IBIS as shown in Fig. 2. Components "C_{TDD} parallel to L_{TDD}" and "C_{TSS} parallel to L_{TSS}" are used to describe this LC effect called stray conductance and parasitic capacitance [27], [26].

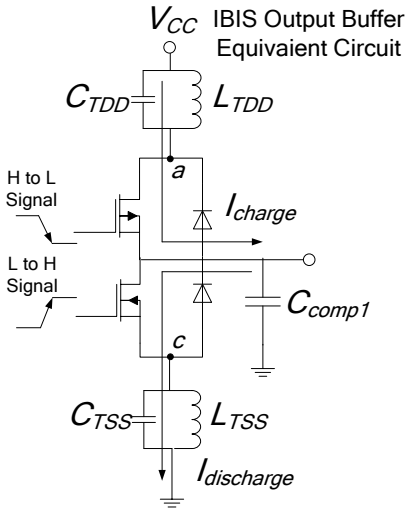

Fig. 2. Equivalent circuit in IBIS and the packaging parasitic circuit.

Buffers sink the current from the power terminal for a transient digital signal, and this current will pass through C_{TDD} and L_{TDD}. This charging current, I_{charge}, passes the equivalent IBIS P-channel metal oxide semiconductor (PMOS) component and then charges the output capacitor C_{comp1}. When the digital signal changes state, the transient discharge current, $I_{discharge}$, discharges to the ground terminal from the previously charged capacitor C_{comp1} through the equivalent IBIS N-channel metal oxide semiconductor (NMOS) component as well as C_{TSS} and L_{TSS} as shown in Fig. 2.

As the input signal of the active components or input/output buffers is in a transient state, these active components will sink current from the power terminal or discharge current to the ground terminal and induce SSN in the power and ground terminals, respectively [23]. When the IC signal is in several transient states simultaneously, the buffer will momentarily draw a large amount of current from the power source. This current passes through the inductor and induces a voltage drop across it, which causes a reference power/ground bounce between the power and ground terminals. Typical SSN between the power and ground terminals is shown in Figs. 3(a) and (b) [27], [26]. The maximum SSN swing, which is the difference between the global minimum and the global maximum in the waveform, is denoted by its peak-to-peak value, $\Delta V_{p\text{-}p}$ [20]. Therefore, this SSN is called the power or ground bounce [23], [9], [26], [33]. The amount of current in the double buffers working together in IBIS is more than that of the single one. In addition, when many IC signals are simultaneously in transient states, the SSN swing becomes more serious. As this increases the error rate of the output timing, the maximum noise swing must be limited to within 10% of its operational voltage by $\Delta V_{p\text{-}p}$ [2], [20], *i.e.*, the peak voltage difference between the global maximum and minimum.

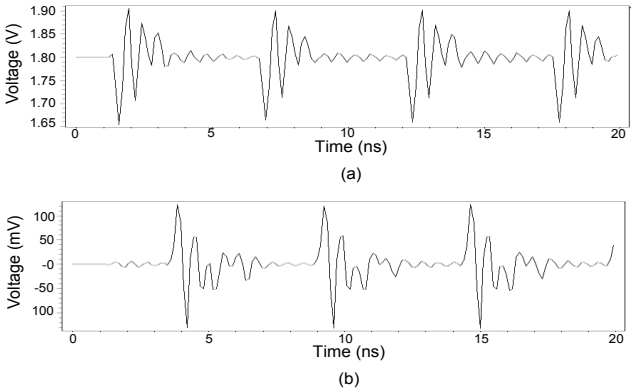

Fig. 3. (a) Typical SSN in the power plane. (b). Typical SSN in the ground plane.

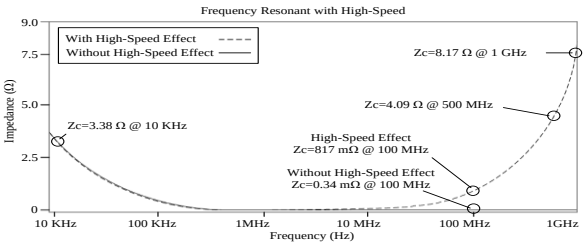

Fig. 4. Characteristics of decoupling capacitors for high frequencies.

2.3 Characteristics of decoupling capacitors

Decoupling capacitors are usually used on printed circuit boards (PCBs) or in IC packaging to reduce the SSN noise and maintain PI stability. The impedance *Zc* of the ideal capacitor is $1/(2\pi fc)$ Ω; this reactance is lower for higher frequencies. A pure capacitor maintains its capacitance characteristics for frequencies below the self-resonant frequency and exhibits inductor characteristics for frequencies greater than the self-resonant frequency [2]. For most electronic products, signal integrity effects begin to be important at clock frequencies above about 100 MHz, called the high-speed effect [2]. For example, in the case without high-speed effect, the lumped impedance values of a 4.7 μF capacitor are 3.38 Ω and 0.34 mΩ at 10 kHz and 100 MHz, respectively. Therefore, it is effectively a short circuit at 100 MHz as shown in Fig. 4

Hence, its capacitive reactance will increase for increasing frequencies during this inductance phase. Therefore, the impedance characteristics of decoupling capacitors change from capacitance behavior to inductance behavior according to the equation *Z-HFC* = *ESR* + *ESL* + $1/(2\pi fc)$ Ω [2], [28], where $f_{Z\text{-}HFC} = \frac{1}{2\pi\sqrt{LC}}$, and *Z-HFC* is the second-order equivalent capacity impendence. In the case with high-speed effect, the lumped impedance values of the same 4.7 μF capacitor are 3.38 Ω and 817 mΩ at 10 kHz and 100 MHz, respectively. Moreover, *Z-HFC* is 4.09 and 8.17 at 500 MHz and 1 GHz, respectively. Therefore, it will not be a short circuit at high frequencies as shown in Fig. 4.

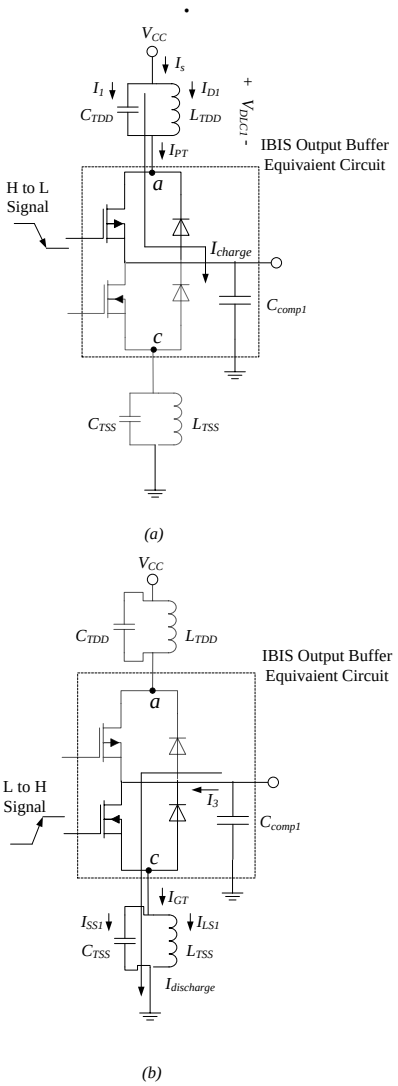

Fig. 5. Behavior of IBIS output buffer operations. (a). *L* to *H* operation. (b). *H* to *L* operation.

2.4 Principle of SSN in the IBIS model

We will use the input and output equivalent circuits of IBIS shown in Fig. 5 to explain different operations. Let capacitors C_{TDD} and C_{TSS} and inductors L_{TDD} and L_{TSS} be the packaging parasitic capacitance and stray

conductance between the power and ground terminals, respectively, [23], [26]. Here, we will first consider the working principle and ignore the packaging parasitism components, R_{pkg}, C_{pkg}, and L_{pkg}.

When the input signal changes from *H* to *L*, *Pull_Down* and *Pull_Up* are in the off and on states, respectively. Then, C_{comp1} is charged by I_{charge} through *Pull_Up* marked by the heavy solid line shown in Fig. 5. I_{D1} passes through the component L_{TDD}, and then L_{TDD} will induce the SSN V_{DLC1} in the power terminal as shown in Eq. (1). Moreover, the terminal voltage of C_{TDD} is parallel to L_{TDD}, and hence, its voltage is equal to V_{DLC1}. I_1 passes through C_{TDD} as shown in Eq. (2). According to node current laws, I_S is equal to the sum of I_1 and I_{D1} as shown in Eq. (3). In this study, let V_{PT} be SSN of node *a*, so $V_{PT} = Vcc - V_{DLC1}$. By substituting Eq. (1) into (2), Eq. (2) into (3), and Eq. (3) into V_{PT} above, then V_{PT} can be obtained as shown in Eq. (4). I_{PT} is the output current of node *a*, which according to Kirchhoff's law, is equal to I_s. Thus, V_{PT} is simply SSN of the power terminal.

$$V_{DLC1} = L_{TDD}\frac{dI_{D1}}{dt} \quad (1)$$

$$I_1 = C_{TDD}\frac{dV_{DLC1}}{dt} \quad (2)$$

$$I_{D1} = I_s - I_1 = I_s - C_{TDD}\frac{dV_{DLC1}}{dt} \quad (3)$$

$$\Delta V_{PT} = Vcc - L_{TDD}\frac{dI_{PT}}{dt} + L_{TDD}C_{TDD}\frac{d^2V_{DLC1}}{dt^2} \quad (4)$$

When the state of the input signal changes from *L* to *H*, *Pull_Down* and *Pull_Up* are in the on and off states, respectively. Then, the $I_{discharge}$ path of C_{comp1} is discharged to the ground terminal through *Pull_Down*. Hence, the stray conductance can induce SSN in the ground terminal. Therefore, the discharge current I_3 of C_{comp1} is equal to I_{PT}, and the discharged current $I_{GT} = I_3$ passes through node *c* as shown in Eqs. (5) and (6). The ground noise ΔV_{GT} is shown in Eq. (7), obtained in a similar manner to Eq. (4).

$$I_{SS1} = C_{TSS}\frac{dV_{C\_comp1}}{dt} \quad (5)$$

$$I_{LS1} = I_{GT} - I_{SS1} \quad (6)$$

$$\Delta V_{GT} = L_{TSS}\frac{dI_{LS1}}{dt} = L_{TSS}\frac{dI_{GT}}{dt} - L_{TSS}C_{TSS}\frac{d^2V_{C\_comp1}}{dt^2} \quad (7)$$

3. Proposed high-frequency low-impedance (HFLI) circuit

3.1 HFLI concept

As decoupling capacitors filter the noise in digital systems [10], they can be added between the power and ground terminals. However, at high frequencies, the capacitance characteristic of a capacitor will change to inductance and cannot effectively reduce SSN. We propose an HFLI equivalent circuit for use in IBIS. This circuit Z_V_{GB} consists of two resistors R_{p1} and R_{p2}, one inductor L_p, and one capacitor C_p, as shown in Fig. 6(a). Its major function is to reduce SSN of power and ground terminals effectively to decrease $\Delta V_{p\text{-}p}$ to a minimum.

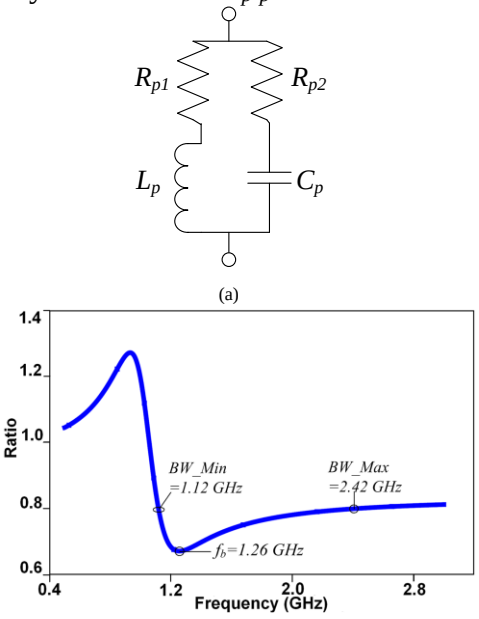

Fig. 6(a). Z_V_{GB} circuit. 6(b). Frequency response diagram of Z_V_{GB}.

3.2 Principle of HFLI Z_V_{GB} circuit

There is a 180° phase difference between an inductor and capacitor, and a 90° phase difference between an inductor and resistor. The capacitive reactance and inductive reactance are shown in Eq. (8). According to the serial-parallel rule, the impendence of Z_V_{GB} is shown in Eq. (8), where f_b is the resonance frequency. Its frequency response diagram is shown in Fig. 6(b), where *BW_Min* and *BW_Max* are the minimum and maximum frequencies of the bandwidth, respectively.

Generally, as decoupling capacitors are limited by the IC die size, most embedded capacitors range from several tens to hundreds of pF[11]. In our case, capacitors of 20 and 40 pF were recommended by the vendor; they were selected and embedded on the chip for simulation [15]. Therefore, resonance frequencies occurred at 1.12 and 2.42 GHz with C_{Td} = 20 and C_{Rd} = 40 pF, and the dip frequency f_b of Z_V_{GB} is 1.26 GHz. Let the "Ratio", also called noise ratio, be the output noise voltage compared by the input noise voltage as shown in Fig. 6(b). Hence, lower "Ratio" can get lower noise output and better performance. As C_{Td} with a 1.12-GHz resonance frequency and C_{Rd} with a 2.42-GHz resonance frequency are directly connected between the power and ground terminals of the driver and receiver, respectively, there is minimum noise at these two resonance frequencies. Therefore, the available bandwidth of *BW_Min* and *BW_Max* for Z_V_{GB} will be dominated by C_{Td} and C_{Rd}. Then, substituting frequencies of 1.12 and 2.42 GHz into Eq. (8) produces values of *BW_Min* and *BW_Max* for Z_V_{GB} as shown in Fig. 6(b).

$$Z\_V_{GB} = \left(R_{p1} + j2\pi f_b L_p\right) // \left(R_{p2} - j\frac{1}{2\pi f_b C_p}\right) = \frac{R_{P1}R_{P2} + \frac{L_P}{C_P} + j\left(2\pi f_b L_P R_{P2} - \frac{R_{P1}}{2\pi f_b C_P}\right)}{R_{P1} + R_{P2} + j\left(2\pi f_b L_P - \frac{1}{2\pi f_b C_P}\right)}, \quad (8)$$

$$where\ f_b = \frac{1}{2\pi\sqrt{L_P C_P}}.$$

3.3 System analysis

The lower impedance reduces the voltage drop for the same current according to Ohm's law. Therefore, the combination of components R_{p1}, R_{p2}, L_p, and C_p of Z_V_{GB} are selected to obtain a low-impedance value for Z_V_{GB} at high frequencies, which results in a lower voltage drop and a smaller noise drop. Therefore, we can determine the optimal values of the components L_P, C_P, R_{P1}, and R_{P2} according to Eq. (8) such that impedance of Z_V_{GB} is 67%, which the Ratio of f_b = 1.26 GHz is equal to 0.67, of the original model, thus decreasing SSN in this frequency band. Let "Ratio" of the original model be the output noise voltage is equal to the input one in HFLI.

When Z_V_{GB} is connected directly between the power (ground) terminals of the driver and receiver [Z_V_{GBP} (Z_V_{GBG}) in Fig. 7], the voltage drop of node *a* (node *c*) is almost the same as that of node *b* (node *d*) in the power (ground) terminal. In this study, we refer to having two nodes with almost the same voltage drop as the high balance method of reducing SSN between them. The reasons are as follows. The inductive and capacitive reactances [$X_L = 2\pi fL\ \Omega$ and $X_C = 1/(2\pi fC)\ \Omega$] of Z_V_{GB} act as a short circuit in the low and high frequency bands, respectively. Moreover, the power consumption of Z_V_{GB} is almost equal to zero for $R_1 = R_2 = 0.1\ \Omega$. Therefore, when Z_V_{GBP} is connected directly between nodes *a* and *b*, it will appear like a short circuit at low and high frequencies so that nodes *a* and *b* can reach the high balance state. According to the above description, when the high-frequency (low-frequency) SSN is produced, the current passes between nodes *a* and *b* (nodes *c* and *d*) by the series *RC* (*RL*) in Z_V_{GB} to reach the high balance state for reducing SSN. We propose adding Z_V_{GB} to the SiP structure to

reduce SSN effectively, placing it between two power (ground) terminals in an IC as shown in Fig. 8. Tsukada *et al.* proposed a circuit to absorb cross-talk and implemented this concept in SoCs [24]. Popovich *et al.* studied a method to add decoupling capacitors to SoCs to alleviate SSN [19]. Therefore, some Z_V_{GB} can be used in SoC and multi-chip modules (MCMs) to alleviate SSN in ICs [14], [18], [19], [24].

4. Simulation concept and analysis

4.1 Simulation concept

To demonstrate the feasibility of our proposed method, the output and input buffers in the IBIS model were used as the driver and the receiver, respectively. The transmission line model, denoted by *TLine*, and the packaging circuit were connected between these two terminals. Z_V_{GBP} (Z_V_{GBG}) was embedded in the power (ground) terminals between the driver and receiver, and decoupling capacitors C_{Td} and C_{Rd} were added between the power and ground terminals as shown in Fig. 7. Let $|Z_{parasitic}|$ and f_a be the resistive reactance of Z_V_{GB} and the working frequency, respectively, as shown in Eq. (9). Let L_{TDD}, L_{RDD}, L_{TSS}, or L_{RSS} be the stray inductances and C_{TDD}, C_{RDD}, C_{TSS}, or C_{RSS} be the parasitic capacitors [23], [26].

$$|Z_{parasitic}| = \left(j2\pi f_a L\right) // \left(-j\frac{1}{2\pi f_a C}\right) = \frac{2\pi f_a L}{j\left(4\pi^2 f_a^2 LC - 1\right)}, \quad \text{where } f_a = \frac{1}{2\pi\sqrt{LC}}. \tag{9}$$

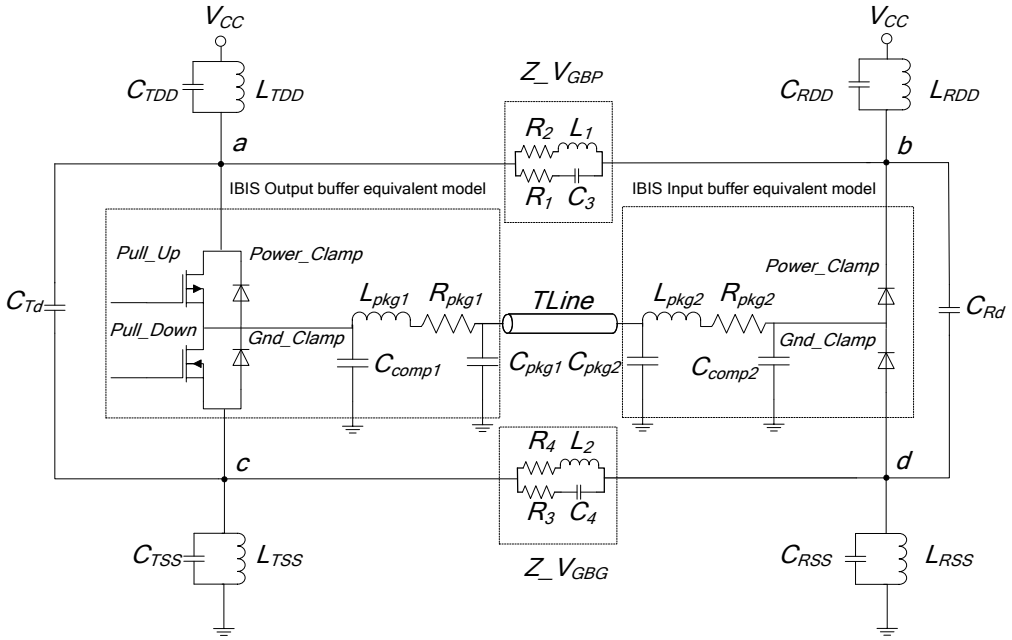

Fig. 7. Schematic of proposed circuit.

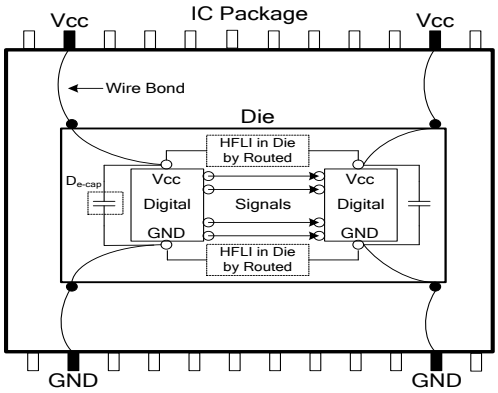

Fig. 8. Application structure of Z_V_{GB} for SiP.

4.2 Analysis of the simulation circuit

Two cases are discussed separately. Case 1 is the input signal transition from *H* to *L* and Case 2 is the input signal transition from *L* to *H*.

Case 1: The input state of the non-inverter (inverter) changes from *H* to *L*. Let Z_{Load} be the load resistance that consists of the package components and *TLine* between the two terminals of the driver and receiver. When the input state of the non-inverter changes from *H* to *L*, the equivalent circuits *Pull_Down* and *Pull_Up* of the IBIS output buffers are in the off and on states, respectively, as shown in Fig. 9. Similarly, when the input state of the inverter changes from *L* to *H*, the equivalent circuits *Pull_Down* and *Pull_Up* of the IBIS output buffers are in the on and off states, respectively. Let $V_{PT\text{-}SSN}$, $V_{PR\text{-}SSN}$, $V_{GT\text{-}SSN}$, and $V_{GR\text{-}SSN}$, be SSN in nodes *a*, *b*, *c*, and *d*, respectively, where Z_V_{GBP} (Z_V_{GBG}) exists between nodes *a* (node *c*) of the driver and *b* (node *d*) of the receiver between the power (ground) terminals.

In a similar manner, the receiver current that passes through C_{RDD} can be obtained from these equations as shown in Eq. (10). Another shunt current passes through L_{RDD} and its voltage can be calculated as shown in Eqs. (11) and (12). Therefore, V_{PT} is as shown in Eq. (4). As the input signal of the receiver will couple to the power and ground planes, this creates more swing noise in the power and ground terminals in the receiver. Therefore, the noise in the receiver is greater than that in the driver terminal. The coupling constant is the degree of noise coupling of the power or ground terminals between the driver and receiver that will determine the degree of noise coupling of the driver to the receiver [12].

Since the received input signal is coupled to the power and ground terminals, it generates more highly unstable noise in these two terminals. In addition, *Power_Clamp* and *Gnd_Clamp* of the receiver terminal will be in the off state since the reverse current passes through them. By substituting Eq. (13) into Eq. (14), the induced current I_4 of C_{Rd} can be obtained as shown in Eqs. (14) and (15). In a manner parallel to Eq. (14), the induced current I_5 of C_{Td} can be obtained in Eq. (15).

$$I_2 = C_{RDD}\frac{dV_{DLC2}}{dt} \tag{10}$$

$$I_{D2} = I_s - I_2 \tag{11}$$

$$V_{DLC2} = L_{RDD}\frac{dI_{D2}}{dt} \tag{12}$$

$$V_{PR} = Vcc - V_{DLC2} = Vcc - L_{RDD}\frac{dI_{PR}}{dt} + L_{RDD}C_{RDD}\frac{d^2V_{DLC2}}{dt^2} \tag{13}$$

$$\begin{aligned} I_4 &= C_{Rd}\frac{d(V_{PR}-V_{GR})}{dt} \\ &= C_{Rd}\frac{dV_{CC}}{dt} - L_{RDD}C_{Rd}\frac{d^2I_{PR}}{dt^2} \\ &\quad - L_{RSS}C_{Rd}\frac{d^2I_{LS2}}{dt^2} + L_{RDD}C_{RDD}C_{Rd}\frac{d^3V_{DLC2}}{dt^3} \end{aligned} \tag{14}$$

$$\begin{aligned} I_5 &= C_{Td}\frac{d(V_{PT}-V_{GT})}{dt} \\ &= C_{Td}\frac{dVcc}{dt} - L_{TDD}C_{Td}\frac{d^2I_{PT}}{dt^2} \\ &\quad - L_{TSS}C_{Td}\frac{d^2I_{LS1}}{dt^2} + L_{TDD}C_{TDD}C_{Td}\frac{d^3V_{DLC1}}{dt^3} \end{aligned} \tag{15}$$

As the noise in the power and ground terminals of the receiver is greater than that in the driver, C_{comp1} is charged through *Pull_Up*. Therefore, I_7 passes through Z_V_{GBP} as shown in Eq. (16).

By substituting Eq. (14) into (16), I_7 can be obtained as shown in Eq. (17). This will generate two shunt currents, I_{ZL1} and I_{ZC1}, when I_7 passes Z_V_{GBP}. Let Z_{C3} be the capacitive reactance of $C3$. V_{C3} can be obtained from Eqs. (18)–(20). In addition, the induced voltage V_{L1} of Z_V_{GBP} is shown in Eq. (21). Finally, I_3 passes through C_{comp1} as shown in Eq. (35).

$$I_7 = I_{PR} - I_4 \tag{16}$$

$$I_7 = I_{PR} - C_{Rd}\frac{dV_{CC}}{dt} + L_{RDD}C_{Rd}\frac{d^2 I_{PR}}{dt^2} + L_{RSS}C_{Rd}\frac{d^2 I_{LS2}}{dt^2} - L_{RDD}C_{RDD}C_{Rd}\frac{d^3 V_{DLC2}}{dt^3} \tag{17}$$

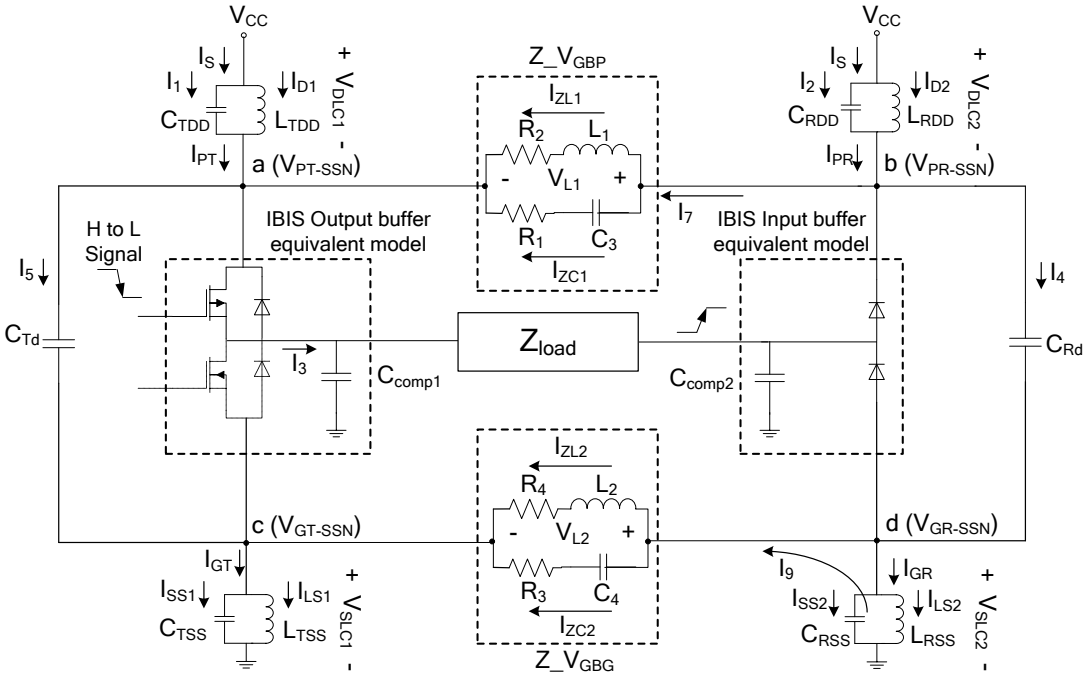

Fig 9. Analysis of an input signal with *H* to *L* transition.

$$V_{C3} = (V_{PR} - V_{PT})\frac{Z_{c3}}{R_1 + Z_{c3}} \tag{18}$$

$$I_{ZC1} = C_3\frac{dV_{c3}}{dt} \tag{19}$$

$$I_{ZL1} = I_7 - I_{ZC1} \tag{20}$$

$$V_{L1} = L_1\frac{dI_{ZL1}}{dt} + I_{ZL1}R_2 \tag{21}$$

Z_V_{GBP} is directly connected between the receiver (node *b*) and the driver (node *a*) such that the potential difference between these two terminals is in high balance according to the law of Section 3.3, as $R_1 = R_2 = 0.1\ \Omega$ is close to zero impedance, and both C_3 and L_1 appear as shorts at the high and low frequencies.

As $R_1 = R_2 = 0.1\ \Omega$, which is close to zero, then C_3 and L_1 are also close to zero at high and low frequencies, respectively.

Therefore, in Eq. (22), $V_{PT\text{-}SSN}$ is almost equal to $V_{PR\text{-}SSN}$. Finally, substituting Eqs. (4), (13), and (21) into (22), SSN of the power terminal can be obtained as shown in Eq. (23). $V_{PT\text{-}SSN}$ is almost equal to the $V_{PR\text{-}SSN}$ shown in Eq. (22), which can be obtained from $V_{PR} - V_{L1} - V_{PT}$, as the V_{PR} shown in Eq. (13) is slightly more than V_{PT} shown in Eq. (4). However, Eq. (22), obtained by subtracting V_{L1} and V_{PT} from V_{PR}, is less than V_{PR} or V_{PT}, which does not include Z_V_{GBP}, as V_{PT} is almost equal to V_{PR}. Therefore, Eq. (22) must be less than V_{PR} or V_{PT}. Moreover, from Eq. (23) after adding Z_V_{GBP}, the

summation of the power terminal SSN will be less than the case without adding this Z_V_{GBP}.

$$V_{PT-SSN} \approx V_{PR-SSN} = \Delta V_{PR} - V_{L1} - \Delta V_{PT} \tag{22}$$

$$V_{PT-SSN} \approx V_{PR-SSN} = L_{TDD}\frac{dI_{PT}}{dt} + L_{RDD}C_{RDD}\frac{d^2V_{DLC2}}{dt^2} - L_{RDD}\frac{dI_{PR}}{dt} - L_{TDD}C_{TDD}\frac{d^2V_{DLC1}}{dt^2} - I_7 \times Z\_V_{GBP} \tag{23}$$

The impedance of Z_V_{GBG} in the driver is more than the ground impedance Z_{G1} that consists of C_{TSS} and L_{TSS}, and Z_{G2} that consists of C_{RSS} and L_{RSS}. Nodes *c* and *d* are open in the transient state when $I_5 = I_{GT}$ and $I_4 = I_{GR}$ pass through these two nodes. When I_{GT} (I_{GR}) passes through the grounded packaging components of the driver terminal to be the shunt current I_{SS1} and I_{LS1}, (I_{SS2} and I_{LS2}), it will generate the induced noise voltage V_{GT} and V_{GR} shown in Eqs. (24) and (25).

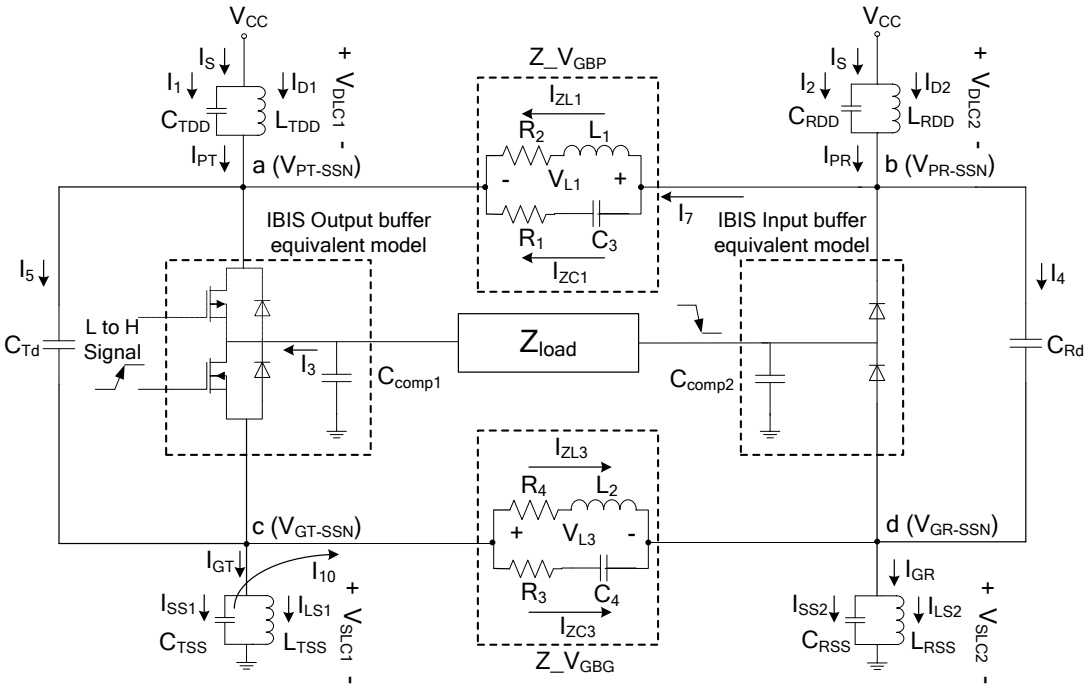

Fig. 10. Analysis of testing circuit of input with *L* to *H*.

$$\Delta V_{GT} = L_{TSS}\frac{dI_{LS1}}{dt},$$
$$where\ I_{SS1} = C_{TSS}\frac{dV_{GT}}{dt}\ and\ I_{LS1} = I_{GT} - I_{SS1}. \tag{24}$$

$$\Delta V_{GR} = L_{RSS}\frac{dI_{LS2}}{dt},$$
$$where\ I_{SS2} = C_{RSS}\frac{dV_{GR}}{dt}\ and\ I_{LS2} = I_{GR} - I_{SS2}. \tag{25}$$

When the scale of C_{RSS} is charged up to V_{GR}, the current is discharged by Z_V_{GBG}, L_{TSS}, and C_{TSS}. Therefore, let I_9 be the discharged current as shown in Eq. (26). When I_9 passes through Z_V_{GBG} to generate two shunt currents, I_{ZC2} and I_{ZL2}, as shown in Eqs. (28) and (29), then according to law of voltage division, V_{C4} is shown in Eq. (27). Let Z_{C4} be the impedance of capacitor *C4*. The voltage V_{L2} as shown in Eq. (30) is induced from Z_V_{GBG}.

$$I_9 = C_{RSS}\frac{dV_{GR}}{dt} \tag{26}$$

$$V_{C4} = (V_{GR} - V_{GT}) \frac{Z_{c4}}{R_3 + Z_{c4}} \quad (27)$$

$$I_{ZC2} = C_4 \frac{dV_{c4}}{dt} \quad (28)$$

$$I_{ZL2} = I_9 - I_{ZC2} \quad (29)$$

$$V_{L2} = L_2 \frac{dI_{ZL2}}{dt} + I_{ZL2} R_4 \quad (30)$$

Z_V_{GBG} is also directly connected between receiver and driver such that the potential difference between these two terminals can also be in high balance. Therefore, in Eq. (31), $V_{GT\text{-}SSN}$ and $V_{GR\text{-}SSN}$ are SSN of driver and receiver, respectively. By substituting Eqs. (24), (25), and (30) into Eq. (31), SSN of the power terminal can be obtained as shown in Eq. (32). Similar to the above description, from Eq. (32), after adding Z_V_{GBP}, the summation of the ground terminal SSN will be less than the case without addition of this Z_V_{GBP}.

$$V_{GT-SSN} \approx V_{GR-SSN} = \Delta V_{GR} - V_{L2} - \Delta V_{GT} \quad (31)$$

$$V_{GT-SSN} \approx V_{GR-SSN} = L_{RSS} \frac{dI_{LS2}}{dt} - L_{TSS} \frac{dI_{LS1}}{dt} - I_9 \times Z\_V_{GBG} \quad (32)$$

Case 2: The input state changes from *L* to *H*. When the input transition state of the non-inverter changes from *L* to *H*, *Pull_Down* and *Pull_Up* are in the on and off states, respectively, as shown in Fig. 10. Similar to the schematic analysis of the input transition state from *H* to *L*, one current is marked by an arrow.

Furthermore, I_5 shown in Eq. (15) is induced by C_{Td} and modified as shown in Eq. (33). Substituting Eq. (17) to Eq. (33), the current I_5 is as shown in Eq. (34).

$$I_5 = I_{PT} + I_7 \quad (33)$$

$$= I_{PT} + I_{PR} - C_{Rd} \frac{dV_{CC}}{dt} - L_{RDD} C_{Rd} \frac{d^2 I_{PR}}{dt^2} + L_{RDD} C_{RDD} C_{Rd} \frac{d^3 V_{DLC2}}{dt^3} \quad (34)$$

The impedance of Z_V_{GBG} in the driver is more than the ground impedance Z_{G1} that consists of C_{TSS} and L_{TSS}, and Z_{G2} that consists of C_{RSS} and L_{RSS}. Both nodes *c* and *d* are momentarily off when I_5 and I_4 pass through them. I_{GT} in C_{comp1} to be discharged passes through L_{TSS} and C_{TSS} to the ground plane as shown in Eq. (35). Furthermore, I_{SS1}, I_{LS1}, I_{SS2}, I_{LS2}, ΔV_{GT}, and ΔV_{GR} are shown in Eqs. (36) and (37).

$$I_{GT} = I_5 + I_3, \quad where\ I_3 = I_{PT} + I_7 - I_5. \quad (35)$$

$$\Delta V_{GT} = L_{TSS} \frac{dI_{LS1}}{dt}, \quad where\ I_{SS1} = C_{TSS} \frac{dV_{GT}}{dt}\ and\ I_{LS1} = I_{GT} - I_{SS1}. \quad (36)$$

$$\Delta V_{GR} = L_{RSS} \frac{dI_{LS2}}{dt}, \quad where\ I_{SS2} = C_{RSS} \frac{dV_{GR}}{dt}\ and\ I_{LS2} = I_{GR} - I_{SS2}. \quad (37)$$

Finally, when C_{TSS} is charged to a voltage equal to V_{GT}, the current is discharged by Z_V_{GBG}, L_{TSS}, and C_{TSS}. Therefore, let I_{10} be the discharged current as shown in Eq. (38). When I_{10} passes through Z_V_{GBG}, it generates two shunt currents, I_{ZC3} and I_{ZL3}, shown in Eqs. (40) and (41); V_{C4} is shown in Eq. (39) according to the law of voltage division. Let Z_{C4} be the impedance of capacitor *C4*. Voltage V_{L3} is induced in Z_V_{GBG} and shown in Eq. (42).

$$I_{10} = C_{TSS} \frac{dV_{GT}}{dt} \quad (38)$$

$$V_{C4} = (V_{GT} - V_{GR}) \frac{Z_{c4}}{R_3 + Z_{c4}} \quad (39)$$

$$I_{ZC3} = C_4 \frac{dV_{c4}}{dt} \quad (40)$$

$$I_{ZL3} = I_{10} - I_{ZC3} \quad (41)$$

$$V_{L3} = L_2 \frac{dI_{ZL3}}{dt} + I_{ZL3} R_4 \quad (42)$$

Similar to the case of input transition for *H* to *L*, for the input transition state from *H* to *L* (*L* to *H*), Z_V_{GBG} can be directly connected between the receiver and driver such that the potential difference between these two terminals will be in a high balance state according to the description in Section 3.3, as $R_1 = R_2 = 0.1\ \Omega$ is close to zero impedance, and both C_3 and L_1 appear as shorts at the high and low frequencies, respectively. Thus, in Eq. (43), $V_{GT\text{-}SSN}$ and $V_{GR\text{-}SSN}$ are SSN of the driver and receiver, respectively, in high balance. By substituting Eqs. (36), (37), and (42) into (43), SSN of the ground terminal can be obtained as shown in Eq. (44).

$$V_{GT-SSN} \approx V_{GR-SSN} = V_{GT} - V_{L3} - V_{GR} \quad (43)$$

$$= L_{TSS} \frac{dI_{LS1}}{dt} - L_2 \frac{dI_{ZL3}}{dt} - L_{RSS} \frac{dI_{LS2}}{dt} - I_{ZL3} R_4 \quad (44)$$

From this derivation, the effect of the input signal can be induced onto the power and ground planes such that it will cause the receiver to produce a heavy swing. That is, SSN in the power and ground terminals of the receiver will be more than that of the driver. Therefore, the V_{PR} and V_{GR} swing of the driver exceed that of V_{PT} and V_{GT} in the driver, respectively.

4.3 Simulation Results

The HSPICE model and IBIS are for an MT47H128M4/MT47H64M8 512 MB DDR2 SDRAM DQ, a 16/32 bit bidirectional buffer chip manufactured by Micron Technology [15]. The $IBIS_{De\text{-}cap+Z\text{-}VGB}$ uses the B-element of HSPICE to describe it [1]. The components were set to $R_1 = R_2 = R_3 = R_4 = 0.1\ \Omega$, $C_{Td} = 20$ pF, $C_{Rd} = 40$ pF, $C_3 = C_4 = 200$ pF [18], [14], $C_{TDD} = C_{RDD} = C_{TSS} = C_{RSS} = C_{comp1} = C_{comp2} = 1$ pF, and $L_1 = L_2 = 0.1$ nH. $L_{TDD} = L_{RDD} = L_{TSS} = L_{RSS} = 1$ nH when $f = 1.2959$ GHz, and the bandwidth of Z_V_{GB} is between 1.1194 and 2.4153 GHz.

Five models were used in our simulations: HSPICE, IBIS, $IBIS_{De\text{-}cap}$, $IBIS_{Z\text{-}VGB}$, and $IBIS_{De\text{-}cap+Z\text{-}VGB}$. The IBIS model is that two stages, driver terminal, receiver terminal, is directly connected by a metal line. Then, $IBIS_{De\text{-}cap}$ and $IBIS_{Z\text{-}VGB}$ are IBIS with decoupling capacitors and with Z_V_{GB}, respectively. $IBIS_{Z\text{-}VGB}$ was obtained from $IBIS_{De\text{-}cap+Z\text{-}VGB}$ without decoupling capacitors. Our design, $IBIS_{De\text{-}cap+Z\text{-}VGB}$, is IBIS with decoupling capacitors and Z_V_{GB}. That is, $IBIS_{De\text{-}cap+Z\text{-}VGB}$ consists of the following components: the driver terminal, receiver terminal, *TLine*, Z_V_{GBP}, Z_V_{GBG}, C_{Td}, and C_{Rd}, such that it can effectively reduce the noise $\Delta V_{p\text{-}p}$ to a minimum.

The comparison result of the driver $V_{GT\text{-}SSN}$ between our derivation equation and simulation $IBIS_{De\text{-}cap+Z\text{-}VGB}$ model are shown in Fig. 11, which just shows one cycle within 8 ns. From this result, they indicate that the peak-to-peak values of our derivation equation model marked by the bold line and $IBIS_{De\text{-}cap+Z\text{-}VGB}$ simulation model marked by the dotted line are 130 mV and 127 mV, respectively. The error rate between them is just within 2.3% ((130-127) /130 = 2.3%). Two reasons cause this error rate between them. The first one is that our derived equation model is three factorials of differential equations and the HSPICE tool maybe is more than these three factorials of differential equations. The second reason is that our derived equation model does not accurately estimate and calculate the noise coupling coefficient model, which is the intensity of the noise energy that can be coupled to the next stage, between of the driver and receiver terminals by transmission line.

Moreover, as $V_{GR\text{-}SSN}$ is the maximum of the four nodes, the results for the various models are

compared in Table 1 and in Figs. 12(a)–(d). Furthermore, Figs. 12(a)–(d) show a comparison of maximum $V_{GT\text{-}SSN}$ values for the four nodes.

In this paper, we propose a new methodology based on an enhanced IBIS mode such that $V_{GR\text{-}SSN}$ of the four models (452 mV for IBIS, 290 mV for $IBIS_{De\text{-}cap}$, 163 mV for $IBIS_{Z\text{-}VGB}$, and 301 mV for HSPICE) was effectively reduced by 121 mV as measured by the peak-to-peak value shown in Figs. 13(a)–(d). That is, our proposed model effectively reduced the noise by more than 73.2%, 58.3%, 25.7%, and 59.8% as compared to the IBIS, $IBIS_{De\text{-}cap}$, $IBIS_{Z\_VGB}$, and HSPICE methods, respectively. According to the voltage constraint, where SSN is less than the power voltage within 10% $V_{p\text{-}p}$ [2], if the working voltage is 1.8 V, its SSN limitation would be less than 180 mV. Therefore, our proposed model can just meet this requirement.

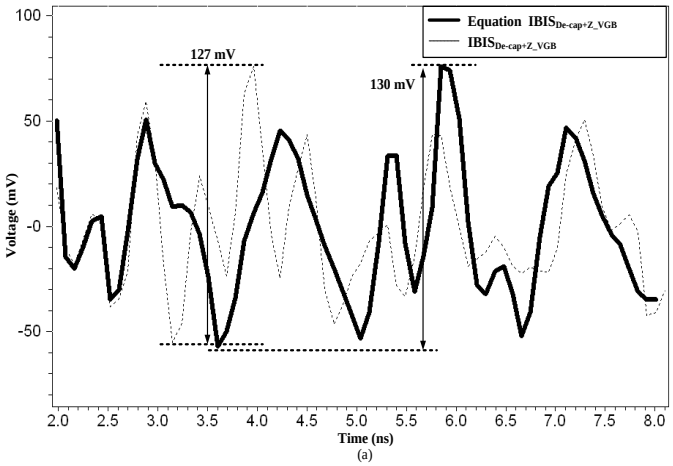

Fig. 11. Comparison of $V_{GT\text{-}SSN}$ between derivation equation and $IBIS_{De\text{-}cap+Z\text{-}VGB}$.

Table 1. Comparison of the input and output noise $V_{p\text{-}p}$ for the five models

Input SSN of various models	**IBIS**		**$IBIS_{De\text{-}cap}$**		**$IBIS_{Z\text{-}VGB}$**		**HSPICE**		**$IBIS_{De\text{-}Cap+Z\text{-}VGB}$**	
$V_{p\text{-}p}$(mV)	$V_{PT\text{-}SSN}$	$V_{GT\text{-}SSN}$	$V_{PT\text{-}SSN}$	$V_{GT\text{-}SSN}$	$V_{PT\text{-}SSN}$	$V_{GT\text{-}SSN}$	$V_{PT\text{-}SSN}$	$V_{GT\text{-}SSN}$	$V_{PT\text{-}SSN}$	$V_{GT\text{-}SSN}$
	300	260	210	182	202	160	200	215	160	127
Output SSN of various models	**IBIS**		**$IBIS_{De\text{-}cap}$**		**$IBIS_{Z\text{-}VGB}$**		**HSPICE**		**$IBIS_{De\text{-}Cap+Z\text{-}VGB}$**	
$V_{p\text{-}p}$(mV)	$V_{PR\text{-}SSN}$	$V_{GR\text{-}SSN}$	$V_{PR\text{-}SSN}$	$V_{GR\text{-}SSN}$	$V_{PR\text{-}SSN}$	$V_{GR\text{-}SSN}$	$V_{PR\text{-}SSN}$	$V_{GR\text{-}SSN}$	$V_{PR\text{-}SSN}$	$V_{GR\text{-}SSN}$
	420	452	250	290	230	163	240	301	140	121

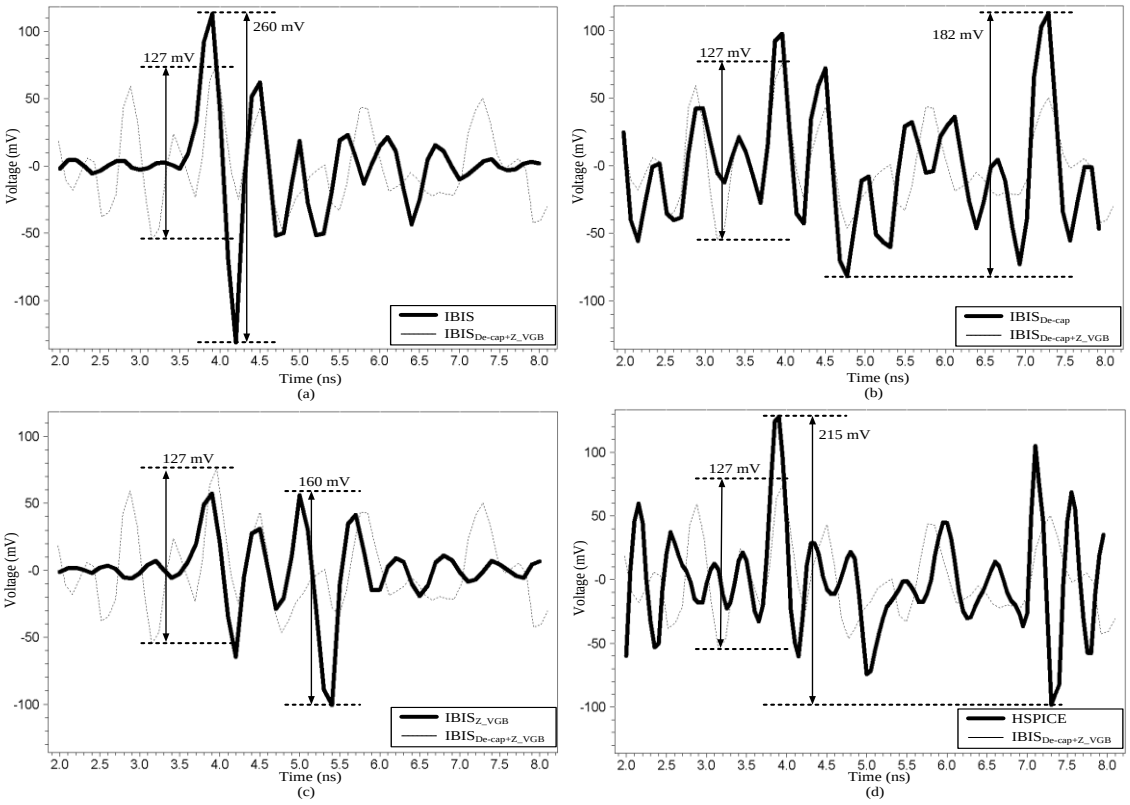

Fig. 12. Comparisons of $V_{GT\text{-}SSN}$ between (a) IBIS and IBIS$_{De\text{-}Cap+Z\text{-}VGB}$, (b) IBIS$_{De\text{-}cap}$ and IBIS$_{De\text{-}Cap+Z\text{-}VGB}$, (c) IBIS$_{Z\text{-}VGB}$ and IBIS$_{De\text{-}Cap+Z\text{-}VGB}$, and (d) HSPICE and IBIS$_{De\text{-}Cap+Z\text{-}VGB}$.

5. Conclusions

A major area of research for high-speed PCB design involves the prevention and reduction of SSN. The method proposed here in the simulation phase showed whether the design specification for SSN in an IC was met. Then, a prevention strategy could be developed based on an integrated approach using the decoupling capacitors on the IC chip and the Z_V_{GB} HFLI enhanced module connected between the driver and the receiver terminals of the power and ground, respectively, to optimize performance and reduce SSN. This design effectively reduced the noise. Moreover, we demonstrate that the error rate of peak-to-peak values between our derivation equation model and IBIS$_{De\text{-}cap+Z\text{-}VGB}$ is just within 2.3%. So, our model can be used to estimate SSN. Our results not only showed that aside from our model, the four other models (IBIS, IBIS$_{De\text{-}cap}$, IBIS$_{Z\text{-}VGB}$, and HSPICE) cannot effectively reduce SSN, but also proved that $V_{GR\text{-}SSN}$ of the four models, 452 mV for IBIS, 290 mV for IBIS$_{De\text{-}cap}$, 163 mV for IBIS$_{Z\text{-}VGB}$, and 301 mV for HSPICE, was effectively reduced by 121 mV of IBIS$_{De\text{-}Cap+Z\text{-}VGB}$ as measured by the peak-to-peak value. That is, our proposed model performed 73.2%, 58.3%, 25.7%, and 59.8% better than the four other methodologies, respectively. In addition, the mathematical equations for the HFLI enhanced-module were deduced and confirmed in this study, and represent the basis for applying HFLI to the high balance design method. We believe that our new method can be used in IC chip design for effectively reducing SSN while retaining adequate PI.

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