A Novel Design for Evaluating Simultaneous Switching Noise within an Enhanced IBIS Model

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Abstract: Simultaneous switching noise (SSN) is a major cause of power integrity (PI) degradation that causes circuits to become unstable and experience errors. As modern ICs operate at higher speeds with higher density and lower voltages, SSN has become a serious issue that must be addressed to ensure system stability during the short rise- and fall-times of the logic transient states. Most traditional designs have generally used decoupling capacitors to reduce SSN. As these capacitors become equivalent series inductances when the system operates at high frequencies, such a technique works against reducing SSN. Therefore, we propose a methodology called the enhanced IBIS model that effectively alleviates the problem of SSN using an evaluation based on the enhanced I/O buffer information specification (IBIS) model with decoupling capacitors and a high-frequency low-impendence circuit. In this study, we showed that SSN from 452 mV, 290 mV, 163 mV, and 301 mV, of IBIS, traditional decoupling capacitors, IBIS with a high-frequency low-impendence circuit, and HP Simulation Program with Integrated Circuit Emphasis (HSPICE) methodologies, respectively, was effectively reduced by 121 mV of our enhanced IBIS mode as measured by the peak-to-peak value. That is, our new method reduces noise by more than 73.2%, 58.3%, 25.7%, and 59.8% compared to other four methodologies, respectively.

Key Word: Simultaneous Switching Noise (SSN), Power Integrity (PI), I/O Buffer Information Specification (IBIS), HSPICE, High-frequency low-impedance (HFLI) circuit.

1. Introduction

Modern integrated circuits (ICs) contain several million transistor cells on a single die. Under high-speed, high-density, low-voltage conditions, ICs can make perfectly controlled timing changes within a single die. Simultaneous switching noise (SSN) is a major source of noise that affects system stability, and is much more significant than crosstalk, reflection-talk, and

frequencies, SSN is caused by the packaging parasitic effect between the die wire bonds and their pads. This causes the reference voltage of the power and ground terminals to bounce, making them unstable [25], [23]. The equivalent circuit of this packaging parasitism consists of a parallel inductor and capacitor (LC) in series with the power and ground terminals of IBIS as shown in Fig. 2. Components "C_{TDD} parallel to L_{TDD}" and "C_{TSS} parallel to L_{TSS}" are used to describe this LC effect called stray conductance and parasitic capacitance [27], [26].

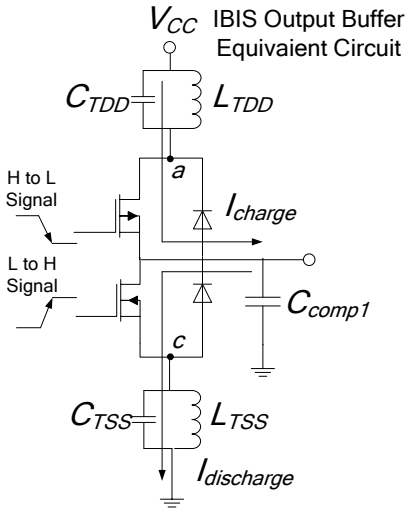

Fig. 2. Equivalent circuit in IBIS and the packaging parasitic circuit.

Buffers sink the current from the power terminal for a transient digital signal, and this current will pass through C_{TDD} and L_{TDD}. This charging current, I_{charge}, passes the equivalent IBIS P-channel metal oxide semiconductor (PMOS) component and then charges the output capacitor C_{comp1}. When the digital signal changes state, the transient discharge current, $I_{discharge}$, discharges to the ground terminal from the previously charged capacitor C_{comp1} through the equivalent IBIS N-channel metal oxide semiconductor (NMOS) component as well as C_{TSS} and L_{TSS} as shown in Fig. 2.

As the input signal of the active components or input/output buffers is in a transient state, these active components will sink current from the power terminal or discharge current to the ground terminal and induce SSN in the power and ground terminals, respectively [23]. When the IC signal is in several transient states simultaneously, the buffer will momentarily draw a large amount of current from the power source. This current passes through the inductor and induces a voltage drop across it, which causes a reference power/ground bounce between the power and ground terminals. Typical SSN between the power and ground terminals is shown in Figs. 3(a) and (b) [27], [26]. The maximum SSN swing, which is the difference between the global minimum and the global maximum in the waveform, is denoted by its peak-to-peak value, $\Delta V_{p\text{-}p}$ [20]. Therefore, this SSN is called the power or ground bounce [23], [9], [26], [33]. The amount of current in the double buffers working together in IBIS is more than that of the single one. In addition, when many IC signals are simultaneously in transient states, the SSN swing becomes more serious. As this increases the error rate of the output timing, the maximum noise swing must be limited to within 10% of its operational voltage by $\Delta V_{p\text{-}p}$ [2], [20], *i.e.*, the peak voltage difference between the global maximum and minimum.

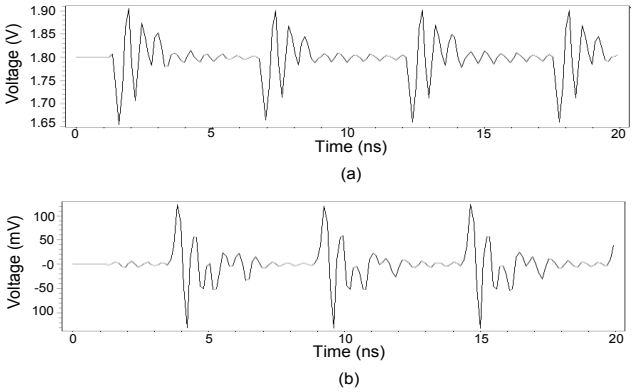

Fig. 3. (a) Typical SSN in the power plane. (b). Typical SSN in the ground plane.

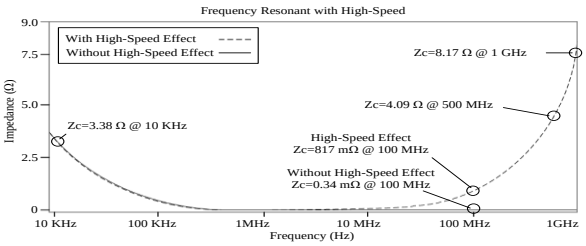

Fig. 4. Characteristics of decoupling capacitors for high frequencies.

2.3 Characteristics of decoupling capacitors

Decoupling capacitors are usually used on printed circuit boards (PCBs) or in IC packaging to reduce the SSN noise and maintain PI stability. The impedance *Zc* of the ideal capacitor is $1/(2\pi fc)$ Ω; this reactance is lower for higher frequencies. A pure capacitor maintains its capacitance characteristics for frequencies below the self-resonant frequency and exhibits inductor characteristics for frequencies greater than the self-resonant frequency [2]. For most electronic products, signal integrity effects begin to be important at clock frequencies above about 100 MHz, called the high-speed effect [2]. For example, in the case without high-speed effect, the lumped impedance values of a 4.7 μF capacitor are 3.38 Ω and 0.34 mΩ at 10 kHz and 100 MHz, respectively. Therefore, it is effectively a short circuit at 100 MHz as shown in Fig. 4

Hence, its capacitive reactance will increase for increasing frequencies during this inductance phase. Therefore, the impedance characteristics of decoupling capacitors change from capacitance behavior to inductance behavior according to the equation *Z-HFC* = *ESR* + *ESL* + $1/(2\pi fc)$ Ω [2], [28], where $f_{Z\text{-}HFC} = \frac{1}{2\pi\sqrt{LC}}$, and *Z-HFC* is the second-order equivalent capacity impendence. In the case with high-speed effect, the lumped impedance values of the same 4.7 μF capacitor are 3.38 Ω and 817 mΩ at 10 kHz and 100 MHz, respectively. Moreover, *Z-HFC* is 4.09 and 8.17 at 500 MHz and 1 GHz, respectively. Therefore, it will not be a short circuit at high frequencies as shown in Fig. 4.

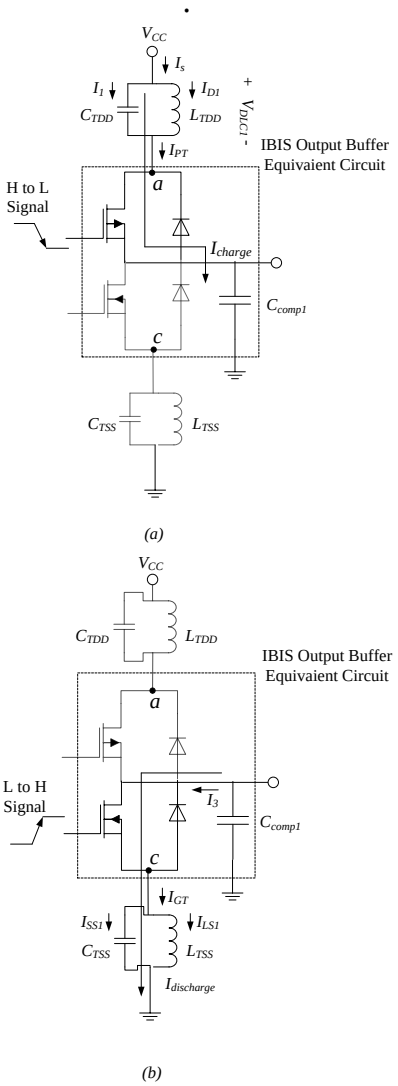

Fig. 5. Behavior of IBIS output buffer operations. (a). *L* to *H* operation. (b). *H* to *L* operation.

2.4 Principle of SSN in the IBIS model

We will use the input and output equivalent circuits of IBIS shown in Fig. 5 to explain different operations. Let capacitors C_{TDD} and C_{TSS} and inductors L_{TDD} and L_{TSS} be the packaging parasitic capacitance and stray

conductance between the power and ground terminals, respectively, [23], [26]. Here, we will first consider the working principle and ignore the packaging parasitism components, R_{pkg}, C_{pkg}, and L_{pkg}.

When the input signal changes from *H* to *L*, *Pull_Down* and *Pull_Up* are in the off and on states, respectively. Then, C_{comp1} is charged by I_{charge} through *Pull_Up* marked by the heavy solid line shown in Fig. 5. I_{D1} passes through the component L_{TDD}, and then L_{TDD} will induce the SSN V_{DLC1} in the power terminal as shown in Eq. (1). Moreover, the terminal voltage of C_{TDD} is parallel to L_{TDD}, and hence, its voltage is equal to V_{DLC1}. I_1 passes through C_{TDD} as shown in Eq. (2). According to node current laws, I_S is equal to the sum of I_1 and I_{D1} as shown in Eq. (3). In this study, let V_{PT} be SSN of node *a*, so $V_{PT} = Vcc - V_{DLC1}$. By substituting Eq. (1) into (2), Eq. (2) into (3), and Eq. (3) into V_{PT} above, then V_{PT} can be obtained as shown in Eq. (4). I_{PT} is the output current of node *a*, which according to Kirchhoff's law, is equal to I_s. Thus, V_{PT} is simply SSN of the power terminal.

$$V_{DLC1} = L_{TDD}\frac{dI_{D1}}{dt} \quad (1)$$

$$I_1 = C_{TDD}\frac{dV_{DLC1}}{dt} \quad (2)$$

$$I_{D1} = I_s - I_1 = I_s - C_{TDD}\frac{dV_{DLC1}}{dt} \quad (3)$$

$$\Delta V_{PT} = Vcc - L_{TDD}\frac{dI_{PT}}{dt} + L_{TDD}C_{TDD}\frac{d^2V_{DLC1}}{dt^2} \quad (4)$$

When the state of the input signal changes from *L* to *H*, *Pull_Down* and *Pull_Up* are in the on and off states, respectively. Then, the $I_{discharge}$ path of C_{comp1} is discharged to the ground terminal through *Pull_Down*. Hence, the stray conductance can induce SSN in the ground terminal. Therefore, the discharge current I_3 of C_{comp1} is equal to I_{PT}, and the discharged current $I_{GT} = I_3$ passes through node *c* as shown in Eqs. (5) and (6). The ground noise ΔV_{GT} is shown in Eq. (7), obtained in a similar manner to Eq. (4).

$$I_{SS1} = C_{TSS}\frac{dV_{C\_comp1}}{dt} \quad (5)$$

$$I_{LS1} = I_{GT} - I_{SS1} \quad (6)$$

$$\Delta V_{GT} = L_{TSS}\frac{dI_{LS1}}{dt} = L_{TSS}\frac{dI_{GT}}{dt} - L_{TSS}C_{TSS}\frac{d^2V_{C\_comp1}}{dt^2} \quad (7)$$

3. Proposed high-frequency low-impedance (HFLI) circuit

3.1 HFLI concept

As decoupling capacitors filter the noise in digital systems [10], they can be added between the power and ground terminals. However, at high frequencies, the capacitance characteristic of a capacitor will change to inductance and cannot effectively reduce SSN. We propose an HFLI equivalent circuit for use in IBIS. This circuit Z_V_{GB} consists of two resistors R_{p1} and R_{p2}, one inductor L_p, and one capacitor C_p, as shown in Fig. 6(a). Its major function is to reduce SSN of power and ground terminals effectively to decrease $\Delta V_{p\text{-}p}$ to a minimum.

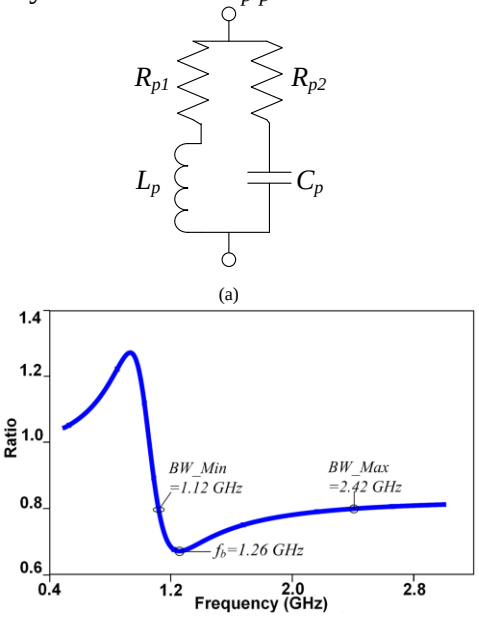

Fig. 6(a). Z_V_{GB} circuit. 6(b). Frequency response diagram of Z_V_{GB}.

3.2 Principle of HFLI Z_V_{GB} circuit

There is a 180° phase difference between an inductor and capacitor, and a 90° phase difference between an inductor and resistor. The capacitive reactance and inductive reactance are shown in Eq. (8). According to the serial-parallel rule, the impendence of Z_V_{GB} is shown in Eq. (8), where f_b is the resonance frequency. Its frequency response diagram is shown in Fig. 6(b), where *BW_Min* and *BW_Max* are the minimum and maximum frequencies of the bandwidth, respectively.

Generally, as decoupling capacitors are limited by the IC die size, most embedded capacitors range from several tens to hundreds of pF[11]. In our case, capacitors of 20 and 40 pF were recommended by the vendor; they were selected and embedded on the chip for simulation [15]. Therefore, resonance frequencies occurred at 1.12 and 2.42 GHz with C_{Td} = 20 and C_{Rd} = 40 pF, and the dip frequency f_b of Z_V_{GB} is 1.26 GHz. Let the "Ratio", also called noise ratio, be the output noise voltage compared by the input noise voltage as shown in Fig. 6(b). Hence, lower "Ratio" can get lower noise output and better performance. As C_{Td} with a 1.12-GHz resonance frequency and C_{Rd} with a 2.42-GHz resonance frequency are directly connected between the power and ground terminals of the driver and receiver, respectively, there is minimum noise at these two resonance frequencies. Therefore, the available bandwidth of *BW_Min* and *BW_Max* for Z_V_{GB} will be dominated by C_{Td} and C_{Rd}. Then, substituting frequencies of 1.12 and 2.42 GHz into Eq. (8) produces values of *BW_Min* and *BW_Max* for Z_V_{GB} as shown in Fig. 6(b).

$$Z\_V_{GB} = \left(R_{p1} + j2\pi f_b L_p\right) // \left(R_{p2} - j\frac{1}{2\pi f_b C_p}\right) = \frac{R_{P1}R_{P2} + \frac{L_P}{C_P} + j\left(2\pi f_b L_P R_{P2} - \frac{R_{P1}}{2\pi f_b C_P}\right)}{R_{P1} + R_{P2} + j\left(2\pi f_b L_P - \frac{1}{2\pi f_b C_P}\right)}, \quad (8)$$

$$where\ f_b = \frac{1}{2\pi\sqrt{L_P C_P}}.$$

3.3 System analysis

The lower impedance reduces the voltage drop for the same current according to Ohm's law. Therefore, the combination of components R_{p1}, R_{p2}, L_p, and C_p of Z_V_{GB} are selected to obtain a low-impedance value for Z_V_{GB} at high frequencies, which results in a lower voltage drop and a smaller noise drop. Therefore, we can determine the optimal values of the components L_P, C_P, R_{P1}, and R_{P2} according to Eq. (8) such that impedance of Z_V_{GB} is 67%, which the Ratio of f_b = 1.26 GHz is equal to 0.67, of the original model, thus decreasing SSN in this frequency band. Let "Ratio" of the original model be the output noise voltage is equal to the input one in HFLI.

When Z_V_{GB} is connected directly between the power (ground) terminals of the driver and receiver [Z_V_{GBP} (Z_V_{GBG}) in Fig. 7], the voltage drop of node *a* (node *c*) is almost the same as that of node *b* (node *d*) in the power (ground) terminal. In this study, we refer to having two nodes with almost the same voltage drop as the high balance method of reducing SSN between them. The reasons are as follows. The inductive and capacitive reactances [$X_L = 2\pi fL\ \Omega$ and $X_C = 1/(2\pi fC)\ \Omega$] of Z_V_{GB} act as a short circuit in the low and high frequency bands, respectively. Moreover, the power consumption of Z_V_{GB} is almost equal to zero for $R_1 = R_2 = 0.1\ \Omega$. Therefore, when Z_V_{GBP} is connected directly between nodes *a* and *b*, it will appear like a short circuit at low and high frequencies so that nodes *a* and *b* can reach the high balance state. According to the above description, when the high-frequency (low-frequency) SSN is produced, the current passes between nodes *a* and *b* (nodes *c* and *d*) by the series *RC* (*RL*) in Z_V_{GB} to reach the high balance state for reducing SSN. We propose adding Z_V_{GB} to the SiP structure to

reduce SSN effectively, placing it between two power (ground) terminals in an IC as shown in Fig. 8. Tsukada *et al.* proposed a circuit to absorb cross-talk and implemented this concept in SoCs [24]. Popovich *et al.* studied a method to add decoupling capacitors to SoCs to alleviate SSN [19]. Therefore, some Z_V_{GB} can be used in SoC and multi-chip modules (MCMs) to alleviate SSN in ICs [14], [18], [19], [24].

4. Simulation concept and analysis

4.1 Simulation concept

To demonstrate the feasibility of our proposed method, the output and input buffers in the IBIS model were used as the driver and the receiver, respectively. The transmission line model, denoted by *TLine*, and the packaging circuit were connected between these two terminals. Z_V_{GBP} (Z_V_{GBG}) was embedded in the power (ground) terminals between the driver and receiver, and decoupling capacitors C_{Td} and C_{Rd} were added between the power and ground terminals as shown in Fig. 7. Let $|Z_{parasitic}|$ and f_a be the resistive reactance of Z_V_{GB} and the working frequency, respectively, as shown in Eq. (9). Let L_{TDD}, L_{RDD}, L_{TSS}, or L_{RSS} be the stray inductances and C_{TDD}, C_{RDD}, C_{TSS}, or C_{RSS} be the parasitic capacitors [23], [26].

$$|Z_{parasitic}| = \left(j2\pi f_a L\right) // \left(-j\frac{1}{2\pi f_a C}\right) = \frac{2\pi f_a L}{j\left(4\pi^2 f_a^2 LC - 1\right)}, \quad \text{where } f_a = \frac{1}{2\pi\sqrt{LC}}. \tag{9}$$

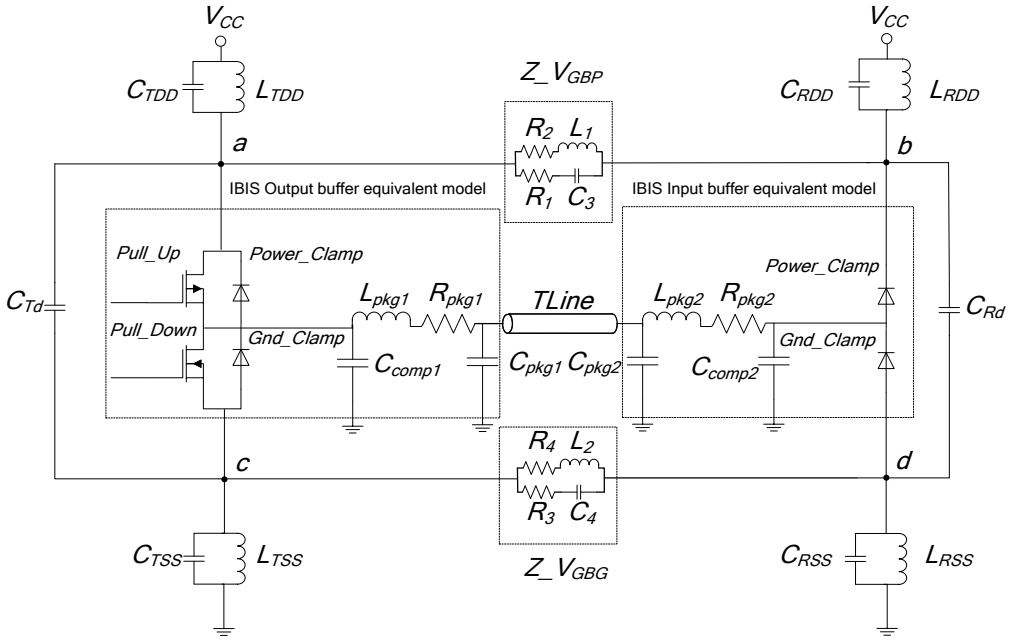

Fig. 7. Schematic of proposed circuit.

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