# Performances of CMOS Thermal-Compensation Total-Current References

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*Abstract:* - „Total"-current reference sources, composed of two classic cross-connected current mirrors, have been launched by the authors in some earlier published works. Theirs major advantages are: simple serially interconnection with the charge and the minimum supply current (this is just the reference current). This work is a comparative analysis of the performances of two total-current reference-source variants with first and second-order thermal compensation, using different integrated resistor types, having positive, zero or negative temperature coefficient. The possibility of obtaining a set of good performances by using NTC resistors is signalled but also, the inefficiency of second-order thermal-compensation for many cases of resistor-temperature-coefficient combinations. A total temperature variation of the reference current, for a particular source variant, is reported, which represents a record: 0.017% for a temperature range of 0-100$^{o}$C.

*Key-words*: Analogue Integrated Circuits, CMOS Current Reference**,** Thermal Compensation, Total-Current Reference.

## 1 Introduction

A simple and compact CMOS current reference source (CRS), composed of two cross-connected current mirrors (or "self-biasing" sources) has been launched by the work [1] (1995). It uses a modified-Wilson mirror and a cascode-mirror combination, having a previously calculated first-order-equivalent thermal compensation. The reference current has a great value (50µA) so that the Wilson-mirror resistance obtains a reduced value. But this source is not conceived with an output to the charge. It needs a start-up circuit too, solved by a logical-gate scheme. The current-temperature-variation performance, of +6.5%, may be considered bad, while the supply-regulation (SR) parameter, of 1960ppm/V, has a good value thanks to the cascode-type superior current mirror.

The work [2] (1997), which uses cross-connected current mirrors too, has the inferior mirror of modified-Widlar type where the resistance was replaced by a transistor in linear regime, biased by a fixed supplementary current source. The output branches for bi-direction current are simple-mirror branches, which may affect the performances. The inferior-mirror transistors work in weak-inversion regime so, the output currents have extremely low values (<10nA). The supply voltage of this scheme is reduced to 1.2V but the other performances are poor: a current-temperature variation greater than 10% in a range of 140$^{o}$C (lower only at a supply voltage of 3.5V), PSRR of 10%/V (100000ppm/V), current-process variation of ±30% (total 60%). The source does not require a start-up circuit and is achieved with a reduced occupied on chip area.

Paper [3] (2002) includes a source with two cross-connected simple-mirrors, without resistors, one of the transistors having thicker gate oxide. The output to the charge is achieved by simple-mirror branch which may affect the thermal behaviour. The reference current is small, 0.43µA, the circuit can be supplied by 2.5V, is conceived in 0.8 µm process and occupies a very small area on the chip. The current-temperature variation is very poor: 0.6%/$^{o}$C, because the circuit does not include any thermal compensation, and the parameters supply and load regulation have good values: SR=5000ppm/V, LR=1455ppm/V.

Work [4] (2005) introduces a CRS with two cross-connected current mirrors: a modified-Widlar type and a "reverse"-Widlar one, having second-order thermal compensation of the branch current. This work is very important because it initiates a new CRS category. It has the merit of premeditated introduction of branch-current-ratio dependence against temperature and thus, of finding a very simple solution for second-order thermal compensation. The proposed CRS achieves a 14µA-order current and attains good performance in the

maximum current variation against temperature (0.35% in a 100°C range, see the first row in Table 1). The scheme does not assure a current output which may deteriorate the performances. It exhibits a supplied current which is a multiple of the reference current. The circuit is simulated for the BiCMOS 0.35 μm process and does not require a start-up circuit. Including resistors, the source shows an exaggerated current total variation with the process and temperature: 60%. In the simulation, this work does not took into consideration the body effect of some transistors and does not present any types, values and dimensions for the components. Being a reference work for our research in the CRS domain, the paper [4] will be critically analysed in detail in Section 2.

In paper [5] (2008) a new compact scheme of branch CRS is proposed, composed of two cross-connected current mirrors: a modified-Wilson and a Widlar one. This kind of source may be connected to the charge only by a supplementary mirror branch. There, the first- and second-order-thermal-compensation conditions were determined. The design of this CRS and the simulation results are presented. The source performances with second-order thermal compensation are: a maximum current variation against temperature of 0.9% in the temperature range of 0-100 °C and a SR parameter of 4550ppm/V. Later on, these performances have been improved [6], attaining a maximum current variation against temperature of 0.43%, SR of 2740ppm/V, LR of 750ppm/V and a current total-variation against the process and temperature of only 7,5% (see row 2 , Table 1).

Papers [7], [8] and [9] (2008) introduce and use the principle of "**total**"-current reference source (TCRS), which consists of the employment, as a reference current, of the sum of currents in two branches of cross-connected mirrors (that is the scheme total current). This kind of CRS may make use of first- and second-order thermal compensations. These works deal with two circuit variants. Theirs major advantages are: simple serially interconnection with the charge and a minimum supply current (this is just the reference current).

Section 2 presents the first- and second-order-thermal-compensation conditions for the reference current achieved in some schemes with cross-connected current mirrors. Section 3 shows a first variant of TCRS and its performances, determined by simulation for different types of integrated resistors. Then, Section 4 includes a second variant of TCRS and its performances. The conclusions are summarized in Section 5.

## 2 Thermal Compensation in CRS with Cross-Connected Mirrors

Paper [4] has the merit of raising the bid of simple and compact current sources with cross-connected mirrors, as performing CRS. There, the first-order thermal compensation of a **branch** current (fig.1) has been introduced for the first time. Then, there has also first been forced a consistent temperature dependence on the two-branch-current ratio m. Then, this permitted the source to be designed, as composed of a cross-connected modified-Widlar mirror (completed by a "diode") and a "reverse"-Widlar mirror, with the goal of achieving a spectacular second-order thermal compensation for one branch current ($I_1$). This fact led to very good thermal performances. In work [4] the manner of conducting the reference current to a charge having a grounded end or a supplied end, is not shown or discussed. Of course, this current may be transmitted to the charge by a supplementary current-mirror branch but, as shown in [6], the current ratio of this new mirror is affected by temperature, too. So, the output reference current should have, in some proportion, a compromised stability in comparison with the performance obtained on a source branch. In addition, a simple

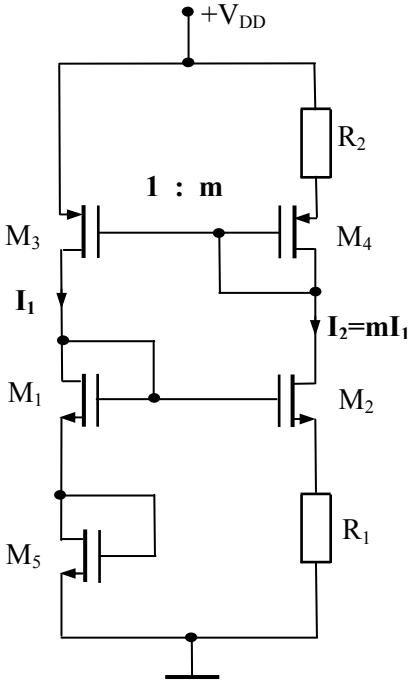


Fig.1 Second-order temperature compensation branch-current reference (Fiori-Crovetti)

supplementary branch cannot always assure good-value SR and LR parameters for the output circuit.

The supply current of the complete CRS scheme will be a super-unity multiple of the reference

current and it may have a great value if ratio m>>1 (a desired situation, when the resistor $R_1$ value, and thus the occupied on chip area is more reduced).

Having considered the temperature dependence of branch-current ratio m, in [4], they have obtained the expression of the first-order temperature coefficient of the current $I_1$, $k_{I1}$ :

$$k_{I1}=\frac{\left(2k_{VTn}+k_{\mu n}\right)V_{Tn}-\left(2k_{R1}+k_{\mu n}+2k_m\right)mI_1R_1-2k_m\sqrt{\frac{mI_1}{\beta_n\alpha_2}}}{V_{Tn}+mI_1R_1} \quad (1)$$

where $k_{VTn}$ , $k_{\mu n}$ , $k_{R1}$ and $k_m$ are the first-order temperature coefficients of quantities $V_{Tn}$ , $\mu_n$ (NMOS transistor parameters), $R_1$ and m, while $\beta_n$ and $\alpha_2$ are the gain factor and the aspect ratio of transistor $M_2$. The calculus of $k_m$ , valid when $R_2$ is used, is shown in [4]:

$$k_m=\frac{\left(1-\sqrt{\sigma m}\right)}{\sqrt{\sigma m}-2}\left(k_{\mu p}+2k_{R2}\right) \quad (2)$$

where $\sigma=\alpha_3/\alpha_4$ (with $\alpha_3$ and $\alpha_4$ – the aspect ratios of transistors $M_3$ and $M_4$), $k_{\mu p}$ and $k_{R2}$ are the first-order temperature coefficients of quantities $\mu_p$ (PMOS transistor parameter) and $R_2$.

Theoretically, this temperature coefficient becomes zero ($k_{I1}=0$) if the "first-order-thermal-compensation condition" is fulfilled:

$$R_1=\frac{V_{Tn}}{mI_1}\cdot\frac{k_{\mu n}+2k_{VTn}-2\gamma k_m}{k_{\mu n}+2k_{R1}+2k_m} \quad (3)$$

where:

$$\gamma=\frac{1}{V_{Tn}}\sqrt{\frac{mI_1}{\beta_n\alpha_2}} \quad (4)$$

Because the first-order temperature compensation did not assure good-enough performances for the CRS (especially the current variation against temperature) the authors of [4] have introduced the second-order thermal compensation with the help of ratio m temperature dependence. The "second-order-thermal-compensation condition" inferred in [4] has the expression:

$$k_{\mu n\mu n}+2k_{VTnVTn}-2\gamma k_{mm}-\gamma k_m\left(k_m-k_{\mu n}\right)+k_{VTn}\left(2k_{VTn}+2k_{\mu n}\right)-$$
$$-\left(k_{\mu n}+2k_{VTn}-2\gamma k_m\right)\cdot\left(k_m+k_{R1}+\frac{k_{\mu n\mu n}+2k_{mm}+2k_{R1R1}}{k_{\mu n}+2k_m+2k_{R1}}\right)=0 \quad (5)$$

where the coefficients with repeated indices are the second-order temperature coefficients of quantities appearing as indices (defined as derivatives against temperature of the respective first - order coefficients). The coefficients $k_{VTn}$ and $k_{\mu n}$ are negative while $k_{R1}$ can be positive, zero or negative, depending on the $R_1$-integrated-resistance used type [6]. Here, $k_m$ is positive, as the second-order-thermal-compensation condition claims, and is achieved with this sign thanks to the reverse-Widlar - type superior mirror (fig.1). As a consequence, the temperature-coefficient fraction in relation (3) is positive for the used BiCMOS process. The calculus for $k_{mm}$, valid when $R_2$ is used, is done in [4]:

$$k_{mm}=\frac{2\sqrt{\sigma m}\left(1-\sqrt{\sigma m}\right)}{\left(\sqrt{\sigma m}-2\right)^3}\left(0.5k_{\mu p}+k_{R2}\right)^2+$$
$$+\frac{\left(1-\sqrt{\sigma m}\right)}{\sqrt{\sigma m}-2}\left(k_{\mu p\mu p}+2k_{R2R2}\right) \quad (6)$$

where the second-order temperature coefficients of $\mu_p$ and $R_2$ , $k_{\mu p\mu p}$ and $k_{R2R2}$ were introduced.

We consider the second - order - thermal - compensation condition is not always fulfilled, this fact depending especially upon the $R_1$- and $R_2$-temperature-coefficient signs ($k_{R1,}$ respectively $k_{R2}$, the latter being comprised in the $k_m$ and $k_{mm}$ formulas).

The CRS performances, established by simulation in [4], are: maximum current variation against temperature 0.41% in the range of -30…+100°C (0.35% in a range of 100°C), minimum supply voltage $V_{DDmin}$=2.5V, SR=4000ppm/V (for a supply voltage not specified), and a current total variation against the process and temperature of 60% for an occupied on chip area of 4200μm$^2$ (see row 1 in Table 1).

But these performances are obtained for a scheme internal branch ($I_1$) without current extracting for an external charge and without considering the body effect of transistors $M_1$ and $M_2$ [4], facts which could alter the performances. The reported performances are good to very good excepting the maximum current variation against the process and temperature, which is unacceptable. This may be improved by increasing the resistance width on the chip to the detriment of the occupied area.

Another important deficiency in work [4] is the absence of the commentary about the value and type of resistances $R_1$ and $R_2$ and the value of branch-current ratio m, which essentially affects the scheme performances: the minimum supply voltage, the total supply current, the occupied on chip area and the total current variation against the process and temperature. There, the numerical data for the scheme and transistors are completely missing, so that the obtained results could be verified.

Another **branch** CRS using two cross-connected current mirrors (with self-biasing) has been launched in paper [5]. The newly proposed source is given in fig.2. It is composed of an inferior modified-Wilson-type mirror (with $M_1$, $M_2$, $R_1$) and a superior normal-Widlar-type mirror (with $M_3$, $M_4$, $R_3$), which are cross-connected. The scheme without the resistance $R_3$ is a classical (known) one. With the help of the resistance $R_3$ one can achieve here

the second-order thermal compensation of the branch current $I_1$.

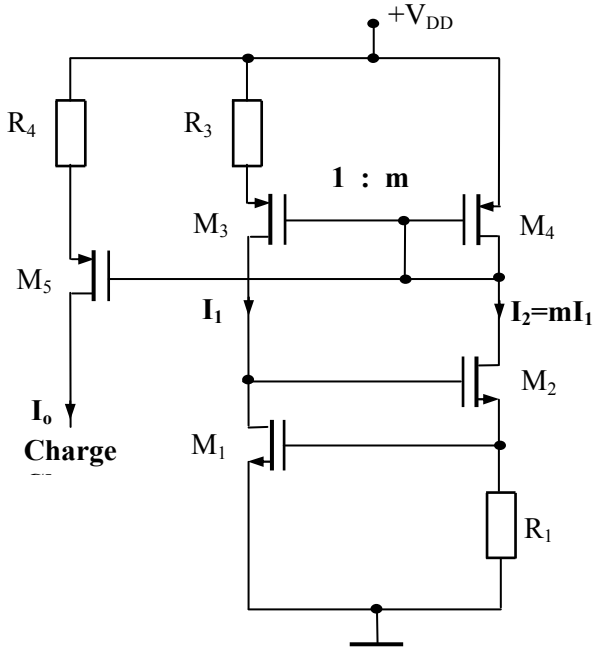


Fig.2 Second-order-thermal-compensation branch-current reference

Then a simple solution is used, to extract the reference current as $I_o$ [5] and inject it in a grounded-end charge. Achieving the supplementary branch (mirror) so that the second-order thermal compensation is preserved, the reference-current stability performances may be even improved relatively to those of two-branch scheme (Table 1).

If one imposes here the first-order-thermal-compensation condition for the current $I_1$, $k_{I1}=0$, the needed value of resistance $R_1$ results:

$$R_1 = \frac{V_{Tn}}{mI_1} \cdot \frac{k_{\mu n} + 2k_{VTn}}{k_{\mu n} + 2k_{R1} + 2k_m} \tag{7}$$

which is similar to condition (3). In order to achieve a current $I_1$ second-order thermal compensation in the case when the $R_1$ temperature coefficient is positive, here a normal-Widlar-type superior mirror ($M_3$, $M_4$, $R_3$) is used, unlike the scheme in fig.1, where the superior mirror ($M_3$, $M_4$, $R_2$) is of a reverse-Widlar type.

Here, the second-order-thermal-compensation condition for the current $I_1$ in fig.2 is:

$$k_{\mu n \mu n} - \left(k_{\mu n} + 2k_{VTn}\right)\left(k_{VTn} + k_{R1} + k_m + \frac{k_{\mu n \mu n} + 2k_{R1R1} + 2k_{mm}}{k_{\mu n} + 2k_{R1} + 2k_m}\right) = 0 \tag{8}$$

The calculus of $k_m$ and $k_{mm}$, valid when $R_3$ is used, is given in [5] and [8]:

$$k_m = \frac{\sqrt{\sigma m} - 1}{\sqrt{\sigma m} + \left(\sqrt{\sigma m} - 1\right)\frac{m}{1+m}} \cdot \left(k_{\mu p} + 2k_{R3}\right) \tag{9}$$

$$k_{mm} = \frac{\left(\sqrt{\sigma m} - 1\right)\left[\frac{1}{2}\sqrt{\sigma m} - \left(\sqrt{\sigma m} - 1\right)^2 \frac{m}{(1+m)^2}\right]}{\left[\sqrt{\sigma m} + \left(\sqrt{\sigma m} - 1\right)\frac{m}{1+m}\right]^3} \cdot \left(k_{\mu p} + 2k_{R3}\right)^2 + \frac{\sqrt{\sigma m} - 1}{\sqrt{\sigma m} + \left(\sqrt{\sigma m} - 1\right)\frac{m}{1+m}}\left(k_{\mu p \mu p} + 2k_{R3R3}\right) \tag{10}$$

In relation (8) the first term is a negative quantity while the parenthesis product gives a positive quantity. Thus, the above second-order-thermal-compensation condition may be carried out for a particular value pair of m and $\sigma=\alpha_3/\alpha_4$, (with $\alpha_3$ and $\alpha_4$ – the aspect ratios of transistors $M_3$ and $M_4$) but not for any sign of $R_1$ and $R_2$-resistance temperature coefficient. In [5] the fulfilling of condition (8) is certified for $k_{R1}>0$, $k_{R2}>0$. Thanks to Wilson mirror, which presents a strong negative feedback, some of CRS performances are much improved, especially the current total variation against the process and temperature (see the row 2 in Table 1).

Papers [6], [7], [8] and [9] propose two compact self-biased CRS, based on cross-connected current mirrors, which deliver a "**total**" reference current, representing the sum of two branch currents. It is a new concept which allows a very simple, serial interconnection of TCRS with the charge having grounded or supplied end. Such scheme assures some good performances related to maximum current variation in a given temperature range, the supply current, the parameter SR (the same as LR), and, in some cases, the minimum supply voltage.

A first variant of TCRS, shown in fig.3 [8], is partially or completely similar to that in fig.1 [4]. The source is composed of an inferior modified-Widlar type mirror and a superior normal-Widlar type (fig.3a) or reverse-Widlar type (fig.3b). The first-order thermal compensation of the total current $I_t$ is obtained with the help of the diode $M_5$ and the resistor $R_1$, while the second-order thermal compensation of $I_t$ is achieved by the superior Widlar mirror [8]. This technique has been discovered in [4] where was used for the branch current $I_1$.

The first-order-thermal-compensation condition for the current $I_t$ in fig.3 leads to resistance $R_1$ calculus relation:

$$R_1 = \frac{1+m}{m} \cdot \frac{V_{Tn}}{I_t} \cdot \frac{k_{\mu n} + 2k_{VTn} + yk_m}{k_{\mu n} + 2k_{R1} + zk_m} \tag{11}$$

Here are written

$$y=\frac{m}{1+m}+\frac{1}{x}\sqrt{\frac{m}{\alpha_2}} \quad , \quad z=\frac{2+m}{1+m}+\frac{1}{x}\sqrt{\frac{m}{\alpha_2}} \tag{12}$$

which use the supplementary notation

$$x=\frac{1}{\sqrt{\alpha_1}}+\frac{1}{\sqrt{\alpha_5}}-\sqrt{\frac{m}{\alpha_2}} \tag{13}$$

where $\alpha_1$, $\alpha_2$ and $\alpha_5$ are the aspect ratios of transistors $M_1$, $M_2$ and $M_5$.

Then, the second-order-thermal-compensation condition for the current $I_t$ has the expression [8]:

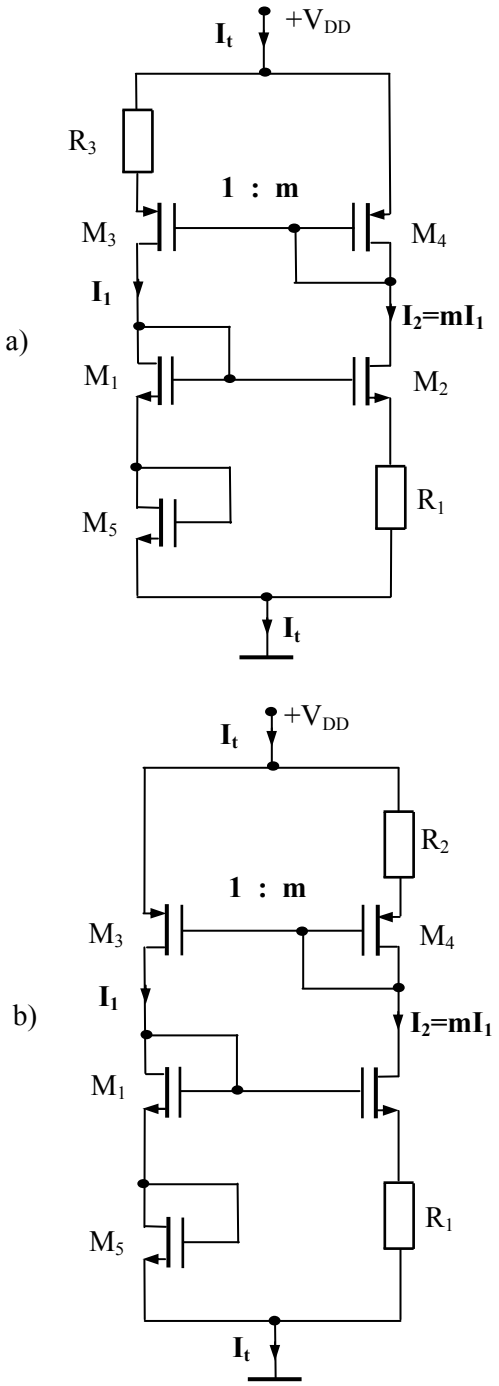


Fig.3 First variant of second-order-thermal-compensation TCRS

$$\left(k_{\mu n}+2k_{VTn}+yk_m\right)k_{VTn}+k_{\mu n\mu n}+uk_m^2+yk_{mm}- \\ -\frac{k_{\mu n}+2k_{VTn}+yk_m}{k_{\mu n}+2k_{R1}+zk_m}\left[\frac{1}{1+m}\left(k_{\mu n}+2k_{R1}+zk_m\right)k_m+k_{\mu n\mu n}+\right. \\ \left.+2k_{R1R1}+wk_m^2+zk_{mm}+\left(k_{\mu n}+2k_{R1}+zk_m\right)k_{R1}\right]=0 \tag{14}$$

where y and z are the notations (12) and

$$u=\frac{m}{(1+m)^2}+\frac{m}{2x^2\alpha_2}+\frac{1}{2x}\sqrt{\frac{m}{\alpha_2}} \\ w=-\frac{m}{(1+m)^2}+\frac{m}{2x^2\alpha_2}+\frac{1}{2x}\sqrt{\frac{m}{\alpha_2}} \tag{15}$$

The calculus of $k_m$ and $k_{mm}$ is given by relations (9) and (10), when the resistance $R_3$ is used (fig.3a) or by (2) and (6), when the resistance $R_2$ is used (fig.3b). In relation (14), the values of y, z, u, w being usually positive, the first row gives a positive quantity while the products in the second and third rows give negative quantities. Thus, the second-order-thermal-compensation condition may be fulfilled for a particular value pair of m, $\sigma=\alpha_3/\alpha_4$, and sign of temperature coefficients $k_{R1}$ and $k_{R2}$. In [8] the condition fulfilling is certified for $k_{R1}>0$, $k_{R2}>0$. In Table 1 one can see the cases when $R_3$ (fig.3a) or $R_2$ (fig.3b) is used.

The second variant of TCRS is shown in fig.4 [9] and is partially similar to the one given in fig.2 [5]. It is composed of an inferior modified-Wilson-type current mirror and of a superior normal-Widlar-type (fig.4a) or reverse-Widlar-type one (fig.4b).

The first-order thermal compensation of the total current $I_t$ may be obtained by means of resistance $R_1$ while the second-order thermal compensation – by means of the superior Widlar mirror [9]. The type of this last mirror depends on the resistance-$R_1$-temperature-coefficient sign (see rows 8-10 in Table 1). The two thermal-compensation conditions are:

$$R_1=\frac{1+m}{m}\cdot\frac{V_{Tn}}{I_t}\cdot\frac{k_{\mu n}+2k_{VTn}+\frac{m}{1+m}k_m}{k_{\mu n}+2k_{R1}+\frac{2+m}{1+m}k_m} \tag{16}$$

and

$$k_{\mu n\mu n}+\frac{m}{(1+m)^2}k_m^2+\frac{m}{1+m}k_{mm}-\left(k_{\mu n}+2k_{VTn}+\frac{m}{1+m}k_m\right)\cdot \\ \cdot\left[-k_{VTn}+k_{R1}+\frac{1}{1+m}k_m+\frac{k_{\mu n\mu n}+2k_{R1R1}-\frac{m}{(1+m)^2}k_m^2+\frac{2+m}{1+m}k_{mm}}{k_{\mu n}+2k_{R1}+\frac{2+m}{1+m}k_m}\right]=0 \tag{17}$$

The calculus of $k_m$ and $k_{mm}$ is similar to the one given in [8] when the resistance $R_3$ is used (fig.4a) or in [4], when the resistance $R_2$ is used (fig.4b). In relation (17) some terms give negative quantities

and others give positive ones. Thus, the above second-order-thermal-compensation condition may be fulfilled for a particular-value pair of m and $\sigma=\alpha_3/\alpha_4$, and sign of temperature coefficients $k_{R1}$ and $k_{R2}$. In [9] the condition fulfilling is certified for $k_{R1}>0$, $k_{R2}>0$ while in [6] – for $k_{R1}=0$, $k_{R2}>0$. In Table 1, one can find the cases when $R_3$ or $R_2$ is used.

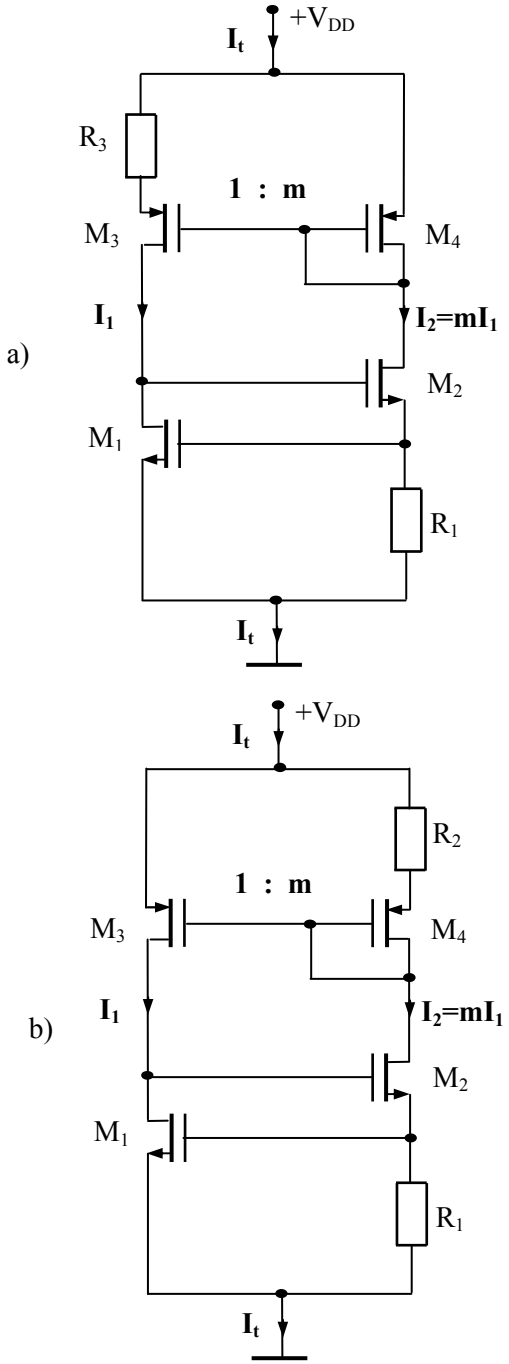


Fig.4 Second variant of second-order -thermal-compensation total RCS

Analyzing the above relations (3), (7), (11) and (16), of a similar form, we get the following important observations:

a) The $R_1$-resistance value depends on branch-current-ratio value, m, and, in all cases, the greater m is, the lower $R_1$ value gets. In practice, m=4…5 could be used.

b) The $R_1$-resistance value is directly proportional to the temperature-coefficient fraction and, considering the coefficient signs, to reduce that, it is necessary that the temperature coefficient of $R_1$, $k_{R1}$, be as small as possible, a negative value of this one being the most propitious. Thus, for a CMOS-0.35μm process, a $N^+$-diffused resistor has a positive temperature coefficient (PTC) and the fraction value tends to 3. For a polysilicon resistor with the temperature coefficient close to zero (ZTC) the fraction tends to 1.6 and for a doped $N^+$ polysilicon resistor, having a negative temperature coefficient (NTC), the fraction comes near to 0.9.

c) One may find out that, for the similarly achieved reference current, in the case of branch CRS the resistance $R_1$ value is approximately 1+m times lower than in the case of total CRS. In exchange, in the first case the supply current is 1+m times greater than the reference current. The resistance $R_1$ growth has the only advantage of source-output-resistance increasing, translated into the parameter SR improvement. But a greater resistance value leads to increased occupied on chip area.

d) If in the $R_1$ relations the factor $mI_1$, respectively $(m/1+m)I_t$ are moved to the left side, one obtains here just the drop voltage on $R_1$, and the voltage $V_{Th}$ multiplied by the temperature-coefficient fraction evaluated above remains on the right side. As a consequence, depending on the type of the integrated resistor $R_1$, the drop voltage on this will be, respectively, of order: $3V_{Tn}$ , $1.6V_{Tn}$ and $0.9V_{Tn}$. Thus, for $V_{Tn}=0.8V$, it leads to an approximate drop voltage of: 2.4V, 1.28V or 0.72V. This will determine the minimum supply-voltage value, $V_{DDmin}$, which has already been reported to be respectively: 4,6V in [5], [6], [7], [8], [9], 3,4V in [6] and 2,5V in [4], as the used resistor $R_1$ was of type PTC, ZTC or NTC (Table 1).

Related to previously given second-order-thermal-compensation conditions (5), (8), (14), (17), one does the following comments:

e) The analytic finding of the situation when the condition is fulfilled was applied in the case of using a PTC-type $R_1$ resistor [8]. This included a complicated and inexact iterative calculus. But the simulations have confirmed the possibility of achieving a second-order thermal compensation in this case.

f) In the cases of ZTC or NTC resistor the possibility of achieving an efficient (optimal)

second-order thermal compensation has been verified by simulation only, in [6] and in this work. The conclusion is a very important one: practically, it is not possible to be always successful in second-order thermal compensation for the fourth scheme given in fig.1…4. The reason is the sign and value of the coefficients $k_{R1}$ and $k_{R2}$ or $k_{R3}$ (the last two intervening in the $k_m$ and $k_{mm}$ formulas), which have an important effect in the second-order-thermal-compensation conditions. For the resistances $R_2$ or $R_3$ in the CRS presented it is not always possible to use any type of PTC, ZTC or NTC because of the important reduction effect on the temperature-coefficient value $k_m$. This may lead to the impossibility to achieve the second-order thermal compensation, as will be seen in the following sections (Table 1).

## 3 TCRS-First-Variant Performances

TCRS first variant has the scheme given in fig.3 [6], [7], [8]. Its performances, for CMOS 0.35μm process, have been evaluated by simulation and presented in the rows 3…7, Table 1. Considering the commentaries in Section 2, one used in turn a PTC, ZTC and NTC resistor $R_1$ and in each case – different types of resistor $R_2$ or $R_3$, trying the second-order thermal compensation. The reference current has been established at a value of 14-16μA, close to that used in paper [4], so that the obtained performances may be correctly compared. Although there are in all 18 resistor-temperature-coefficients combinations, as can be seen in columns 2 and 3 of Table 1, the second-order thermal compensation of total current was successful in 5 cases only. The transistor dimensions used in the simulated circuits are shown in Table 2 (ratios W/L in μm).

On the basis of the minimum supply-voltage value (row 1, Table 1), one can infer that paper [4] used a resistor $R_1$ of NTC type. The occupied on chip areas (column 10, Table 1) have been evaluated considering resistors of a 2μm width. Of course, an increase of the resistor width could lead to the lowering of current variation against process and temperature, detrimental to the occupied on chip area. For the cases in rows 3 and 4 in Table 1, one finds a maximum current variation just a little greater than the one reported in reference paper [4], for the temperature range of 0…100°C (calculated again for the same temperature range). In both cases, the parameter SR has a lesser performance than the one reported in [4]; still, it can be improved only by increasing the occupied on chip area. For an area close to that of [4] the scheme corresponding to row 4 shows a lower current total variation with the process and temperature.

The variants in rows 4, 5 and 6 in Table 1 reach better maximum current variation with temperature, even much better than the source in [4]. Thus, the performance of TCRS in row 6, of 0.017%, is placed close to the best one reported in paper [10], but obtained by complex circuits and not including an output branch (which still may deteriorate the performance). The current total variation with the process and temperature in these three cases, of 31-32%, is nearly half the one reported in reference paper [4]. The parameter SR for situations as those given in rows 6 and 7 may be once again improved by increasing the transistor cannel widths, having a reserve available here (column 10, Table 1), as compared to paper [4]. The increase of transistor width W leads to a reduction of minimum supply voltage, too. The very small occupied on chip area for TCRS in row 7 is due to great square resistance for the NTC-type resistor. The minimum supply voltage corresponds to the case of row 7, for NTC-type resistance $R_1$, as discussed in the above section.

To prove some of those performances, in fig.5 there is the graph of the reference current against chip temperature for the TCRS case of row 6. Fig.6 presents the graph of the reference current against the supply voltage for the same case.

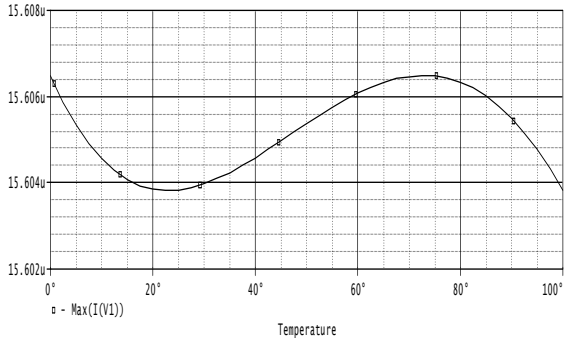


Fig.5 Reference-current variation against temperature in the range 0-100°C for TCRS in row 6

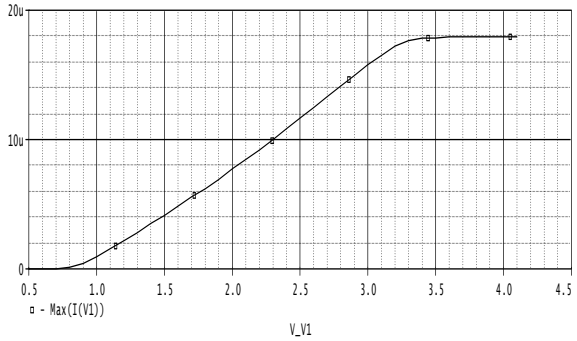


Fig.6 Reference-current variation against supply voltage for TCRS in row 6

Table 1. CRS known and news variants with second-order thermal compensation

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| | Reference current source | Resistor $R_1$ type and value [kΩ] | Resistor $R_2$ or $R_3$ type & value [kΩ] | m | Maximum current variation (0-100°C) [%] | Minimum supply voltage [V] | Parameter SR / supply voltage [ppm/V] | Parameter LR / charge voltage [ppm/V] | Process & temperature current variation [%] | Chip area [μm²] |
| 1 | Branch Widlar-Widlar [4] | (NTC) | $R_2$ | | 0,35 % (without body effect) | 2.5 | 4000 (supply voltage lack) | **Lack of output for charge** | 60 | 4200 |
| 2 | Branch Wilson-Widlar [6] | PTC 240 | $R_3$-PTC 53.3 | 1 | 0,43 | 4.6 | 2740 / 5V | 750 /1V | 16.3 7.5 | 5500 10700 |
| 3 | Total Widlar-Widlar [8] | PTC 268 | $R_3$-PTC 42.5 | 2 | 0,40-0,45 | 4.5 | 7690 /5V | Same as SR | 56 | 16500 |
| 4 | Total Widlar-Widlar [6] | ZTC 90 | $R_3$-PTC 45 | 5 | 0,42 | 3.6 | 9400 / 4V | Same as SR | 38 | 4500 |
| **5** | **Total Widlar-Widlar (new)** | **PTC 110** | **$R_3$-NTC 44** | **4.8** | **0.055** | **3.3** | **3900 / 4V** | Same as SR | **31.6** | **6300** |
| **6** | **Total Widlar-Widlar (new)** | **ZTC 120** | **$R_2$-NTC 3.356** | **4.2** | **0.017** | **3.3** | **7600 / 4V** | Same as SR | **31** | **3300** |
| **7** | **Total Widlar-Widlar (new)** | **NTC 100** | **$R_2$-NTC 17.6** | **2** | **0.2** | **2.7** | **6300 / 4V** | Same as SR | **32.5** | **800** |
| **8** | **Total Wilson-Widlar (new)** | **PTC 175** | **$R_3$-PTC 60** | **12** | **0,31** | **4.4** | **3200 / 5V** | Same as SR | **45** | **12500** |
| 9 | Total Wilson-Widlar [6] | ZTC 90 | $R_3$-PTC 45 | 5 | 0,47 | 3.4 | 3900 / 4V | Same as SR | 57 | 4.500 |
| **10** | **Total Wilson-Widlar (new)** | **NTC 82** | **$R_2$-NTC 18.8** | **2.8** | **0.21** | **2.6** | **3840 / 3.5V** | Same as SR | **12.5** | **1550** |

Table 2. Transistor aspect ratios (W/L in μm) for CRS in Table 1

| | Circuit | $M_1$ | $M_2$ | $M_3$ | $M_4$ | $M_5$ |
|---|---|---|---|---|---|---|
| 1 | Branch Widlar-Widlar [4] | | | | | |
| 2 | Branch Wilson-Widlar [6] | $\frac{2}{20}$ | $\frac{2}{5}$ | $\frac{25}{5}$ | $\frac{3.6}{5}$ | $\frac{3.6}{5}$ |
| 3 | Total Widlar-Widlar [8] | $\frac{2.1}{5}$ | $\frac{4.2}{5}$ | $\frac{14.1}{5}$ | $\frac{8}{5}$ | $\frac{0.35}{4.1}$ |
| 4 | Total Widlar-Widlar [6] | $\frac{0.8}{5}$ | $\frac{3.2}{5}$ | $\frac{1.88}{5}$ | $\frac{5.6}{5}$ | $\frac{0.35}{4.1}$ |
| **5** | **Total Widlar-Widlar** | $\frac{2.1}{5}$ | $\frac{8.4}{5}$ | $\frac{10}{5}$ | $\frac{20}{5}$ | $\frac{0.35}{1.225}$ |
| **6** | **Total Widlar-Widlar** | $\frac{3.2}{5}$ | $\frac{25}{5}$ | $\frac{6}{5}$ | $\frac{36}{5}$ | $\frac{0.35}{1.306}$ |
| **7** | **Total Widlar-Widlar** | $\frac{2.1}{5}$ | $\frac{17}{5}$ | $\frac{6.2}{5}$ | $\frac{68.5}{5}$ | $\frac{1.035}{0.35}$ |
| **8** | **Total Wilson-Widlar** | $\frac{0.35}{19.7}$ | $\frac{18}{5}$ | $\frac{40}{5}$ | $\frac{120}{5}$ | |
| 9 | Total Wilson-Widlar [6] | $\frac{1}{2.71}$ | $\frac{2}{5}$ | $\frac{2.54}{5}$ | $\frac{7.2}{5}$ | |
| **10** | **Total Wilson-Widlar** | $\frac{0.593}{0.4}$ | $\frac{24}{5}$ | $\frac{6}{5}$ | $\frac{145}{5}$ | |

In fig.7 there is shown the graph of the reference current against chip temperature for the TCRS case of row 7. Fig.8 presents the graph of the reference current against the supply voltage for the same case.

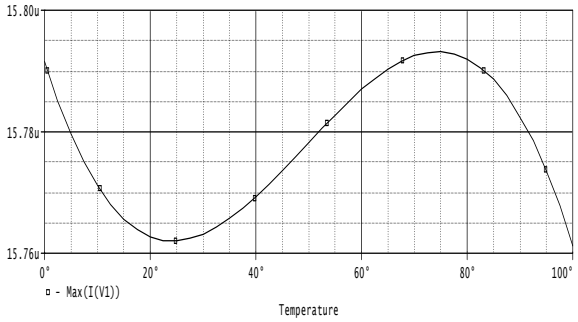


Fig.7 Reference-current variation against temperature in range 0-100°C for TCRS in row 7

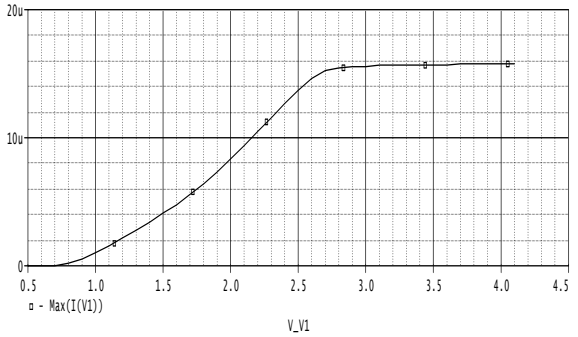


Fig.8 Reference-current variation against supply voltage for TCRS in row 7

The mention is made here that the minimum value of the maximum current variation is obtained when the graph form is close to a sine form extended over 1+1/4 periods as in fig.5 and fig.7. This form is obtained only for an optimal value of resistance $R_2$ (or $R_3$ in other cases). Using the graph in fig.6, the SR parameter (identical here to LR) could be determined, for a supply voltage specified in Table 1. The current total variation against the process and temperature, for the case of resistor widths of 2μm, has been measured by the maximum difference between current values obtained in the „*best case*" and „*worst case*" in the specified temperature range.

## 4 TCRS-Second-Variant Performance

The TCRS second variant (fig.4) uses a modified-Wilson inferior mirror [9]. Its performances, for CMOS 0.35μm process, have been evaluated by simulation and presented in rows 8…10 in Table 1. Considering the commentaries done in Section II, one used in turn a PTC, ZTC and NTC resistor $R_1$ and in each case – different types of resistors $R_2$ or $R_3$, trying the second-order thermal compensation.

The reference current has been established at a value of 14-16μA, close to that used in paper [4], so that the obtained performances may be correctly compared. Although, as in the case of Widlar-Widlar TCRS (Section 3), there are 18 resistor-temperature-coefficients combinations in all, as can be seen in columns 2 and 3 in Table 1, the second-order thermal compensation of total current was successful in 3 cases only. The transistor dimensions used in the simulated circuits are shown in Table 2 (W/L in μm).

The occupied on chip areas (column 10, Table 1) have been estimated considering resistors of 2μm width. Of course, here too, the increase of resistor width leads to lowering of current variation against process and temperature, to the prejudice of occupied on chip area.

In the case of row 9 in Table 1, a maximum current variation in the temperature range of 0…100°C can be found a little greater than was reported in reference paper [4] (calculated again for the same temperature range). In both cases, the parameters SR, the current total variation with the process and temperature and the occupied on chip area have close values. Of course, the minimum supply voltage for the cases in rows 1 and 9 differs because of the resistor $R_1$-temperature-coefficient type, being lower for the NTC type.

The variant in row 8, Table 1, presents some better performances than the reference one in row 1 regarding: the maximum current variation against temperature, SR parameter and the current total variation against process and temperature (columns 5, 7, 9 in Table 1), mainly thanks to the great value of the branch-current ratio m. But the performances regarding the minimum supply voltage and occupied on chip area (columns 6 and 10) are much poorer.

The variant in row 10 attains better and even much better performances than the reference variant in row 1 [4] to categories: maximum current variation, current total variation against process and temperature, occupied area (columns 5, 9, 10). **Based on aggregate obtained performances by the TCRS variant in row 10, we can say this is the best of all the analyzed cases.** The only category where this TCRS is overtaken by another variant is that of the maximum current variation with temperature (column 5) where the TCRS in row 6 detains a real record. In exchange, the current total variation against process and temperature of

variant 10 (column 9) is one of the best and may still be improved (to the detriment of the occupied area, where a reserve exists) by increasing the resistor width, as has been proceeded in the case of the variant in row 2. The minimum supply voltage corresponds to the case of row 10, using NTC-type resistance $R_1$. The increase of transistor width W leads to a reduction of minimum supply voltage, too. The small occupied on chip area for the TCRS in row 10 is due to great square resistance for NTC-type resistor.

To prove some of those performances, the graph of the reference current against temperature is presented in fig.9, and in fig.10 – the graph of the reference current against the supply voltage, for the TCRS case in row 10. The form close to a sine form extended on 1+1/4 periods has been obtained by optimising the value of $R_2$. With the help of the graph in fig.10 the SR parameter (identical to LR) was determined for a supply voltage specified in Table 1. The reference-current total variation against the process and temperature was determined in the same conditions as in Section 3.

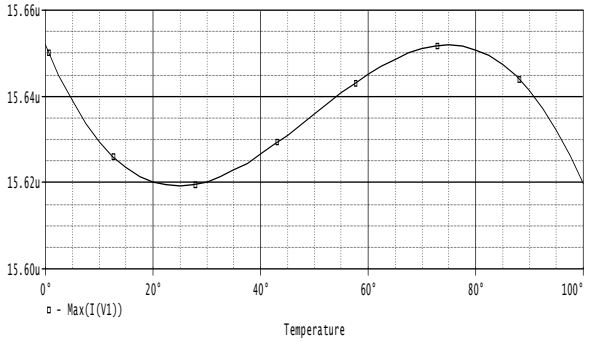


Fig.9 Reference-current variation against temperature in the range 0-100°C for TCRS in row 10

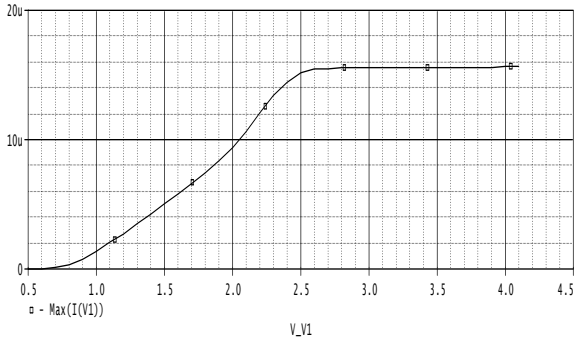


Fig.10 Reference-current variation against supply voltage for TCRS in row 10

# 5 Conclusion

In this work, the new idea of **total**-current second-order thermal compensation in a reference source (TCRS) composed of two cross-connected usual mirrors has been analyzed. This kind of source has the property of a very simple interconnection with a grounded-end or supplied-end charge, practically without affecting the current value.

The paper presents the first- and second-order-thermal-compensation conditions for the reference total current. Having the advantages of: scheme simplicity, charge connection simplicity, minimum supply current and, in some cases of variants in Table 1, good performances regarding current thermal stability, minimum supply voltage, SR (LR) parameter, current total variation against the process and temperature and occupied on chip area, the TCRS may represent a very good solution in numerous applications of analogue CMOS circuits.

This work signalled, for all CRS variants, the importance of the resistor $R_1$-temperature-coefficient value on the $R_1$ value (consequently, on the occupied on chip area) and the minimum supply-voltage value.

The verification of fulfilling the second-order-thermal-compensation condition by analytic calculus is very difficult and inexact. For this reason, the transistor dimension and resistance value finishing off has been done by simulations. Here, the $R_2$ value optimisation one sought, in view of reduction to minimum of the reference-current variation against temperature. This situation was attained when the current-graphic shape was similar to a sine segment of 1+1/4 period duration.

Although for each CRS circuit there exist 18 variants of resistance-temperature-coefficient and resistor $R_2$ or $R_3$ -use combinations, only 3…5 variants among those permitted to achieve an efficient second-order thermal compensation of the reference current, as seen in Table 1.

Especially the **record performance** of the maximum current-temperature variation in a range 0-100°C, of only 0.017%, achieved by the TCRS variant in row 6, Table 1, can be remarked, as well as the aggregate performance of the variant in row 10, too, which overtakes the performance majority in reference-paper CRS [4] (row 1, Table 1).

A good aggregate performance is also obtained by using the TCRS variant in row 7, where the performances may still be improved by increasing the branch-current ratio m and the resistor width.

As a conclusion we can say that the TCRS which use NTC-type resistors have the best aggregate performances.

Using the total-current reference leads to a single disadvantage, that of the increased $R_1$ resistance value as compared to the branch-current reference, fact which brings about the occupied-on-chip- area increase.

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