Modeling and Performance evaluation of UTB SGOI Devices scalable to 22 nm Technology node

KIRAN BAILEY[1] K.S. GURUMURTHY[2]
1 Department of ECE, BMS college of Engineering, Bangalore, INDIA
Email: kiranbailey@gmail.com
2 Department of ECE , UVCE, Bangalore University Bangalore, INDIA
Email: drksgurumurthy@gmail.com

Abstract
There is a limit for classical CMOS devices' scaling. So to keep the Moore's law in force,attempts are being made to explore the possibility of designing newer devices. These attempts are in the direction of optimizing the design for high performance and low power applications. Silicon-Germanium on Insulator (SGOI) MOSFET is one such device which has got a bright future. An Attempt has been made in this paper to design 2D SGOI MOSFET using a commercial Technology CAD (TCAD) tool. Development of SGOI based Ultra thin Body (UTB) MOSFETs are proposed in this work. Device Simulations were performed for various Gate lengths, Body thicknesses, Anti punch doping and Si cap layer doping. It was found that, for a given body thickness and gate length, increasing the Silicon cap doping and anti-punch doping, the transconductance remains unchanged while I_{off}, Drain Induced Barrier lowering (DIBL), Subthreshold slope and threshold voltages show improvement. Also, the devices with gate lengths 45nm, 32nm and 22nm demonstrate very good performance such as low leakage currents and good on current that are comparable to ITRS and hence can be implemented for sub-30 nm gate length devices. Device doping profiles have been optimized for the 22nm gate length CMOS devices to obtain minimum leakage and minimum static power dissipation. The performance of these devices has been evaluated by incorporating them in a Ring Oscillator and analyzing the circuit for static power dissipation and delay. The Ring oscillator consists of 3 inverter stages and with each inverter stage having a lumped capacitance of 6 MOSFETs.

Key-words: UTB MOSFETs, SGOI, Leakage currents, DIBL, Subthreshold Slope, Ring Oscillator (RO), TCAD.

.

1. Introduction

Scaling of Bulk CMOS is approaching Technological limits [1] and hence the need for new device architectures is growing [2] in order to continue Moore's law. Bulk CMOS scaling will face significant challenges below the 45 nm regime due to high channel doping required, band-to-band tunneling across the junction and gate induced drain leakage (GIDL), gate leakage, random doping variations and short channel effects (SCEs). Hence, high permittivity (high-k) gate dielectrics and metal gate electrodes as well as low resistance ultra shallow junctions are required in order to meet the requirements of the International Technology Roadmap for Semiconductors (ITRS). Advanced MOSFET structures such as Ultra Thin Body (UTB) Silicon-On-Insulator single gate transistors, Double Gate FETs (DGFETs) and FinFETs can be scaled more aggressively than the classic bulk-Si structure and hence may be adopted for IC production in the 25-nm physical gate length range. Metal gate electrodes will be necessary for these devices in order to provide maximum performance benefits over the bulk-Si CMOS since poly depletion effects in poly silicon gates degrade the MOS capacitance.

2. New Device structures:

2.1: Limitations to scaling: The scaling of MOSFETs is driving the industry towards major technological innovations, including material and process changes such as Metal gates and High- k dielectrics [3] and also new structures such as Ultra-Thin

Body SOI MOSFETs and FinFETs. With Scaling of planar Bulk MOSFETs, Significant challenges such as high channel doping, Junction leakage due to band-to-band tunneling and various Short channel effects (SCE) need to be addressed. Also, random doping variations [4] in the channel in extremely small MOSFETs lead to variability of threshold voltages. Gate oxide thickness cannot be scaled below a limit due to increased gate tunneling leakage current [5]. Also, V_t cannot be scaled to a large extent as off currents increase exponentially. While it may be possible to scale the traditional bulk MOSFET structure down to 25-nm channel length, a heavily doped channel will be required to control short channel effects. This impacts mobility of charge carriers in the channel leading to significant degradation in device drive current. Also with the resultant increase in electric fields in the device, reliability issues will pose a challenge. Heavy doping of the channel would also enhance the band-to-band tunneling leakage current between the drain and the body.

Abrupt halo doping profiles are desirable in the channel to localize the heavy channel doping whereas abrupt drain doping profiles are desirable for the reduction of series resistance. Together, these effects will enhance the band-to-band tunneling which would increase the off-state leakage mechanism in the transistor. However, thin body devices can control short channel effects with only the intrinsic doping in the channel. Thus, these tradeoffs can be avoided and a significant improvement in the performance can be expected.

In the UTB and Double Gate (DG) devices [6]-[9], short channel effects can be controlled by a thin silicon film, thus allowing for gate length scaling down to the 10 nm without the use of channel dopants. With a lightly doped channel, DG and Ultra Thin Body devices have negligible depletion charge and capacitance, which yield a steep subthreshold slope. Lower transverse electric field and negligible impurity scattering contribute to increased mobility that further improves the drive current in both the devices. Also, the enhancement in drive current at a given off state current specification leads directly to an improvement in the gate delay. Therefore, below the 45 nm technology node, the novel devices such as DGFETs and FinFETs have to be considered as alternative devices.

In the Nanoscale CMOS devices, Short Channel effects (SCE) have to be addressed. To counter the SCEs, a high doping of the channel is employed which degrades the mobility of the carriers in the channel due to scattering. The reduced mobility affects the drive current thus taking away the advantage of scaling. Biaxially strained Silicon by the growth of Silicon on Silicon Germanium (SiGe) [10] results in improved mobility and the use of Silicon Germanium on Insulator (SGOI) reduces SCEs. A possible alternative to continued scaling of planar MOSFETs is the fully depleted Ultra-thin body (UTB) Silicon-on Insulator (SOI) devices [11]-[13] with Silicon-Germanium (SiGe) Channel for improved mobility. Ultra Thin body (UTB) SOI devices have very thin body thickness so the gate control of the channel may be good, but the source/drain series resistance increases, leading to reduced drive currents [14]-[15]. The $Si_{0.7}Ge_{0.3}$ channel for the UTB devices improves mobility of the carriers and thereby addresses this problem. In comparison with the Standard SOI MOSFETS, the structure of the SiGe channel SGOI devices has a Silicon Cap on either side of the channel to provide better interface with the oxide [16] as shown in Fig.1.

The excellent performance characteristics of the SGOI MOSFETs with scaling have been reported in this paper. The SGOI devices are Modeled using Synopsys Technology CAD (TCAD) tool within the context of optimizing for device design. Different gate length devices at 45 nm, 32 nm and 22nm are reported.

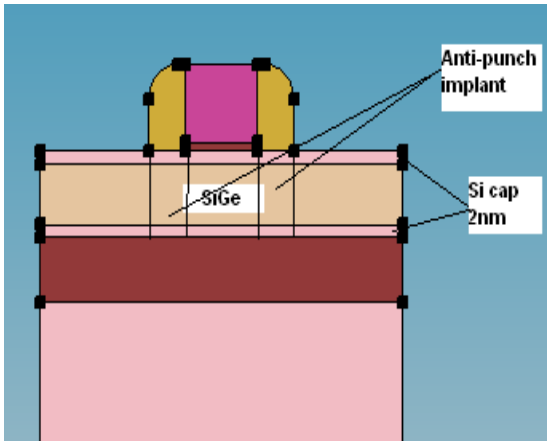


Fig 1. UTB SGOI devices with L_G=22 nm and Si Cap layers 2nm thick.

3. SGOI structure and Device Design

Synopsys Sentaurus structure and device simulators have been used in this work since the mainstream 2D TCAD tool [17]-[19] has been well calibrated to all advanced CMOS logic technologies. The critical steps in the device design are i)the formation of SiGe channel of 15-30 nm over a buried oxide approximately of 150 nm thick; ii) Thin Silicon cap layers on either side of the channel (approximately 2-4 nm thick) provides for better interface properties with the oxide layer; iii) An anti-punch doping in the Source/ Drain extension regions give excellent immunity to Short Channel effects(SCEs); iv) Lightly Doped Drain(LDD) implants and Nitride Spacer formation; v) PolySilicon gate formation with a thin layer of gate oxide (0.9-1 nm) and vii) Source/ Drain Implants.

Device simulations have been performed using the Hydrodynamic model taking into account the Ge mole fraction, Bandgap narrowing effects, Schokley-Read-Hall (SRH) recombination and Auger recombination processes. Off current I_{off} was defined at Vgs = 0.0V and Vds=1.0 V and I_{on} was defined at Vgs=Vds=1.0V.

Circuit Realization:

The performance of the UTB SGOI devices has been evaluated by implementing the devices in the basic inverter circuit comprising of a PMOS and an NMOS device with 22 nm gate length.

The NMOS transistor is optimized by varying the source drain extension Anti punch (AP) doping for minimum sub threshold leakage current. The aim is to control SCEs and thereby control leakage currents thus optimizing for minimum static power dissipation. The Saturation drain current for both NMOS and PMOS reduces linearly due to the increase in threshold voltage, but at the same time the Leakage current reduces exponentially with the increase in AP doping concentration. Thus, the AP doping is limited by the power supply-to-threshold voltage ratio (V_{dd}/V_t). The optimal values of source and drain extension AP doping are $10^{18}/cm^3$ for both source and drain sides. A similar design approach has been adopted for the PMOS transistor. The V-I characteristics for the 22 nm gate length NMOS and PMOS devices is shown in Fig.2.

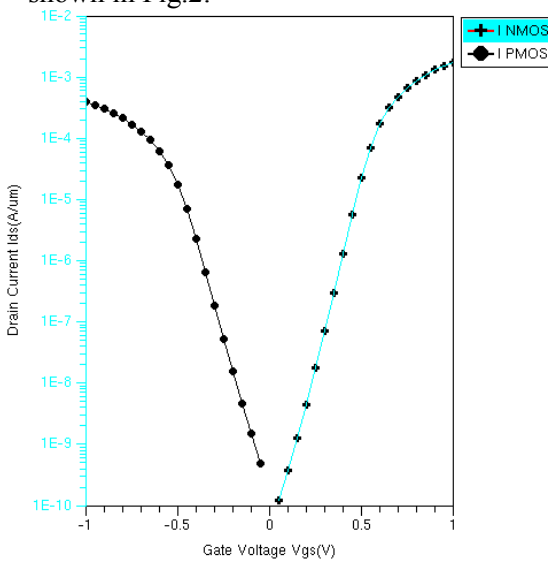


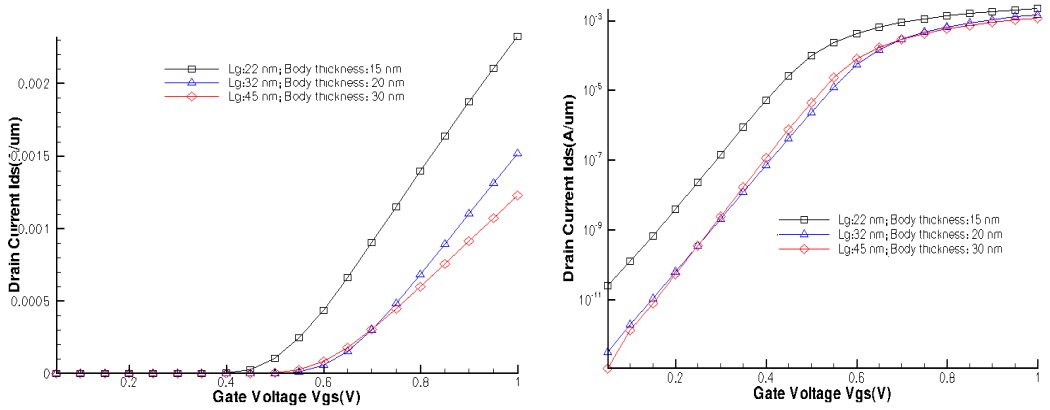
Fig 2. V-I characteristics of NMOS and PMOS devices with 22 nm gate length

4. Results and Discussion

Transfer characteristics for different gate lengths are shown in Fig.3 with body thickness as a parameter. The curves show excellent control of short channel effects due to the Anti-punch implants and high doping in the Silicon cap layers as compared to devices that do not

have doping in these regions. The SGOI body is moderately doped (1e +16/cm^3) with body thicknesses of 30nm, 20nm and 15nm for 45nm, 32nm and 22nm gate length devices respectively. Gate oxide thickness varies between 1.0 and 0.9 nm for these devices.

The use of undoped or moderately doped channel is advantageous to avoid Vt variations due to random doping fluctuations in the channel region and mobility degradation in a heavily doped channel due to Coulomb scattering. However, in undoped channels, Vth has to be controlled by other means, like modulating metal gate work function. In this work, Vt can be varied by varying the doping concentration (N_E) of the anti-punch implant in the Source/ drain extension regions.



(a) (b)

Fig. 3(a) and 3(b) Transfer characteristics for various gate length UTB SGOI devices.

Fig 4a and 4b show the variation of threshold voltage Vt with various levels of doping (N_E) and different gate lengths. Drain Induced barrier lowering (DIBL) and Subthreshold slope (SS) also varies with Doping concentration and Gate lengths as shown in Fig 5 and Fig.6. The variation of off current with the anti punch doping in the source/drain extension regions is shown in Fig 7. A high doping of the Silicon cap layers was found to improve leakage current effectively as seen in Fig.8. The transconductance (gm) was observed to remain quiet immune to variations in doping profile in the Source/drain extension regions and various gate lengths as seen in Fig.9.

Table 1 gives a comparative analysis of the UTB SGOI devices with ITRS [20] and other references.

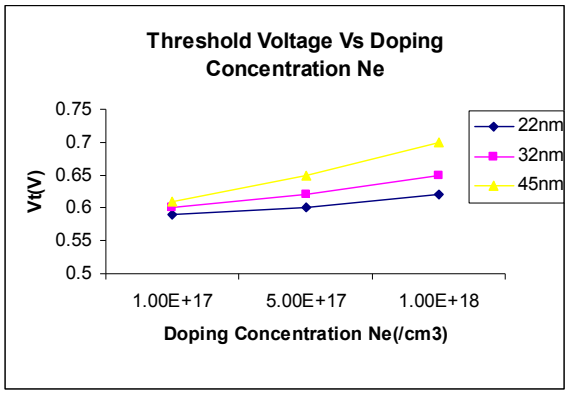


Fig. 4(a) Variation of threshold voltage with anti punch doping in the source /drain extension regions.

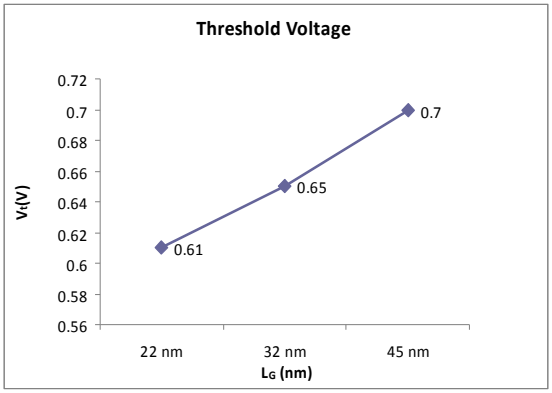


Fig.4(b) Variation of Threshold voltage with gate length.

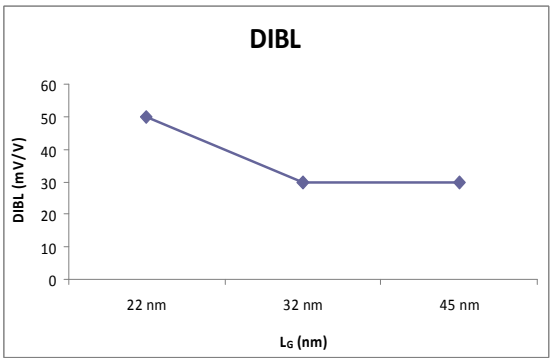


Fig.5 variation of DIBL with gate length for UTB SGOI devices.

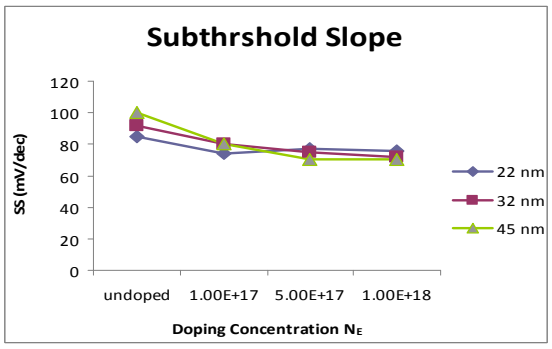


Fig. 6 Variations in Subthreshold slope for various gate length devices with doping concentration Ne.

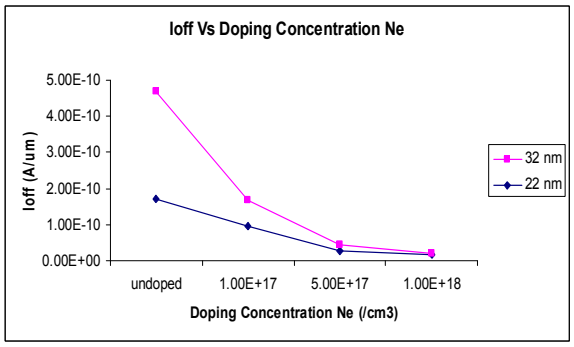


Fig. 7 The variation of I_{off} with Anti punch doping in the Source/Drain extension regions.

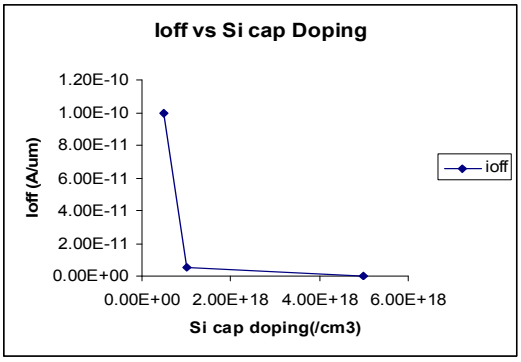


Fig.8 The doping in the Silicon cap layer effectively reduces leakage current.

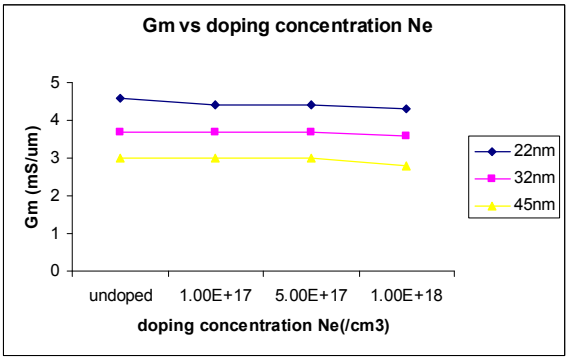


Fig. 9 Tranconductance Vs doping concentration 'Ne' for various gate lengths.

Table1 Summary of transistor parameters of this work compared with the works

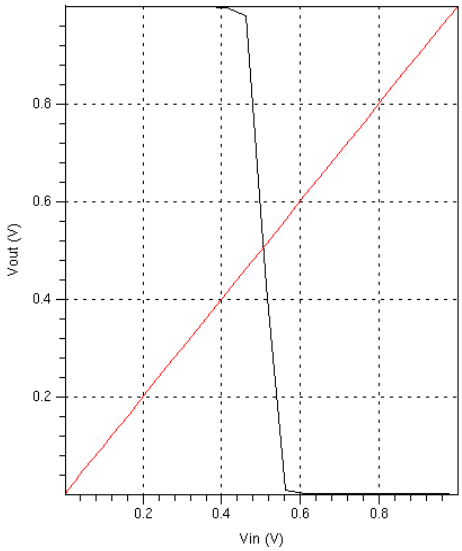
Transistor parameter	This work	This Work	This Work	ITRS HP	ITRS HP	ITRS LSTP	Ref[18] FinFET	Ref[19]	Ref[20] IEDM'01
Lg(nm)	22	32	45	22	32	45	30	35	20
Vdd(V)	1.0	1.2	1.5	1.0	1.1	1.1	1.5	1	1
Tox(nm)	0.9	0.9	0.9	0.9	1.2	1.9	2	2.4	2.1
Gate Electrode	PolySi	PolySi	PolySi	n.a	n.a	n.a	PolySi	N+ Poly	N+SiGe
Ion (uA/um)	2328	2000	1300	1513	1020	465	187.4	1240	n.a
Ioff(A/um)	26p	3p	0.3p	0.71u	0.06u	30p	3.1u	200 n	n.a
DIBL(mV/V)	60	30	30	n.a	n.a	n.a	324.34	n.a	75
SS(mV/dec)	77	72	70	n.a	n.a	n.a	121	78	100

4.1 Performance and Power

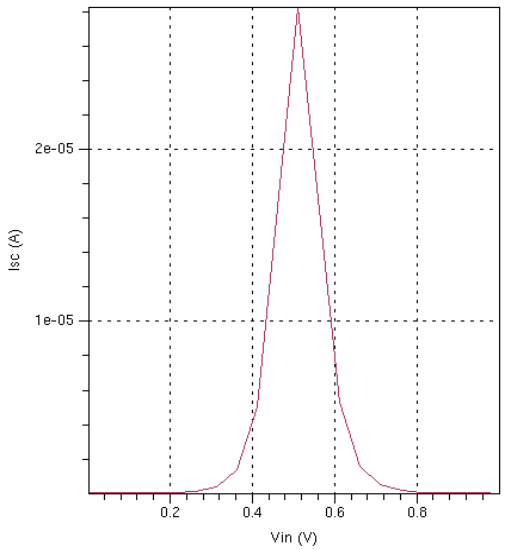
The performance of the UTB SGOI devices has been evaluated by implementing the devices in the basic inverter circuit comprising of a PMOS and an NMOS device with 22 nm gate length.

Performance and Power consumption is analyzed for a 3 stage Ring Oscillator (RO) circuit using the 22 nm gate length UTB SGOI NMOS and PMOS devices. Each stage of the RO is a CMOS inverter. The width ratio of PMOS to NMOS is 2:1 to obtain symmetrical characteristics. The voltage transfer characteristics along with the short circuit currents for the designed MOSFETs are shown in Fig.10.

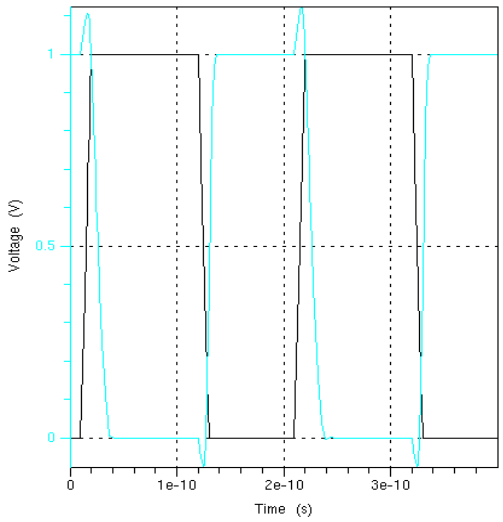
.



(a)



(b)



(c)

Fig 10. (a) Voltage transfer characteristics of CMOS inverter, (b) Short circuit current Vs input voltage in inverter. (c) Input and Output waveforms of a single stage of Inverter of RO.

A. Performance Analysis:

The Gate input capacitance calculated using C-V curves is 1.2fF. Therefore, a constant lumped capacitance of 7.2fF (for 3 stage RO) is connected to the output of each stage. The stage delay for RO is 5ps and 10ps for output rising edge and falling edge respectively simulated at a frequency of 500 MHz.

B. Power Dissipation:

The main leakage components in a transistor when it is off are the sub threshold leakage I_{sub}, Gate leakage I_{gd}, and the band-to-band tunneling leakage I_{btbt}. When the transistor is on, is main leakage component is I_{gd}. The Static power dissipation is given by

$P_{static}= (I_{sub} + I_{gd} + I_{btbt}) V_{dd}$.

Table II gives the leakage current components and total static power dissipation for the inverters in the RO.

C. Noise Margin:

The Noise Margins for the inverter are obtained from the voltage transfer curves and are given by

$NM_H=V_{OH}-V_{Sx}$

$NM_L=V_{Sy}-V_{OL}$

The values of the NM_H are 0.5 and NM_L are 0.5 respectively for the devices.

Table II. Static Power dissipation in an inverter of RO

	Input '0'			Input '1'		
	Ileak,NMOS	Ileak, PMOS	Pstatic	Ileak,NMOS	Ileak PMOS	Pstatic
UTB SGOI MOSFETs	0.16nA	0.63nA	0.79nW	0.73nA	0.53nA	1.26nW

5. Conclusion:

New devices keeping the power dissipation and performance parameters in mind, have been proposed in this paper. Various process parameters such as anti-punch doping, gate oxide thickness, Silicon cap doping have been used judiciously to design the proposed devices. The proposed devices have been simulated using commercial 2D TCAD tool. The modified device structure for SGOI UTB MOSFET has also been implemented with the similar motivation. For a given body thickness and gate length, increasing the Silicon cap doping and anti-punch doping, the transconductance remains unchanged while off current, DIBL, Subthreshold slope and threshold voltages show improvement. The 22 nm gate length devices have been used to implement the 3 stage Ring Oscillator (RO). The static power dissipation and delay have been calculated for the RO. We found out that the Anti-punch doping and Si cap doping are crucial to improve the SCEs. Thus, these structures show that they are highly scalable and it is expected that focus would shift towards these devices in the near future.

References

[1]. Taur Y, "CMOS design near the limit of scaling", IBM J Res Develop 2002, 46(2/3):213–22.

[2] Skotnicki T, Fenouillet-Beranger C, Gallon C, Boeuf F, Monfray S, Payet F, et al, "Innovative materials, devices, and CMOS technologies for low-power mobile multimedia", IEEE Trans Electron Dev 2008,55(1):96–130.

[3]. Shih-Ching Lo, Yiming Li and Jyun-Hwei Tsai, "Quantum Mechanical Simulation of High-K Dielectrics Metal-Oxide-Semiconductor structures", www.wseas.us/e-library/conferences/taiwan2004/papers/481-189.pdf

[4]. Shih-Ching Lo and Yiming Li,"Numerical simulation of Random Dopant Fluctuation in Sub-65 nm Metal-oxide-Semiconductor Field Effect Transistors", Proceedings of the 8th WSEAS International conference on Applied Mathematics, PP272-280, Dec 2005.

[5]. Shao-Ming Yu, Jam-Wem Lee and Yiming Li, "Gate tunneling current calculation of Nanoscale MOSFETS with a unified quantum Correction Spice Model", www.wseas.us/e-library/conferences/taiwan2004/papers/481-179.pdf

[6] Leland chang, Yang-Kyu Choi, Daewon HA, Pushkar Ranade, Shiying Xiong, Jeffrey Bokor, Chenming Hu and Tsu-Jae king, " Extremely Scaled Silicon Nano-CMOS Devices", Proceedings of the IEEE, Vol.91, No.11, Nov 2003.

[7] Doris B, Ieong M, Kanarsky T, Zhang Y, Roy RA, Dokumaci O, et al. "Extreme scaling with ultrathin Si channel MOSFETs", Int Electron Dev Meet 2002;1:267–70.

[8] Wei Ke, Xu Han, Dingyu Li, Xiaoyan Liu, Ruqi Han, and Shengdong Zhang, "Recessed Source/Drain for Scaling SOI MOSFET to the Limit", 1-4244-0161- 5/06©2006 IEEE

[9] K. Bernstein, D.J. Frank, A.E. Gattiker, W. Haensch, B.L. Ji, S.R. Nassif, E.J. Nowak, D.J. Pearson and N.J. Rohrer, "High-Performance CMOS Variability in the 65-nm regime and Beyond", www.research.ibm.com/ journal/rd/504/Bernstein.html

[10] M. Reiche, O. Moutanabbir, J. Hoentschel , U. Gösele, S. Flachowsky and M. Horstmann , "Strained Silicon Devices", Solid State Phenomena Vols. 156-158 (2010) pp 61-68.

[11]Suzuki E, Ishii K, Kanemaru S, Maeda T, Tsutsumi T, Sekigawa T, et al. "Highly suppressed short-channel effects in ultrathin SOI n-MOSFETs.", IEEE Transactions Electron Dev 2000;47(2):354–9.

[12] Hisamoto D. "FD/DG-SOI MOSFET – a viable approach to overcoming the device scaling limit.", Int Electron Dev Meet 2001;1:429–32.

[13] Trivedi VP, Fossum JG, "Scaling fully depleted SOI CMOS.", IEEE Trans Electron Dev 2003;50(10):2095–103.

[14] Choi CH, Goo JS, Yu Z, Dutton RW. "Shallow source/drain extension effects on external resistance in sub-0.1 lm MOSFETs". IEEE Trans Electron Dev 2000;47(3):655–8.

[15] Doris B, Ieong M, Kanarsky T, Zhang Y, Roy RA, Dokumaci O, et al. "Extreme scaling with ultrathin Si channel MOSFETs.", Int Electron Dev Meet 2002;1:267–70.

[16] Yee Chia Yeo, Vivek Subramanian, Jakub Kedzierski, Peiqi Xuan, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu, "Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel" IEEE Electron device letters, vol. 21, no. 4, April 2000.

[17] Shih-Ching Lo, Jyun-Hwei Tsai and Yiming Li, "Transport Models for Double-Gate Metal Oxide Semiconductor Field Effect Transistor Simulation". www.wseas.us/e-library/conferences/taiwan2004/papers/481-116.pdf

[18] Taib Ziad Mohamad, Ibrahim Ahmad and Azami Zaharim, "Optimum Solution in fabricating 65 nm NMOS Transistors using Taguchi method" 7th WSEAS Int. Conf. on Applied computer & Applied computational science (ACACOS '08), Hangzhou, China, April 6-8, 2008

[19] Yiming Li1, Yen-Yu Cho, Chuan-Sheng Wang, Pu Chen, and Ting-Wei Tang, "A Compact Carrier Quantization Model for Nanoscale MOSFETs Simulation". www.wseas.us/e-library/conferences/skiathos2002/papers/445-187.pdf mathematics, PP272-280, Dec 2005

[20] International Technology Roadmap for Semiconductors (ITRS) 2007 edition.

[21] Muhammad Nawaz, Stefan Deckar, Luis-Felipe Giles, Wolfgang Molzer, Thomas Schulz, " Evaluation of process parameter space of bulk FinFETs using 3D TCAD", Microelectronic Engineering 85 (2008) 1529-1539.

[22] Fu-Liang Yang, Haur-Ywh Chen, Fang-Cheng Chen, Yi-Lin Chan, Kuo-Nan Yang, Chih-Jian Chen, Hun-Jan Tao, Yang-Kyu Choi, Mong-Song Liang and Chenming Hu, " 35 nm CMOS FinFETs", 2002 Symposium on VLSI Technology Digest of Technical papers.

[23]Y.K.Choi, N. Lindert, P.Xaun, S.Tang, D.Ha, E.Anderson,et al "Sub-20nm CMOS FinFET technologies", IEDM Tech. Digest, Dec 2001, pp 421-424.Taiwan2004/papers/481-116.pdf

Kiran Bailey (1975): She completed her bachelor's degree in Electronics and Communication engineering in 1997 and her master's degree in 2001 securing II rank. She is currently pursuing research in Nanoscale CMOS devices. She is currently working as lecturer in BMS College of engineering, Bangalore. Her areas of interest include solid state devices and VLSI systems.

K S Gurumurthy (1951): K S Gurumurthy obtained PhD (1990) from IISc, Bangalore. He is currently working as a professor in the Dept. of E &CE, UVC College of Engg, Bangalore University, Bangalore. He has about 33 years of teaching experience. He is a recipient of gold medal in ME and 'KHOSLA AWARD for the best published Technical Paper from IIT ROORKEE. He is MIMAPS INDIA, MISTE and MIEEE. He has published more than 50 research papers.