Role of driver and load transistor (MOSFET) parameters on pseudo-NMOS logic design

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Abstract: The pseudo-NMOS logic can be used in special applications to perform special logic function. The pseudo- NMOS logic is based on designing pseudo-NMOS inverter which functions as a digital switch. During the design phase of pseudo-NMOS inverters and logic gates based on MOS technologies, it is necessary to take into consideration many parameters which characterise MOS transistors, which impact static and dynamic performances of the different logic gates. The aim of this paper is to research impact the NMOS (driver) and PMOS (active load) transistors parameters during the design phase of pseudo-NMOS inverters and in design phase pseudo-NMOS logic gates for different work cases. The results obtained emphasize the impact of each single parameter of MOSFET transistor at the low output level state, at the level values of static current at output, on the shape of the voltage transfer characteristic in the pseudo-NMOS inverter, on propagation delays during transition logic state, and impact in pseudo-NMOS logic gates. By adjusting the parameters values of NMOS and PMOS transistor it's possible to design pseudo-NMOS inverters and pseudo-NMOS logic gate which will have acceptable performance depending on designers' requests.

Key words: Threshold Voltage, Driver Transistor, Active Load, Device Transconductance Parameter, Voltage Level, Low Output Level, VTC- Characteristic, Static Current, Propagation Delays, Fan-In.

1 Introduction

An important value which characterizes all types of MOSFET transistors is the value of threshold voltage (V_{th} or V_t). According to the MOSFET type, the value of threshold voltage can be positive and negative. This value can be controlled during the fabrication process of MOSFET transistors, Fig. 1 [2, 3, 4, 5, 8].

The value of the threshold voltage is controlled by some physical parameters which characterize the MOSFET (NMOS) structure such as: the gate material, the thickness of oxide layer t_{ox}, substrate doping concentrations (density) N_A, oxide–interface fixed charge concentrations (density) N_{ox}, channel length L, channel width W and the bias voltage V_{SB} [1, 9, 11, 12, 13].

For nonzero substrate bias voltage ($V_{SB} > 0$), the threshold voltage is given by this expression [2, 4, 6, 7]:

$$V_t = V_{t0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right) \quad (1)$$

where V_{t0} is the threshold voltage for V_{SB} = 0 V, and ϕ_F - is the substrate Fermi potential,

γ - is a fabrication-process parameter, known as the body-effect parameter, and it is given by:

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}} \quad (2)$$

where: q - electron charge, N_A – the doping concentration of th p-type substrate, ε_{Si} – dielectric constant of silicon (S_i), C_{ox} – the gate oxide capacitance per unit area.

The value of threshold voltage will have influence on static and dynamic work regime of MOSFET transistors. The MOSFET transistors play a significant role in designing of digital circuits because of many advantages they have over the other digital families.

In many applications of digital circuits, the pseudo-NMOS logic is used in designing logic circuits where the parameter fan-in must be higher. The pseudo-

MOS logic can be used to supplement the CMOS circuits in special application. The operation of pseudo-NMOS logic is based on pseudo-NMOS inverter, which is a modified form of the CMOS inverter [6, 7, 8, 9, 16].
Other values which can be controlled during MOSFET fabrication phase are their parasitic capacitance values, values of process transconductace parameters, and device transconductance parameter [4, 14, 15, 17]. All these characteristics values will have significant role during the design phase based on pseudo-NMOS logic.

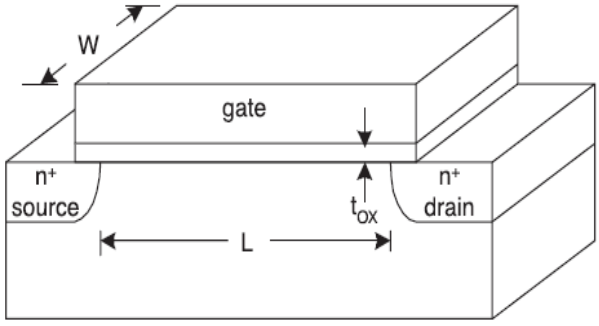

Fig. 1 The physical structure of an enhancement-type MOSFET (NMOS) in perspective view.

2 Impact of threshold voltage on pseudo-NMOS inverter

The pseudo-NMOS inverter contains two interconnected MOSFET transistors: one NMOS transistor (Q_N) which works as driver and one PMOS-transistor (Q_P) which works as an active load. The pseudo-NMOS inverter is shown in Fig. 2.

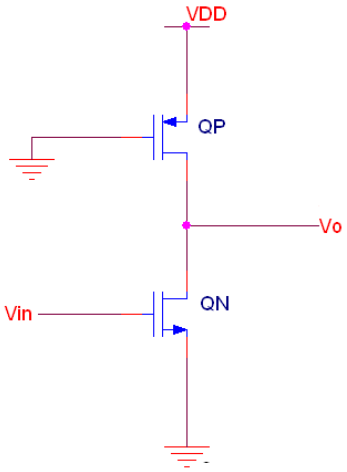

Fig. 2 Circuit structure of pseudo-NMOS inverter.

Now we will examine particularly impact of the threshold voltage of driver (NMOS) and the threshold voltage of active load (PMOS) in driver current and load current (especially in static case), low-output state, shape of VTC (voltage transfer characteristics), propagation delays and role of the load inverter (Fan-out factor) in propagation delays.

2.1 Impact of the driver threshold voltage in driver and load current

Variation of the active load current (i_{DP}) and the driver current (i_{DN}) as function of output voltage (v_O) for various values of the driver threshold voltage (Q_N), when the input voltage will have value of V_{DD} ($V_{in} = V_{DD}$, $V_{DD} = 3.3$ V) and $V_{tp0} = -0.4$ V are represented in Fig. 3, Fig. 4, Fig. 5 and Fig. 6. During these analyses the dimensions of NMOS and PMOS transistors will be the same, while the ratio of the transconductance process parameter (or device transconductance parameter) will be $k_R = 4$.

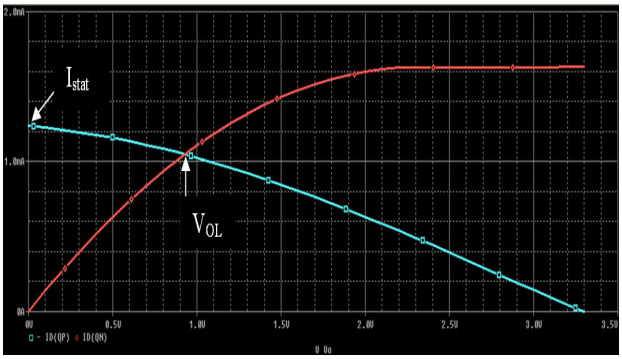

Fig. 3 Variation of load (i_{DP}) and driver (i_{DN}) current as function of output voltage (V_O) when the threshold voltage of driver is $V_{tn0} = 1$ V.

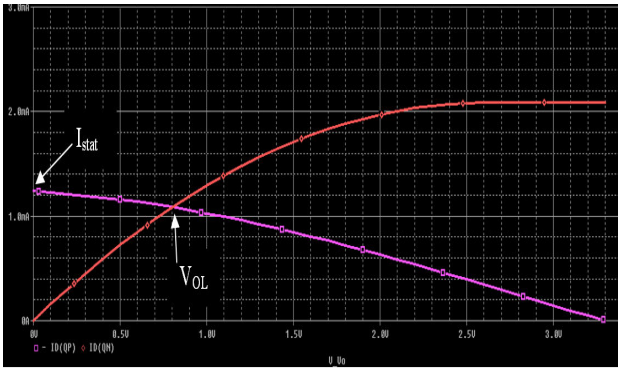

Fig. 4 Variation of load (i_{DP}) and driver (i_{DN}) current as function of output voltage (V_O) when the threshold voltage of driver is $V_{tn0} = 0.7$ V.

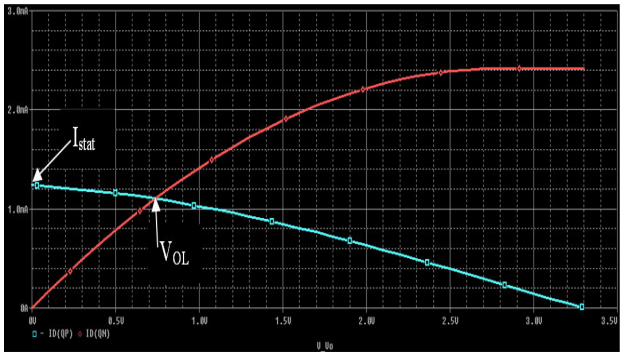

Fig. 5 Variation of load (i_{DP}) and driver (i_{DN}) current as function of output voltage (V_O) when the threshold voltage of driver is $V_{tn0} = 0.5$V.

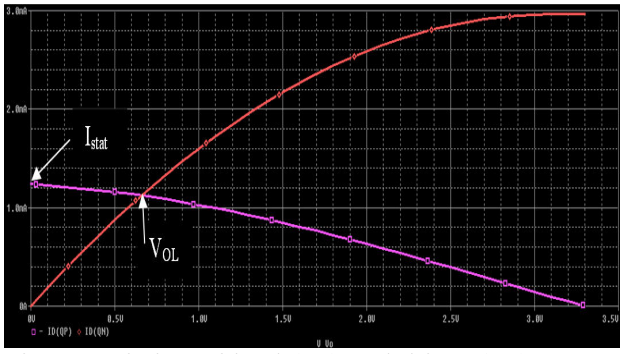

Fig. 6 Variation of load (i_{DP}) and driver (i_{DN}) current as function of output voltage (V_O) when the threshold voltage of driver is $V_{tn0} = 0.2$V.

Based on accrued resultants for Fig. 3 to Fig. 6, it can be concluded that: the static current I_{stat} for low output logic level (low output state) is independent from the values of the driver threshold voltage, whereas for different values of driver threshold voltage will have impact at the low output logic level (V_{OL}). For lower values of the driver threshold voltage, the values of the low level at output will be lower and results in best performance in digital circuits.

The non-zero value of V_{OL} is an obvious disadvantage of pseudo-NMOS inverters, which will have influence in noise margins (on noise margin for low output level). Another disadvantage is that the static current at low output state has non-zero values, and thus there will be static power dissipation [6, 8].

$$P_D = I_{stat} \times V_{DD} \quad (3)$$

2.2 Impact of the active load threshold voltage in driver and load current

Variation of load (i_{DP}) and driver (i_{DN}) current as function of output voltage (V_O) for various values of active load threshold voltage (V_{tp0}), where the input voltage and driver threshold voltage will be held at constant values ($V_{in} = V_{DD}$, $V_{tn0} = 0.4$ V) are represented in Fig. 7, Fig. 8, Fig. 9, Fig. 10.

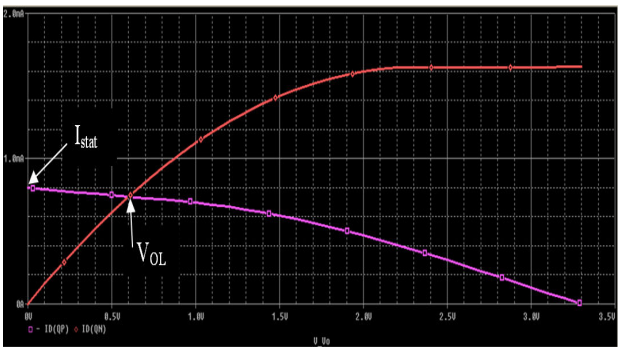

Fig. 7 Variation of load (i_{DP}) and driver (i_{DN}) current as function of output voltage (V_O) when the active load threshold voltage is $V_{tp0} = -1$ V.

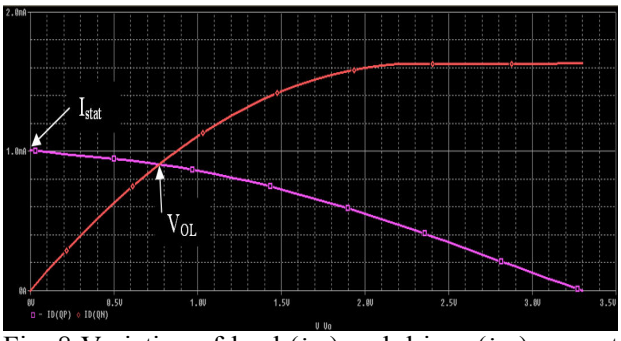

Fig. 8 Variation of load (i_{DP}) and driver (i_{DN}) current as function of output voltage (V_O) when the threshold voltage of active load is $V_{tp0} = -0.7$ V.

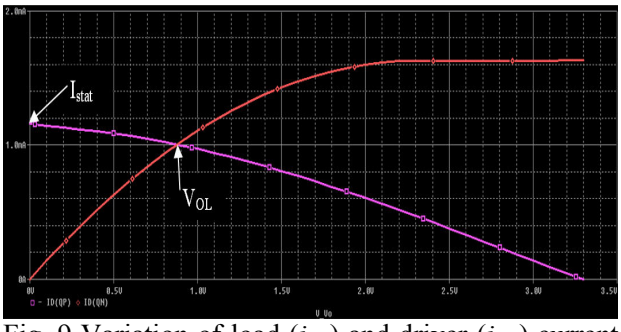

Fig. 9 Variation of load (i_{DP}) and driver (i_{DN}) current as function of output voltage (V_O) when the threshold voltage of active load is $V_{tn0} = -0.5$ V.

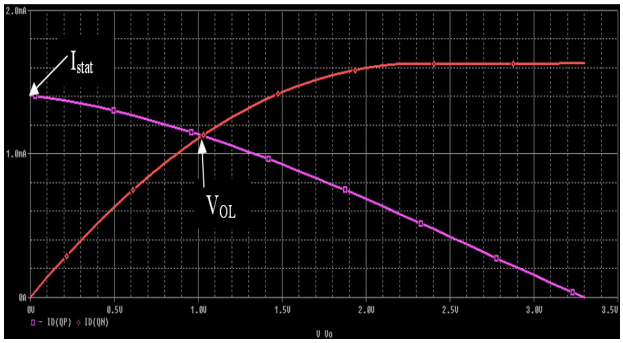

Fig. 10 Variation of load (i_{DP}) and driver (i_{DN}) current as function of output voltage (V_O) when the threshold voltage of active load is $V_{tn0} = -0.2$ V.

Based on accrued resultants for Fig. 7 to Fig. 10 it can be concluded that: the static current I_{stat} when the output is at the low logic level, it depends on the values of the load threshold voltage, and results on the lower values for higher values of active load threshold voltage, and also for higher values of load threshold voltage the value at low-output state will be lower. Also in this case the values of static current (I_{stat}) and output voltage (V_{OL}) will be disadvantages of pseudo-NMOS invertors for low-output state, which will have impact in the noise margin for low level (NM_L) and static power dissipation P_D as in Fig. 11.

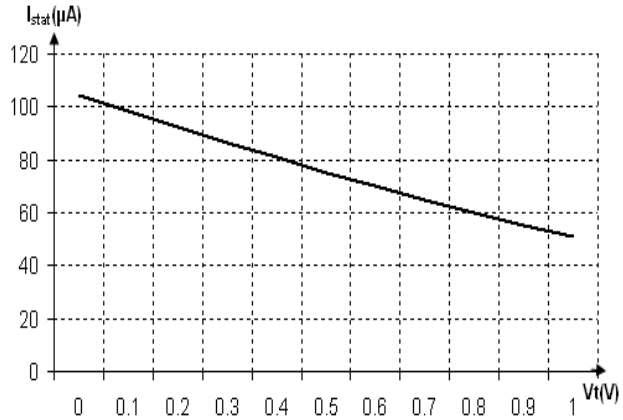

Fig. 11 Variation the I_{stat} of pseudo-NMOS inverter as function of load threshold voltage.

The values of the driver and load current will have significant role in propagations delays during transition states.

2.3 Impact of the driver and the active load threshold voltage on propagation delays

The values of threshold voltage which characterize the driver transistor (NMOS) and active load transistor (PMOS) will have influence on propagation delays in pseudo-NMOS invertors. For the examine time delays it will be used a pseudo-NMOS inverter which drives a capacitive load C_L of 0.5 pF as in Fig 12.

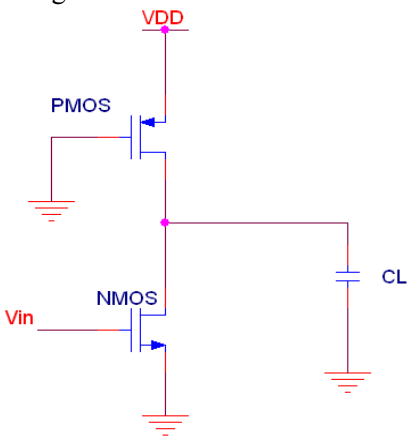

Fig. 12 The pseudo-NMOS inverter with capacitive load $C_L = 0.5$ pF.

The active load threshold voltage (PMOS) will have impact in propagation delays during the low to high transition (t_{PLH}). For two different values of the active load threshold voltage the low to high transition is represented in Fig. 13.

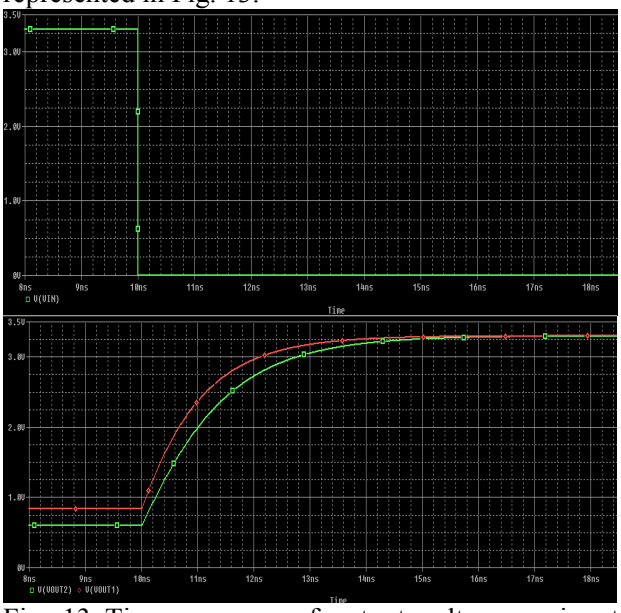

Fig. 13 Time response of output voltage on input voltage when the active load threshold voltage

(PMOS) has two different values and the driver threshold voltage (NMOS) holds fixed value of V_{tn0} = 0.7 V. The V(VOUT1) curve corresponds to the output voltage when V_{tp0} = – 0.3 V, the V(VOUT2) curve corresponds to the output voltage when V_{tp0} = – 0.7 V.

Based on accrued resultants on Fig. 13, the propagation delays will be higher for higher values of the active threshold voltage during low to high transition (t_{PLH}). Also form Fig. 13 can shown that the values of active threshold voltage has impact on low output voltage level.
In Fig. 14 there are represented the shapes of output voltages for two periods of inputs voltages when the active load threshold voltage has two different values.

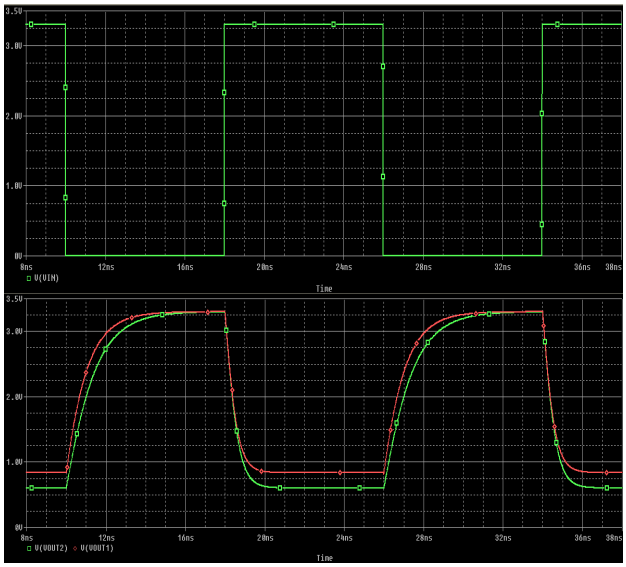

Fig. 14 Time response of output voltage for two periods of input voltage when the active load threshold voltage (PMOS) has two different values and the driver threshold voltage (NMOS) holds fixed value of V_{tn0} = 0.7 V. The V(VOUT1) curve corresponds to the output voltage when V_{tp0} = – 0.3 V, the V(VOUT2) curve corresponds to the output voltage when V_{tp0} = – 0.7 V.

Based in Fig. 14 it can be concluded that: the active load threshold voltage will have influence in values of propagation delays during low to high transition and on low output voltage level, but not any role in high to low transition.
The values of driver transistor threshold voltage (NMOS) will have influence in propagation delays during high to low transition at output voltage (t_{PHL}). In Fig. 15 it is shown the impact of the driver threshold voltage in propagation delays (t_{PHL}) when two different values of driver threshold voltage are considered as parametric value.

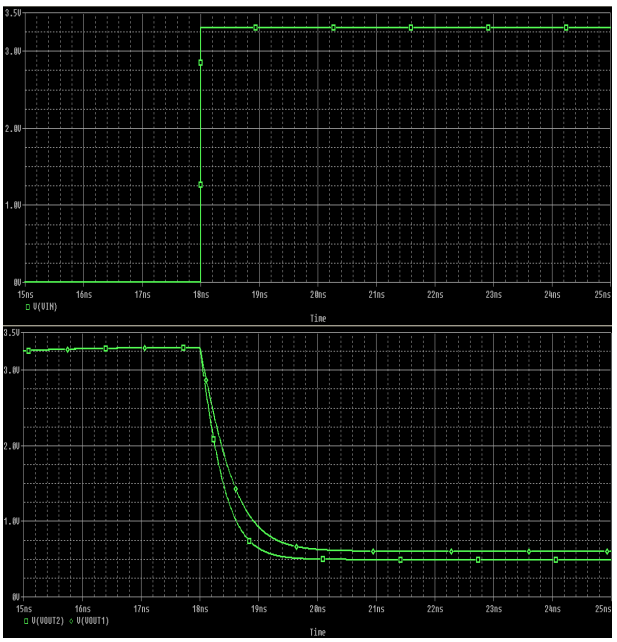

Fig. 15 Time response of output voltage on input voltage when the driver threshold voltage (NMOS) has two different values, and the active load threshold voltage (PMOS) holds fixed value of V_{tp0} = – 0.7 V. The V(VOUT1) curve corresponds to the output voltage when V_{tn0} = 0.7V, the V(VOUT2) curve corresponds to the output voltage when V_{tn0} = 0.2 V.

From the time response of the output voltage in Fig. 15 there are shown impact values of the driver threshold voltage on time delays during high to low transition at output and on low output voltage level, when pseudo-NMOS inverter is driven by input voltage. For higher values of the driver threshold voltage the propagation delays during high to low transition will be shorter, so and low output voltage level will be lower.
The time response of the pseudo-NMOS inverter when drives a capacitive load for two different values of the driver threshold voltage, and when driver input voltage has two periods is shown in Fig. 16.
Form the time response in Fig. 16 can be concluded that: the driver threshold voltage will have influence only on propagation delays during high to low

transition and on low output voltage level, but not on propagation delays during low to high transition.
From all time responses of pseudo-NMOS inverter the propagation delays during high to low transition are shorter than propagation delays during low to high transition as a result of carrier mobility in the driver transistor (NMOS), and during the design phase of inverters this must be taken into consideration.

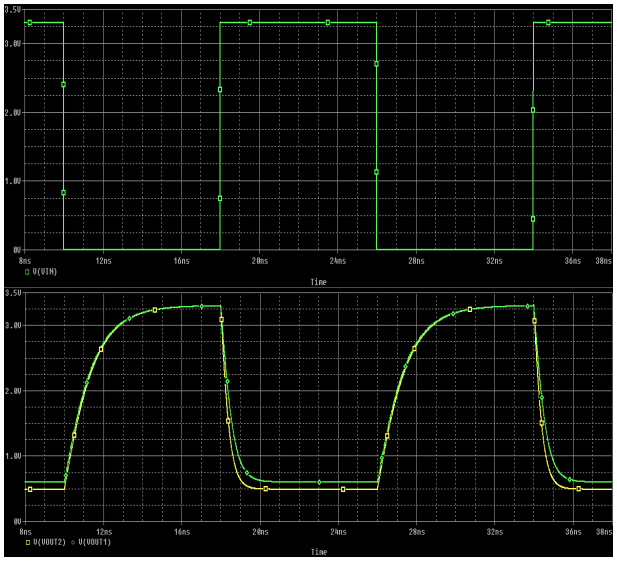

Fig. 16 Time response of output voltage for two periods of input voltage when the driver threshold voltage (NMOS) has two different values and the active load threshold voltage (PMOS) holds fixed value of V_{tp0} = – 0.7 V. The V(VOUT1) curve corresponds to the output voltage when V_{tn0} = 0.7 V, the V(VOUT2) curve corresponds to the output voltage when V_{tn0} = 0.2 V.

It's very important that: values of driver and active load transistors threshold voltage will have impact on values of propagation delays only when the capacitive load has smaller values, but when the load has higher values the impact of the threshold voltages of NMOS and PMsOS transistors haven't any significant role. The impact of the load value (or fan-out) in propagation delays for two cases and the driver threshold voltage is assumed as a parametric value are shown in Fig. 17. Same behaviour will have when the active load threshold voltage would be assumed as a parametric value.

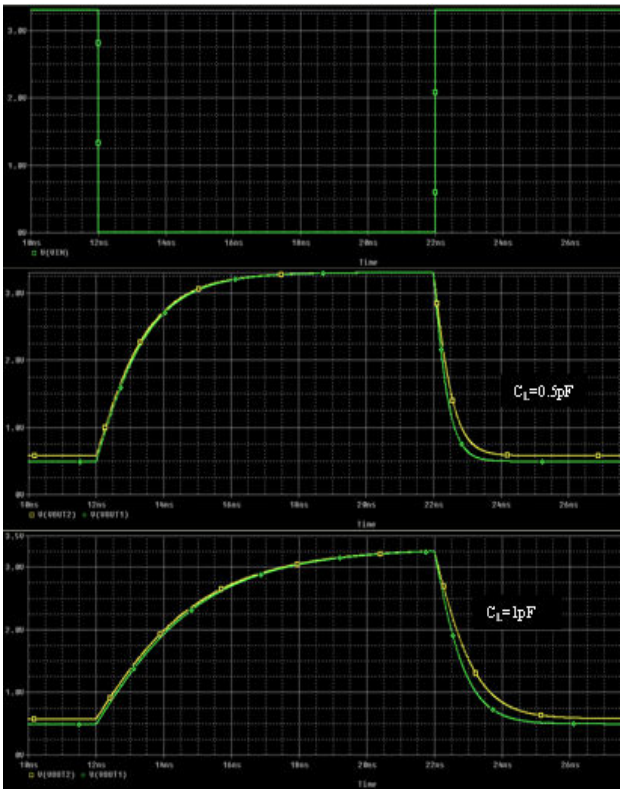

Fig. 17 The waveforms of input and output voltages for two different values of capacitive load C_L. The first case is when the capacitive load has value of C_L = 0.5 pF, and second case is when load has value of C_L = 1 pF. The driver threshold voltage has two different values of 0.6V and 0.2V, whereas the active load threshold voltage has fixed value of – 0.7V.

2.4 The role of the transconductance parameters of driver and active load transistors

An important value which must be taken into consideration during design phase of pseudo-NMOS inverters is the transconductance parameter of the driver and active load device. By controlling the trasconductance parameter of devices (of NMOS and PMOS transistors) the important parameters of pseudo- NMOS inverter can be controlled, such as: low output voltage level, propagation delays, shape of VTC, noise margin, static current and dissipation power.
The transconductance parameters devices are defined by:

$$k_n = (k' \frac{W}{L})_{driver} \quad (4)$$

$$k_p = (k' \frac{W}{L})_{active\ load} \quad (5)$$

k' - process transconductance parameter,
W,L - dimensions of channel region.

By selecting the ratio of the device transconductane parameters ($k_R = k_n/k_p$), the above characteristics values of pseudo-NMOS inverter can be adopted in dependency on applied cases. The destined parameters ratio can be achieved by selecting the wide dimensions of NMOS or PMOS transistors which contain pseudo-NMOS inverters.
The shape of the driver and active load currents, level value of static current and level value of low output state for some different values of device parameters ratio (k_R) are shown in Fig. 18.

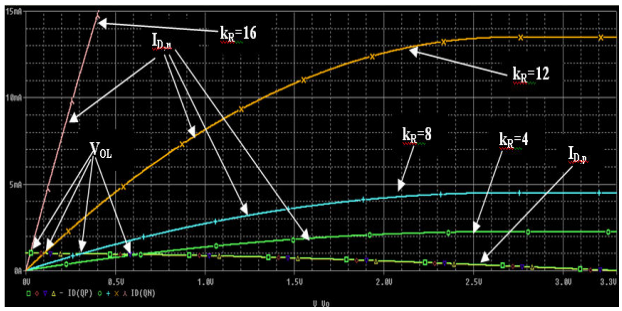

Fig.18. Varation of the driver and active load current (I_{Dn}, I_{Dp}) on output voltage (V_o), when the input driver voltage is high ($V_{in} = V_{DD}$) and the device transconductance parameters ratio has four parametric values: 4, 8, 12 and 16**.** The breakpoints between load curve (I_{Dn}) and driver current (I_{Dn}) will give the level values of V_{OL}.

The variation of the VTC characteristic on k_R as parametric values is shown in Fig. 19.

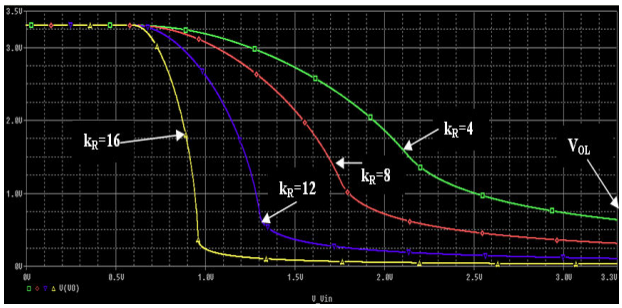

Fig.19 Input-output voltage transfer characteristic (VTC) of the pseudo-NMOS inverter, when the device transconductance parameter ratio has values of k_R = 4, 8, 12 and 16.

The Impact of device transconductance parameters ratio (k_R) on propagation delays when a pseudo-NMOS inverter drives load of C_L = 0.5 pF is shown in Fig.20.
All graphical construction to determine the impact of devices transconductance parameters ratio on the driver current, the active load current, the VTC characteristic and propagation delays during transient response in pseudo-NMOS inverter, during analysis are used these values V_{DD} = 3.3 V, V_{tn0} = 0.6 V, V_{tp0} = -0.7 V and V_{in} with max value of 3.3 V.
Based on pseudo-NMOS inverter response from Fig. 18 and Fig. 19 can be concluded as: by selecting larger value of devices tansconductance parameter ratio will results in lower values of low output state, in higher values of driver current, the higher slope of VTC characteristic. The static power is determined only by the active load device tranconductance parameter and biased voltage V_{DD}.

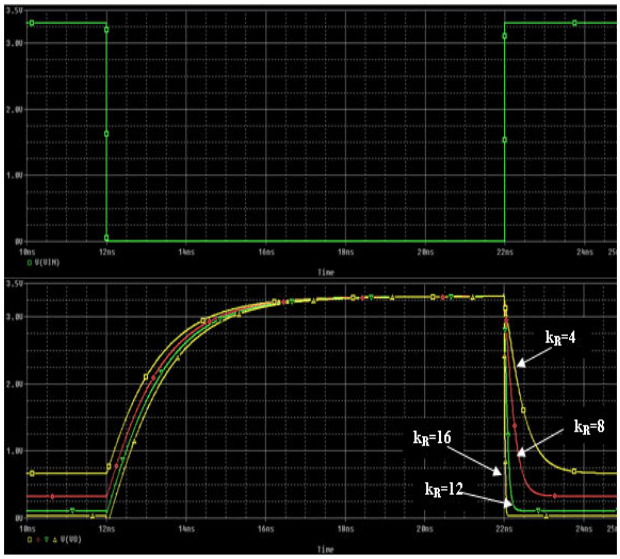

Fig. 20 Time response of output voltage on input voltage when the devices transconductance ratio has for different values of k_R = 4, 8, 12, and 16.

Based on the time response of output voltage in Fig.20, the propagation delays in inverter can be shorter if the parameter k_n by values will be higher. The higher values of k_n parameter will have significant role on propagation delays during high to low transition and low output state, but not any significant role on propagation delays during low to high transition.

The higher values of the device transconductance parameters ratio (k_R) during design phase of pseudo-NMOS inverter can be achieved by selecting the k_n parameter greater than the k_p parameter. The selection of a greater parameter k_n its possible during the design phase to design driver transistor with a wider channel (W_n) than active load transistor ($W_n > W_p$). But during the design phase of inverter must take in consideration, that the channel width of the active load transistor will have influence especially in static current and propagation delays during low to high transition. Usually, the pseudo-NMOS inverters designed with device transconductance parameters ratio are higher then four ($k_n > 4$).
Since the pseudo-NMOS inverters characteristics are in dependency on ratio of the device tranconductance parameters (k_n/k_p), such circuits are known as ratioed logic circuits, unlike the CMOS inverters which are known as ratioless logic circuits.

2.5 Impact of threshold voltage in output voltage of pseudo-NMOS gates

During the design phase of pseudo-NMOS logic circuits, designers must take into consideration the values of the threshold voltage of transistors which contain that logic gate. Firstly, it will begin with the VTC (voltage transfer characteristic) of pseudo-NMOS invertors and show its shape for the some different values of the driver threshold voltage where the load threshold voltage has same values as in Fig. 21 and Fig 22.

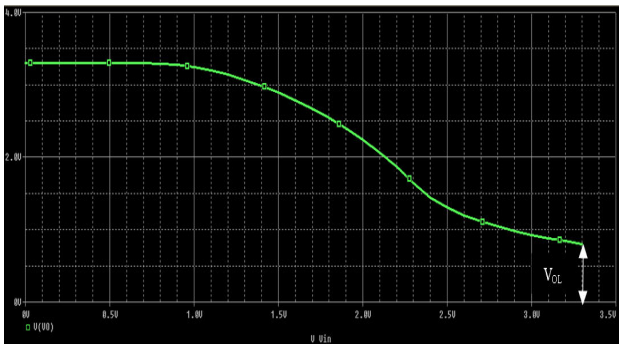

Fig. 21 Shape of VTC for pseudo-NMOS inverter when the driver threshold voltage is $V_{tn0} = 0.7$ V and active load threshold voltage is $V_{tp0} = -0.4$ V.

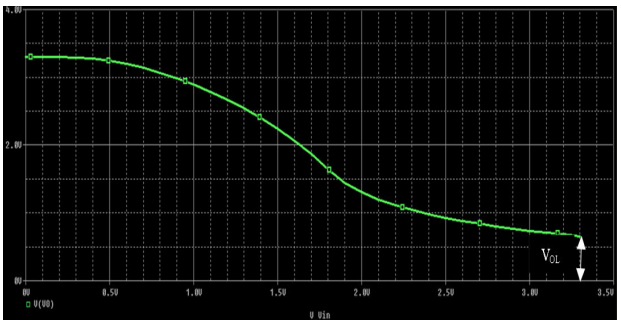

Fig. 22 Shape of VTC for pseudo-NMOS inverter when the driver threshold voltage is $V_{tn0} = 0.2$ V and active load threshold voltage is $V_{tp0} = -0.4$ V.

The value of V_{OL} and V_{OH} can be calculated using expressions:

$$V_{OH} = V_{DD} \quad (6)$$

$$V_{OL} = V_{DD} - V_{tn} - \sqrt{(V_{DD} - V_{tn})^2 - \frac{k_p}{k_n}(V_{DD} - |V_{tp}|)^2} \quad (7)$$

k_n, k_p – are the transconductance parameters of devices.
Based on Fig. 21 and Fig. 22 it can be concluded that for lower values of driver threshold voltage, there will be higher slope of VTC, which results lower propagation delay, i.e. faster operation
The NAND pseudo-NMOS structure contains NMOS transistors (drivers) in series depending on the number of inputs (fan-in) as in Fig. 23.

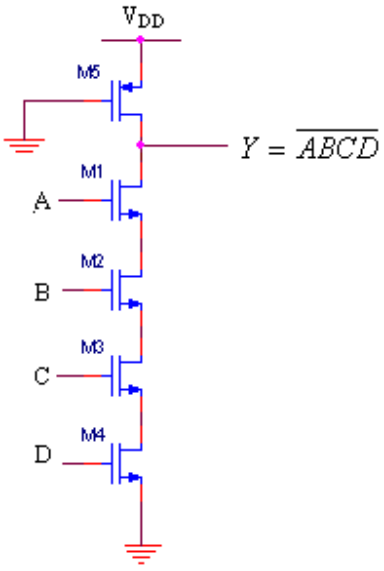

Fig. 23 NAND pseudo-NMOS gates with 4-inputs.

In the static work regime, the values of driver threshold voltages will have impact on the value V_{OL}

of NAND structure. The VTC-NAND shapes and values of V_{OL} for two different values of driver threshold voltage when fan-in has four different values are represented in Fig. 24 and Fig. 15.

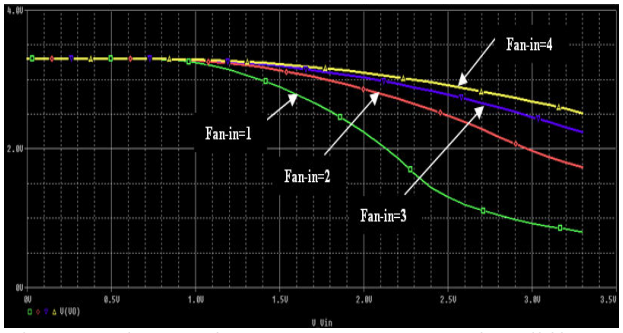

Fig. 24 Shape of VTC-NAND gates for different number inputs (fan-in) when V_{tn0}= 0.7 V.

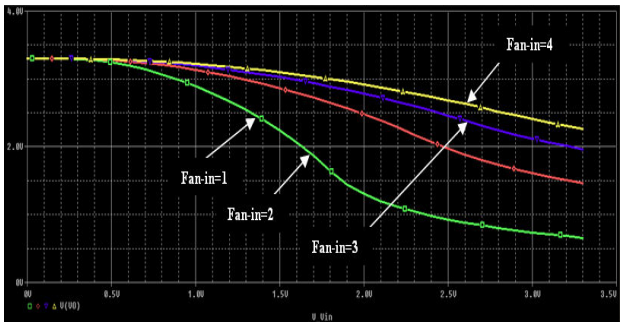

Fig. 25 Shape of VTC-NAND gates for different number inputs (fan-in) when V_{tn0} = 0.2V.

Shape and slope of characteristics from Fig. 24 and Fig. 25 show that in the NAND gate fan-in has significant role and for higher values of number inputs (fan-in) there will be lower slope of VTC and higher values for low output state. The higher values of fan-in will result in higher values of propagation delays.

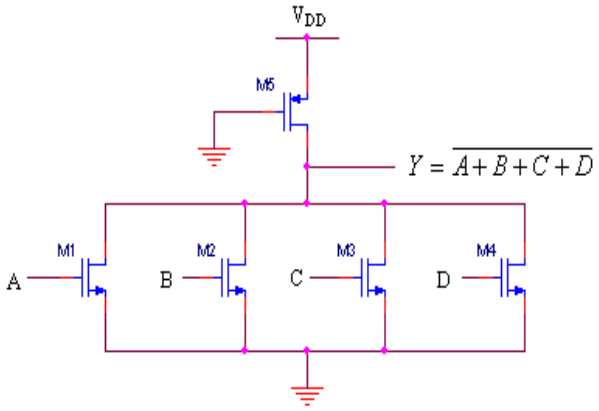

Fig. 26 NOR pseudo-NMOS gates with 4-inputs.

The NOR pseudo-NMOS structure contains NMOS transistors (drivers) in parallel depending on the number of inputs (fan-in) as in Fig. 26.
The VTC shape of NOR gate and values of V_{OL} for two different values of driver threshold voltage when fan-in has four different values are represented in Fig. 27 and Fig. 28.

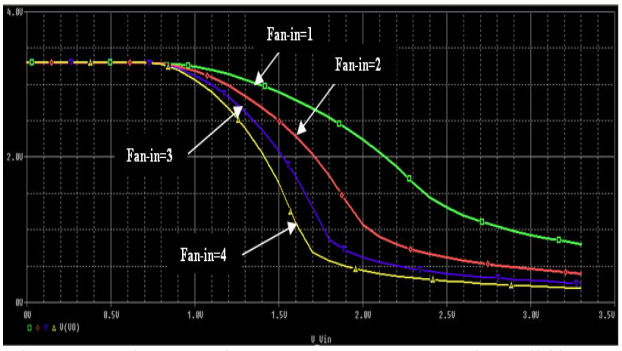

Fig. 27 Shape of VTC NOR gate for different number inputs (fan-in) when V_{tn0} = 0.7 V.

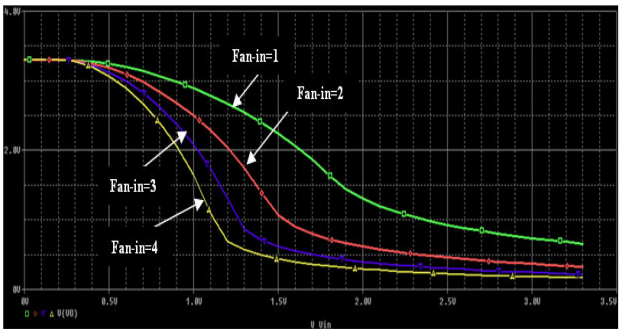

Fig. 28 Shape of VTC NAND gates for different number inputs (fan-in) when V_{tn0} = 0.2V.

Based on Fig. 27 and Fig. 28 it can be concluded: for a higher number of inputs the slope of VTC characteristics is higher and the low level values (V_{OL}) will be lower. These results show that for higher values of fan-in the propagation delays will be lower and the noise margin (for low-output state) will be higher.
From the all analyses done so far, it can be concluded that in pseudo-NMOS logic, NOR gates are preferred over NAND logic gates in static and dynamic cases.

3 Conclusions

The MOSFET technologies possibilities that the important MOSFET transistors parameters to controls during the fabrication process. By selecting

the adequate MOSFET parameters we can design digital circuits with the best performances in both static and dynamic work regime. To reduce the number of MOSFET transistors compared to CMOS technologies in special application as supplements to complementary CMOS design, it is possible to use pseudo-NMOS technologies for logic design. But, the disadvantages of pseudo-NMOS logic are: the static dissipation power for low output state and low output voltage level. Pseudo-NMOS logic is suitable for the applications in which the output remains high most of the time.

Selecting the values of the driver (NMOS) and active load (PMOS) threshold voltage we can adjust: the level of static current when output is at low stage (I_{stat}), the low output level (V_{OL}), the static power dissipation (P_D), and the shape of voltage transfer characteristics (VTC).

By selecting adequate ratio of the device tarnsconductace parameters can be adjusted the behaviour the pseudo-NMOS inverter in static and dynamic cases.

The best effectiveness in pseudo-NMOS logic design in many cases can be reached by selecting the higher values of ratio device transconductance parameters. The higher values of the ratio device transconductance parameters will result in the asymmetry on time response during high to low transition and low to high transition (propagation delays).

When designing pseudo-NMOS logic gates we can consider that the NOR pseudo-NMOS logic gate is in advantage compared to NAND pseudo-NMOS logic gate by: low output level (V_{OL}), propagation delay, noise margin for low output state (NM_L) and occupied area size.

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