Charge Equalization Based-on Three-Level NPC Converter for Series Connected Battery Strings

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Abstract: - The main purpose of this paper is to design a charge equalization circuit for series connected lead-acid batteries. The charger utilizes a three-level neutral point clamped (NPC) AC/DC converter with voltage balance control to charge the series connected rechargeable battery strings. This paper details the operation principles of the charge equalization circuit under different operation modes and derives the governed equations. The proposed charge equalization circuit can not only regulate the power factor of AC source side, but also can balance the charge voltage for series connected rechargeable batteries. Finally, some simulation results are made to demonstrate the effectiveness of the charge equalization circuit scheme presented in this paper.

Key-Words: Lead-Acid Battery, Charge Equalization Circuit, Three-Level Converter, Voltage Balance Control, Neutral Point Clamped (NPC) Converter.

1 Introduction

Lead-acid batteries play an important role in human life. In recent years, the demand for lead-acid batteries has increased due to energy shortages and problems of environmental pollution. However, as single rechargeable batteries cannot satisfy the electrical demands of many systems, generally multiple batteries are series connected into a battery pack in order to provide sufficient voltage. Nevertheless, when multiple rechargeable batteries are series connected for recharging, imbalances result in the amounts of electricity charged into the batteries due to differences in internal characteristics, and chemical components between the batteries involved. Consequently, as the number of batteries series connected in a battery pack increases, the lifespan of the batteries will decrease exponentially [1,2]. The main purpose of battery chargers is to create an equivalent state-of-charge (SOC) in each battery in a series connected battery pack. When there are unequal charges between batteries in a battery pack, high capacity batteries require less energy for recharging, while lower capacity rechargeable batteries require higher energies for recharging in order to meet the equivalent charging needs of battery packs.

Current research on charge equalization technologies can be broadly divided into extended time overcharging, consumable charge equalization scheme, inductor charge equalization scheme, switched capacitor charge equalization system, and multi-winding transformer charge equalization scheme [3-10]. The extended time overcharging method [3] involves extending the charging times for series connected battery packs. Battery packs that generally require only 12 hours for charging have their charging times extended in order to ensure that every battery within the pack is highly charged and to allow the lowest-capacity battery to meet high-capacity needs. However, this method leads to the risk of gas seepage in higher-capacity batteries. Consumable charge equalization schemes [4] connect a charge equalizer to each battery in a battery pack. These equalizers are generally composed of resistors, zener diodes, and voltage controlled current elements. When any battery in the pack exceeds a set voltage, the equalizers are activated and redirect a portion of the charging current to the equalizer, thereby reducing current flow to batteries and preventing the occurrence of overcharging. However, this method wastes a significant amount of energy on equalizers and leads to unnecessary energy loss. Inductor charge equalization schemes [5] are divided into forward and backward charge equalization schemes. The operation principle of inductor charge equalization scheme is to use switches and inductors of charge equalization sub-circuits to transfer energy of high-capacity batteries, causing the battery energies of every battery in a pack to be equalized. The shortcoming of this method is that the energy transfer is limited by the capacity of the inductors, which may lead to overly long charging times. Capacitor charge equalization schemes [6] connect linked battery packs

to a scheme consisting of bi-direction switches and capacitors. This scheme switches rapidly between switches and capacitors to transfer unequal energy between batteries, thereby reducing power difference between batteries and attaining the goal of equal charging. The shortcomings of this method are that energy transfer is limited by the energy storage capacities of the capacitors and that excessively long equal charging times may be produced. The operation principle of multi-winding transformer charge equalization schemes [7-10] lies in using DC-DC converters to charge series connected battery packs at the high-charging rate when the series connected battery packs are in a low-power state at the beginning of the charging process; when the set voltage has been reached, the batteries are switched to charging under a charge equalization mode. The charge equalization circuits of this scheme consist of a set of multi-winding transformers and a DC-DC converter. As the series connected battery packs charge each battery at identical voltages on the secondary side, the batteries are charged at identical voltages; higher-capacity batteries are charged at lower charging rates, while relatively lower-capacity batteries are charged at higher rates. Consequently, over a period of time, the capacities in each battery in a series connected battery pack will be balanced, thereby reaching the effect of charge equalization. This type of scheme faces the issues of mutual inductance and leakage inductance between mutually coupled windings. As a result, even with equal numbers of winding turns, identical charge voltages cannot be obtained.

This study presents the use of a three-level neutral point clamped AC/DC converter to directly perform constant voltage charging in order to overcome the problems with existing rechargeable battery charge equalization circuits. Not only can the converters and their control schemes cause the power factor for the AC input side to approach 1, it can also rapidly complete equal charging for series connected battery packs.

2 Three-Level Neutral Point Clamped Converter Charge Equalization Scheme

Figure 1 depicts the proposed neutral point voltage balance control three-level AC/DC converter charge equalization scheme that possesses power factor correction. So that the power voltage will obtain three-level voltage wave forms every 1 1/2 cycles, we use eight IGBT power semiconductors $S_1 - S_8$ as power switches and the neutral point clamped rectifier composed of four clamped diodes $D_1 - D_4$ [11-13]. A boosting inductor L_s is connected to the AC side as a storage inductor for power factor control; the DC side of the converter is connected to the serial battery strings, so that through the DC voltage controller, a stable DC voltage can be provided to charge the series connected battery pack. In order for the power factor of the input end to approach 1.0, the errors of DC feedback voltage $V_{dc}^{'} = K_v V_{dc}$ (K_v is the sensed voltage factor) and command voltage V_{dc}^{*} produce the peak value command $\hat{I}_{ac}^{*}$ of the input current after being regulated by the voltage controller. This value multiplied by the unit sine wave $S(\omega t)$ with the same phase as the input voltage v_{ac} produces the input current command i_{ac}^{*} . Thereafter, a hysteresis current controller (HCC) is used to produce the switching control signal for the power semiconductor, thereby causing the actual input current $i_{ac}^{'} = K_s i_{ac}$ (K_s is the sensed current factor) closely following command current i_{ac}^{*}, causing the power factor of the AC input side to approach 1.

3 Operation Principles of the Charge Equalizer

We first make the following four assumptions to analyze this charge equalization circuit for rechargeable batteries: (1)assume that all components are ideal and do not suffer from voltage drop or switching loss; (2)the characteristics of the two rechargeable batteries are identical; (3)within a short switching period, input AC voltage can be viewed as a constant value; (4)AC line resistance R_s can be ignored. For this converter, there are three possible switching states, $S_1 = S_2 = 1$ ($S_5 = S_6 = 1$), $S_2 = S_3 = 1$ ($S_6 = S_7 = 1$), and $S_3 = S_4 = 1$ ($S_7 = S_8 = 1$). Consequently, there are $3^2 = 9$ possible changes in switching modes for the three-level neutral point clamped converter switch. Three of these modes can produce zero voltage at the input end voltage v_{ab}. To save on switching states, only $S_2 = S_3 = S_6 = S_7 = 1$ zero voltage switching mode was selected. Thus, seven possible switch switching modes remain; these modes can produce five types of voltage (0 , $\pm V_{dc}/2$, $\pm V_{dc}$) levels at AC side input voltage v_{ab}. If the three-level input voltage wave form is to be obtained, the relationship between electrical input voltage v_{ac} and DC output voltage must meet the condition of $V_{dc}/2 < \left| v_{ac,\,peak} \right| < V_{dc}$. Consequently, we first designate $|v_{ac}| < V_{dc}/2$ as Area 1 and designate $|v_{ac}| > V_{dc}/2$ as Area 2; we assume that

$v_{B1} = v_{B2} = V_{dc}/2$.

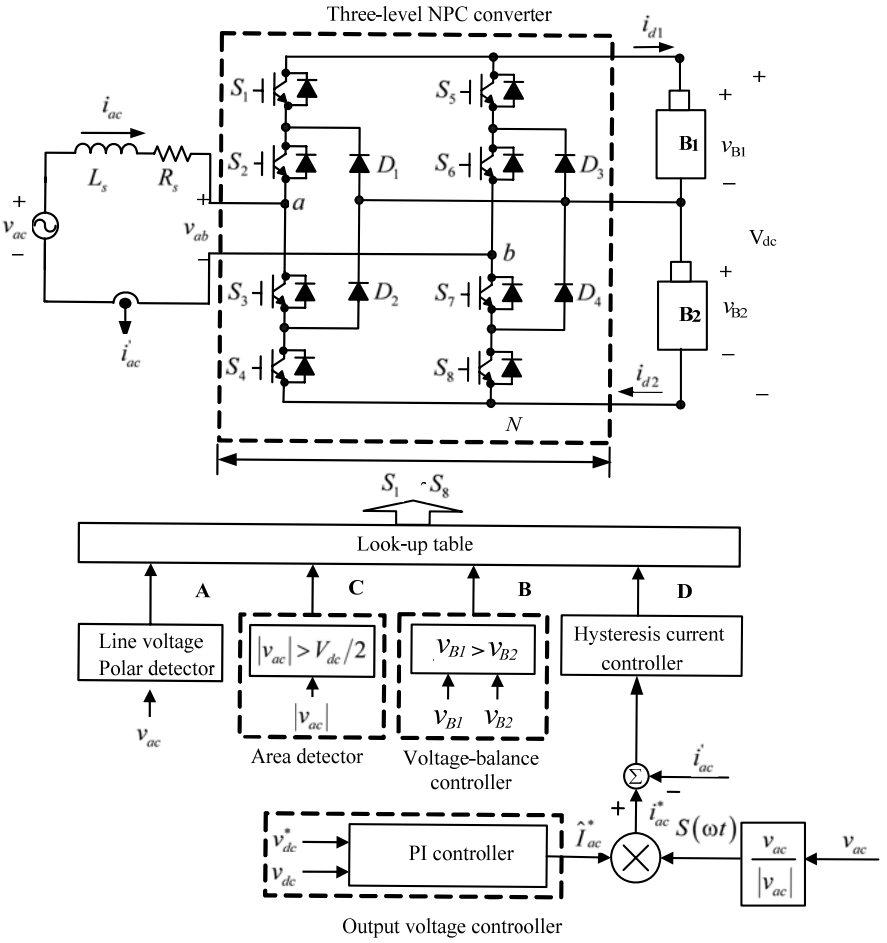


Fig. 1 The scheme of three-level NPC AC/DC converter charge equalizer with power factor correction

If the three-level AC/DC converter is operated at forward power transmission, it can be divided into seven different operation modes for analysis. The circuit configurations for the various modes are as shown in Figs. 2 through 8; the corresponding switch state, input voltage, input current, and charging and discharging state of the battery pack are shown in Table 1. The circuit operations of the various operating modes are described below.

(1) Mode 1

Power semiconductor switches S_1, S_2, S_7, and S_8 are triggered; the circuit configuration is as shown in Fig. 2. At this instant, line current i_{ac} flows towards boost inductor L_s, travels through the anti-parallel diodes of switches S_2 and S_1, batteries B_1 and B_2, and the anti-parallel diode of switch S_8, then finally returns to the electrical supply terminal through the anti-parallel diode of switch S_7. In this mode, the input terminal voltage of the converter is $v_{ab} = V_{dc}$ ($= v_{B1} + v_{B2}$). Since the electrical supply voltage $v_{ac} > 0$ and its amplitude is within Area 2, the line current i_{ac} decreases. At this instant, the circuit equation can be expressed as:

$$v_{ac} = L_s \frac{di_{ac}}{dt} + v_{B1} + v_{B2} \tag{1}$$

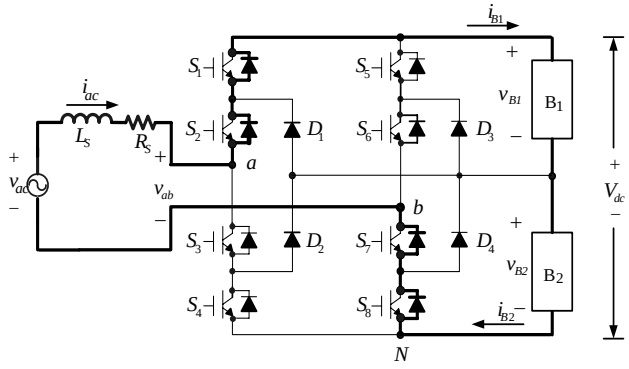


Fig. 2 Circuit for mode 1 of the three-level neutral point clamped charge converter

(2) Mode 2

Power semiconductor switches S_1, S_2, S_6, and S_7 are triggered; the circuit configuration is as shown in Fig. 3. At this instant, line current i_{ac} flows towards boost inductor L_s, passes through the anti-parallel diodes of switches S_2 and S_1, battery B_1, clamped diode D_3, and then finally returns to the power source terminal through switch S_6. In this mode, the input terminal voltage of the converter is $v_{ab} = V_{dc}/2\,(= v_{B1})$. If the power source voltage $v_{ac} > 0$ and its amplitude is within Area 2, then the line current i_{ac} will increase. However, if the power source voltage $v_{ac} > 0$ and the amplitude is within Area 1, then the line current i_{ac} will decrease. In this interval, the circuit equation can be written as:

$$v_{ac} = L_s \frac{di_{ac}}{dt} + v_{B1} \tag{2}$$

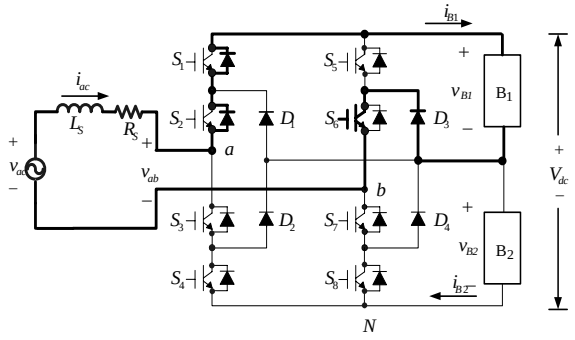


Fig. 3 Circuit for mode 2 of the three-level neutral point clamped charge converter

(3) Mode 3

Power semiconductor switches S_2, S_3, S_7, and S_8 are triggered. At this time, the line current i_{ac} flows towards boost inductor L_s, passing through switch S_3, clamped diode D_2, battery B_2, and the anti-parallel diode of switch S_8, then finally returns to the power source terminal through the anti-parallel diode of switch S_7. The circuit configuration is as shown in Fig. 4. In this mode, the input terminal voltage of converter is $v_{ab} = V_{dc}/2\,(= v_{B2})$. If the power source voltage $v_{ac} > 0$ and its amplitude is within Area 2, then the line current i_{ac} rises. However, if power source voltage $v_{ac} > 0$ and the amplitude is within Area 1, then the line current i_{ac} drops. At this instant, the circuit equation can be expressed as:

$$v_{ac} = L_s \frac{di_{ac}}{dt} + v_{B2} \tag{3}$$

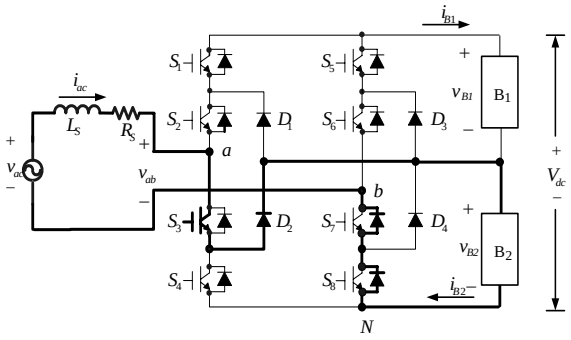


Fig. 4 Circuit for mode 3 of the three-level neutral point clamped charge converter

(4) Mode 4

Power Semiconductor switches S_2, S_3, S_6, and S_7 are triggered. At this instant, the line current i_{ac} flows towards boost inductor L_s, passing through switch S_3, clamped diodes D_2 and D_3, and then finally returning to the power source terminal through switch S_6. The circuit configuration is as shown in Fig. 5. In this mode, the input terminal voltage of the converter is $v_{ab} = 0$. When the power source voltage $v_{ac} > 0$ and its amplitude is within Area 1, the line current i_{ac} will rise. However, when the power source voltage $v_{ac} < 0$ and its amplitude is within Area 1, the line current i_{ac} will drop. At this instant, the circuit equation can be expressed as:

$$v_{ac} = L_s \frac{di_{ac}}{dt} \tag{4}$$

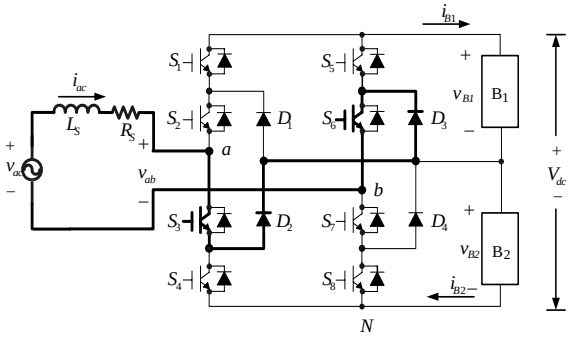


Fig. 5 Circuit for mode 4 of the three-level neutral point clamped charge converter

(5) Mode 5

Power semiconductor switches S_2, S_3, S_5, and S_6 are triggered. At this instant, the line current i_{ac} flows towards boost inductor L_s, passing through switch S_3, clamped diode D_2, battery B_1 and switch S_5, then finally returns to the power source terminal through switch S_6. The circuit configuration is as shown in Fig. 6. In this mode, the input terminal

voltage of the converter is $v_{ab} = -V_{dc}/2$ ($= -v_{B1}$). When the power source voltage $v_{ac} < 0$ and its amplitude is within Area 1, the line current i_{ac} rises; when the power source voltage $v_{ac} < 0$ and its amplitude is within Area 2, line current i_{ac} drops. At this time, the circuit equation can be expressed as:

$$v_{ac} = L_s \frac{di_{ac}}{dt} - v_{B1} \tag{5}$$

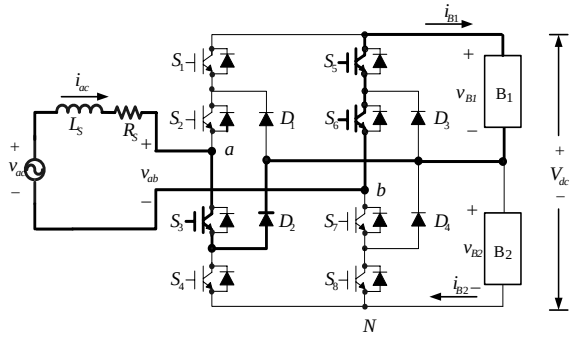


Fig. 6 Circuit for mode 5 of the three-level neutral point clamped charge converter

(6) Mode 6

Power Semiconductor switches S_3, S_4, S_6, and S_7 are triggered. At this instant, line current i_{ac} flows towards boost inductor L_s, passing through switches S_3 and S_4, battery B_2, and clamped diode D_3, and then finally returns to the power source terminal through switch S_6. The circuit configuration is as shown in Fig. 7. In this mode, the input terminal voltage of the converter is $v_{ab} = -V_{dc}/2$ ($= -v_{B2}$). When the power source voltage $v_{ac} < 0$ and its amplitude is within Area 1, the line current i_{ac} rises; when power source voltage $v_{ac} < 0$ and its amplitude is within Area 2, the line current i_{ac} drops. At this instant, the circuit equation can be expressed as:

$$v_{ac} = L_s \frac{di_{ac}}{dt} - v_{B2} \tag{6}$$

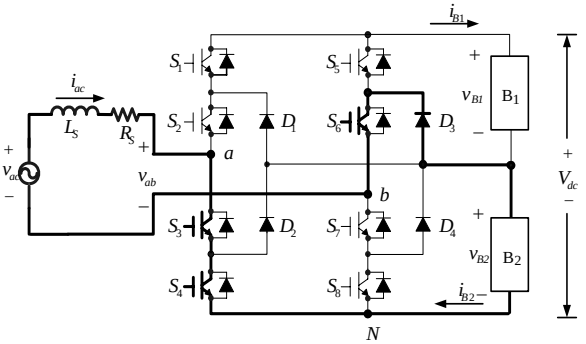


Fig. 7 Circuit for mode 6 of the three-level neutral point clamped charge converter

(7) Mode 7

Figure 8 depicts the circuit configuration for the converter under operating mode 7. Power semiconductor switches S_3, S_4, S_5, and S_6 are trigger. At this instant, line current i_{ac} flows towards boost inductor L_s, passing through switches S_3 and S_4, batteries B_2 and B_1, and switch S_5, and then finally returns to the power source terminal through switch S_6. In this mode, the input terminal voltage of the converter is $v_{ab} = -V_{dc}$ ($= -v_{B1} - v_{B2}$). Since the power source voltage $v_{ac} < 0$ and its amplitude is within Area 2, the line current i_{ac} rises. At this instant, the circuit equation can be expressed as:

$$v_{ac} = L_s \frac{di_{ac}}{dt} - (v_{B2} + v_{B1}) \tag{7}$$

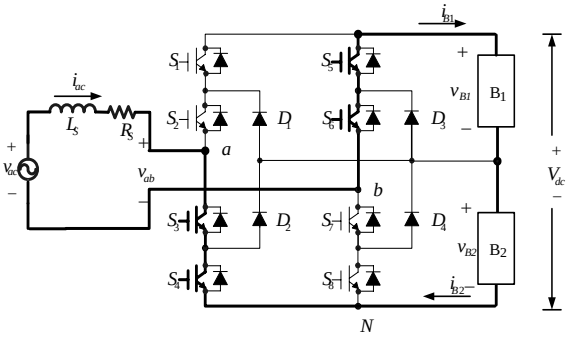


Fig. 8 Circuit for mode 7 of the three-level neutral point clamped charge converter

Based on the above analysis of the seven operation modes of the charge equalization circuits of the three-level converter, the governed equations that can ultimately be derived as:

$$L_s \frac{di_{ac}}{dt} = v_{ac} - R_s i_{ac} - v_{ab} \approx v_{ac} - v_{ab} \tag{8}$$

$$v_{ab} = S_a v_{B1} - S_b v_{B2} \tag{9}$$

The switching functions S_a and S_b are defined as:

$$\begin{cases} S_a \overset{\Delta}{=} (S_1 S_2 - S_5 S_6) \\ S_b \overset{\Delta}{=} (S_3 S_4 - S_7 S_8) \end{cases} \tag{10}$$

And

$$S_{i=1,2,\ldots,8} = 1(0), \text{ if } S_{i=1,2,\ldots,8} \text{ trigger (non-trigger)} \tag{11}$$

$$S_{i=3,4,7,8} = 1 - S_{1,2,5,6} \tag{12}$$

The key variables of every operation mode shown in Table 1 can be found from governed equations (8) to (12).

According to Table 1, if the changes in the

direction of the line current and the area occupied by the line voltage amplitude are already known, then the appropriate operating mode can be selected to cause input terminal voltage v_{ab} to produce appropriate voltage levels to equally charge the rechargeable battery pack. The lower part of Fig. 1 is the control algorithm employed in the three-level neutral point clamped charge equalization scheme. The outer loop voltage controller adopts a proportional plus integral (PI) controller to regulate DC-link voltage, while the inner loop employs a hysteresis current controller (HCC) to force actual current $i_{ac}^{'}$ to follow command current i_{ac}^{*} . The voltages of the two batteries are adjusted using a battery voltage balance controller. The AC-side of the converter uses an area detector to determine the area occupied by the power source voltage to decide the switch trigger signal and produce the appropriate voltage level. The decisions for the four control signals included in this control algorithm are:

$$A = \begin{cases} 0, & \text{if } v_{ac} < 0; \\ 1, & \text{if } v_{ac} > 0 \end{cases} \tag{13}$$

$$B = \begin{cases} 0, & \text{if } |v_{ac}| < V_{dc}/2 \text{(Area 1)}; \\ 1, & \text{if } |v_{ac}| > V_{dc}/2 \text{(Area 2)} \end{cases} \tag{14}$$

$$C = \begin{cases} 0, & \text{if } v_{B1} < v_{B2}; \\ 1, & \text{if } v_{B1} > v_{B2} \end{cases} \tag{15}$$

$$D = \begin{cases} 0, & \text{if } (i_{ac}^{*} - i_{ac})/K_s < -x; \\ 1, & \text{if } (i_{ac}^{*} - i_{ac})/K_s > x \end{cases} \tag{16}$$

The relationships between power switch states and control signals in Table 2 can be obtained from Table 1 and (13)-(16). Based on the states produced by four digital signals A-D, the corresponding switching state of switches can be determined, causing line current i_{ac} to follow the command current i_{ac}^{*}, to be of the same phase as power source voltage v_{ac} , and to control the equal charging of the battery pack at the same time. For example, if line voltage v_{ac} is greater than 0 (A=1) and falls within Area 2 (B=1), the battery voltage v_{B1} is greater than v_{B2} (C=1), and the line current error $(i_{ac}^{*} - i_{ac})/K_s$ is greater than the hysteresis band x (D=1), then power switches S_2, S_3, S_7, and S_8 are selected to be triggered (Mode 3), charging battery B_2, increasing the line current, and producing a voltage level of $v_{ab} = v_{B2}$. According to the control strategies employed in Table 2, the line current i_{ac} can be caused to follow command current i_{ac}^{*} and be of the same phase as power source voltage v_{ac}, realizing a high input power factor and a low current harmonic.

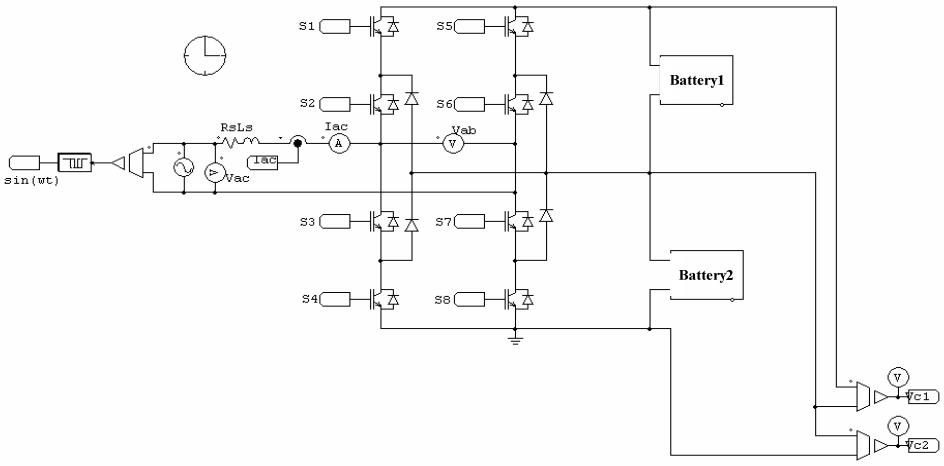
Table 1 Key variable for each operation mode of the three-level NPC converter charging circuit

Variable / Mode	Switch trigger condition	v_{ab}	Line current i_{ac} state		Battery in charging or discharging state	
					B_1	B_2
Mode 1	S_1,S_2 ,S_7,S_8	v_{B1}+v_{B2}	$V_{dc}/2< v_{ac} <V_{dc}$	Decrease	Charge	Charge
Mode 2	S_1,S_2 ,S_6,S_7	v_{B1}	$0< v_{ac} <V_{dc}/2$	Decrease	Charge	Discharge
			$V_{dc}/2< v_{ac} <V_{dc}$	Increase		
Mode 3	S_2,S_3 ,S_7,S_8	v_{B2}	$0< v_{ac} <V_{dc}/2$	Decrease	Discharge	Charge
			$V_{dc}/2< v_{ac} <V_{dc}$	Increase		
Mode 4	S_2,S_3 ,S_6,S_7	0	$0< v_{ac} <V_{dc}/2$	Increase	Discharge	Discharge
			$-V_{dc}/2< v_{ac} <0$	Decrease		
Mode 5	S_2,S_3 ,S_5,S_6	-v_{B1}	$-V_{dc}/2< v_{ac} <0$	Increase	Charge	Discharge
			$-V_{dc}< v_{ac} <-V_{dc}/2$	Decrease		
Mode 6	S_3,S_4 ,S_6,S_7	-v_{B2}	$-V_{dc}/2< v_{ac} <0$	Increase	Discharge	Charge
			$-V_{dc}/2< v_{ac} <-V_{dc}/2$	Decrease		
Mode 7	S_3,S_4 ,S_5,S_6	-v_{B1}-v_{B2}	$-V_{dc}< v_{ac} <-V_{dc}/2$	Increase	Charge	Charge

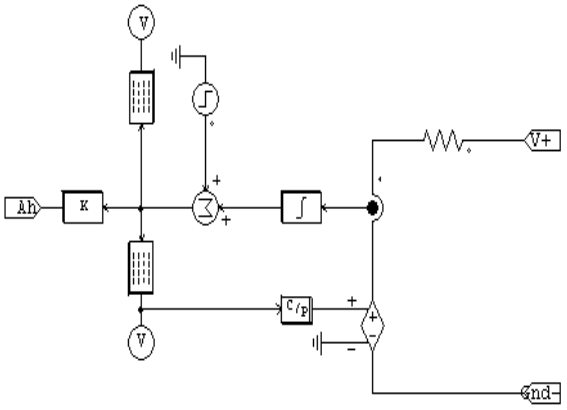
4 Simulation Results

Figure 9(a) shows the simulated circuit of the proposed three-level neutral point clamped AC/DC converter for equalization charge two series connected batteries. The number of required components for the simulated circuit of the three-level neutral point clamped AC/DC converter charge equalizer can be obtained through the following formulas [11]: the formula $(m-1)\times 2$ (m is the number of levels) obtains the number of power semiconductor switches need for each leg of bridge converter, while the formula $(m-1)\times(m-2)$ obtains the number of neutral point clamped diodes needed for each leg of bridge converter. For example, for a three-level converter, there will be 8 IGBT power semiconductor switches and 4 neutral point clamped diodes composing the circuit scheme. Figure 9(b) is the sub-circuit diagram for the lead-acid batteries in the simulated circuit diagram of the three-level neutral point clamped circuit using PSIM software [14].

Figure 10 (a) is the simulated circuit for the controller of the three-level neutral point clamped charge equalizer. The parameter settings for the outer loop voltage controller are $K_P = 0.01$ and $K_I = 0.035$; the power source terminal resistance is $R_S = 5m\Omega$, the power source terminal inductor is $L_S = 0.175mH$, the power source voltage is $v_{ac} = 14V$, and the DC link output voltage is $V_{dc} = 28V$; the battery is a 12V-13Ah battery. The inner loop produces an A-D digital signal through comparison, and then uses the relationship between the switching functions of power switches and control signals, writing the relationship as C-code and using a complier to produce the dynamic link library (DLL) needed for the PSIM circuit simulation software [15]. Figure 10 (b) is the switch control decision established in Table 2 used to decide the operating mode of the switches.

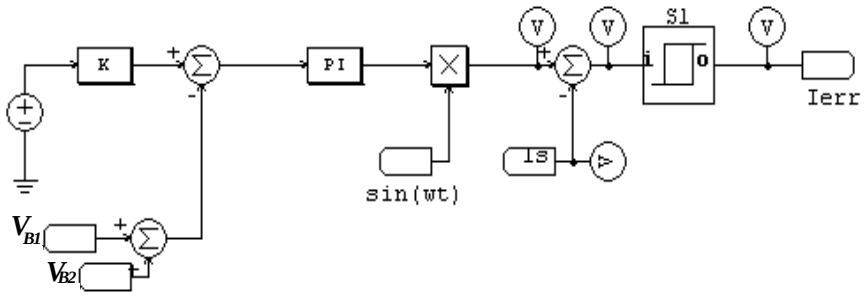


(a)

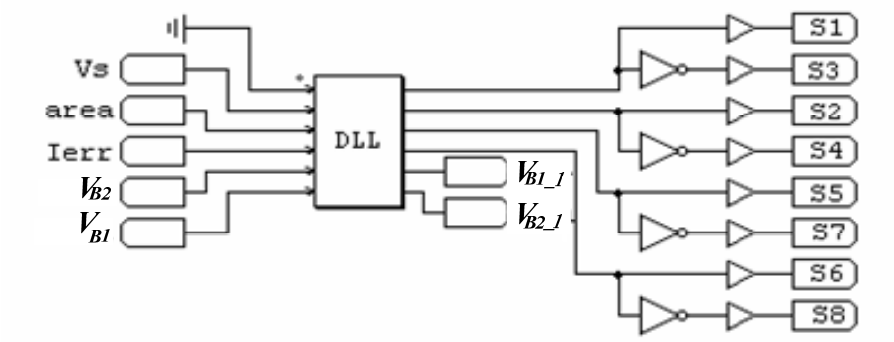


(b)

Fig. 9 Simulated circuit diagrams using PSIM software for the three-level neutral point clamped converter charger equalization circuit: (a)main circuit scheme; (b)sub-circuit of lead-acid batteries



(a)



(b)

Fig. 10 Control circuit diagrams using PSIM software for the three-level neutral point clamped converter charge equalization circuit: (a)voltage controller; (b)switching controller of digital signal

Table 2 Relations between control signals and switching functions of power switches in each mode

A	B	C	D	S_1 ($\bar{S}_3$)	S_2 ($\bar{S}_4$)	S_5 ($\bar{S}_7$)	S_6 ($\bar{S}_8$)	Operation Mode
0	0	0	0	0	1	0	1	4
0	0	0	1	0	1	1	1	5
0	0	1	0	0	1	0	1	4
0	0	1	1	0	0	0	1	6
0	1	0	0	0	1	1	1	5
0	1	0	1	0	0	1	1	7
0	1	1	0	0	0	0	1	6
0	1	1	1	0	0	1	1	7
1	0	0	0	1	1	0	1	2
1	0	0	1	0	1	0	1	4
1	0	1	0	0	1	0	0	3
1	0	1	1	0	1	0	1	4
1	1	0	0	1	1	0	0	1
1	1	0	1	1	1	0	1	2
1	1	1	0	1	1	0	0	1
1	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**3**

Figure 11 shows the simulated wave form of the input terminal voltage v_{ab} for the three-level NPC converter equalization equal charger, it can be seem from simulation results that v_{ab} has three levels at positive and negative half cycles and can thus reduce output voltage harmonics. Figure 12 shows the change curves for the capacities of the two batteries during charging. The initial voltages and capacities of the two batteries were set differently at the start of the simulation. The voltage of Battery 1 was initially set at 11.1V, while the voltage of Battery 2 was initially set as 11.39V. In the charging period (at 3 minutes), the capacity of Battery 2 was increased to exacerbate the inequality in the capacities of lead-acid batteries. The simulation results shown in Fig. 12 indicate that the charge equalization circuit does indeed have good equal charging effects. Figure 13 shows the voltage changes in the two batteries during the charging period, while Fig. 14 shows the voltage differences between the two batteries. Fig. 15 shows the simulated wave forms for input AC voltage v_{ac} and current i_{ac} during the charging period. It can be seen from the simulation results shown in Figs. 13-15 that the three-level converter charger equalization circuit possesses excellent performance in providing battery packs with equal charging and can improve the power quality of the charging power source.

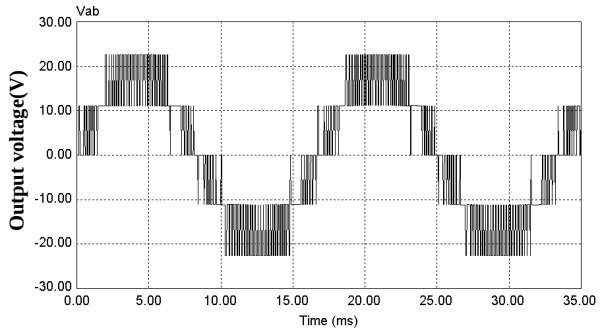


Fig. 11 Simulated wave form for input voltage v_{ab} of the three-level neutral point clamped converter charge equalization circuit

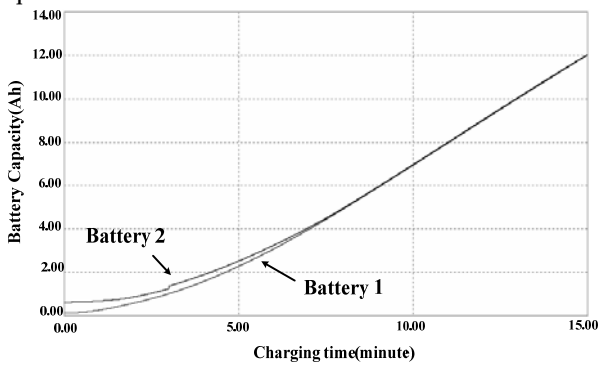


Fig. 12 Capacities and charge time relationship graph for the batteries in the three-level neutral point clamped converter charge equalization circuit

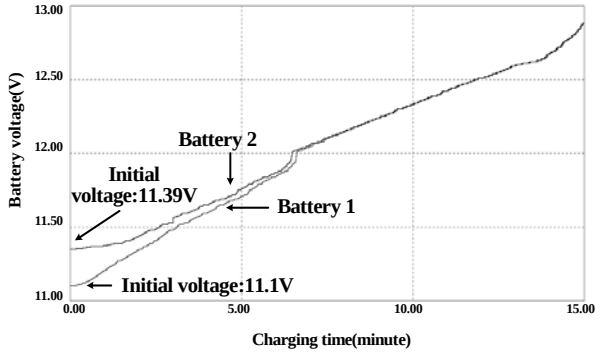


Fig. 13 Relationship graph for the voltage and charging time of the two batteries in the three-level neutral point clamped converter charge equalization circuit

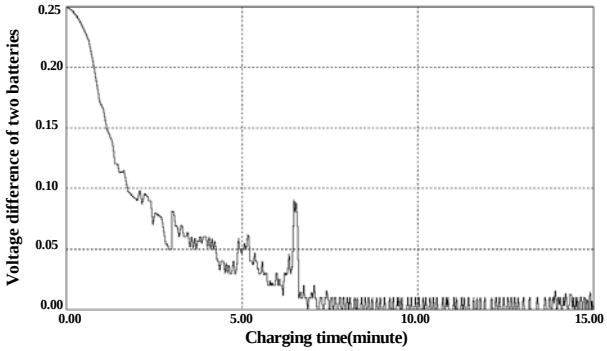


Fig. 14 Relationship graph of the battery voltage difference and charging time of the three-level neutral point clamped converter charge equalization circuit

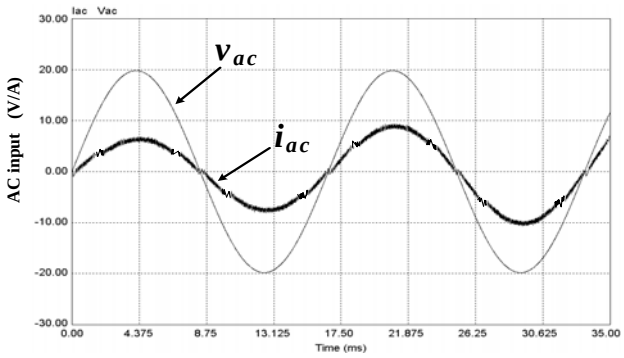


Fig. 15 Simulated wave forms for the AC input terminal voltage v_{ac} and current i_{ac} for the three-level neutral point clamped converter charge equalization circuit

5 Conclusion

This paper presented a battery charge equalization circuit using a three-level neutral point clamped converter as a scheme and used PSIM simulation software to establish a simulated circuit model. Simulation results demonstrated that the battery charge equalization circuit can not only attain the purpose of equally charging rechargeable batteries, but can also cause the power factor for the AC input terminal to approach 1, thereby raising the power quality for the AC-side power supply.

6 Acknowledgement

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References

[1] N. H. Kutkut, D. M. Divan, and D. W. Novotny, "Charge Equalization for Series Connected Battery Strings," *IEEE Transactions on Industry Applications*, Vol. 31, 1995, pp. 562-568.

[2] S. West and P. T. Krein, "Equalization of Valve-Regulated Lead-Acid Batteries: Life Test Results," *in Proceedings of IEEE Telecommunications Energy Conference*, 2000, pp. 439-446.

[3] P. T. Krein and R. S. Balog, "Life Extension through Charge Equalization of Lead-Acid Batteries," *in Proceedings of International Telecommunications Energy Conference*, 2002, pp. 516-523.

[4] B. Lindemark, "Individual Cell Voltage Equalizers (ICE) for Reliable Battery Performance," *in Proceedings of International*

Telecommunications Energy Conference, 1991, pp. 196-201.

[5] Y. C. Hsieh, et al., "Balance Charging Circuit for Charge Equalization," *in Proceedings of IEEE Power Conversion Conference*, 2002, pp. 1138-1143.

[6] P. T. Krein and C. Pascual, "Switched Capacitor System for Automatic Series Battery Equalization," *in Proceedings of IEEE Applied Power Electronics Conference*, 1997, pp. 23-27.

[7] N. H. Kutkut, D. M. Divan and D. W. Novotny, "Charge Equalization for an Electronic Vehicle Battery System," *IEEE Transactions on Aerospace and Electronic Systems*, Vol. 34, 1998, pp. 235-246.

[8] N. H. Kutkut, H. L. N. Wiegman, D. M. Divan and D. W. Novotny, "Design Considerations for Charge Equalization of an Electric Vehicle Battery System," *IEEE Transactions on Industry Applications*, Vol. 35, 1999, pp. 28-35.

[9] N. H. Kutkut, D. M. Divan and D. W. Novotny, "Charge Equalization for Series Connected Battery Strings," *in Conference Record IEEE on Industry Applications Society Annual Meeting*, 1994, pp. 1008-1015.

[10] N. H. Kutkut, "Nondissipative Current Diverter Using a Centralized Multiwinding Transformer," *in Proceedings of IEEE Power Electronics Specialists Conference*, 1997, pp. 648-654.

[11] J. S. Lai and F. Z. Peng, "Multilevel Converters - A New Breed of Power Converters," *IEEE Transactions on Industry Applications*, Vol. 32, 1996, pp. 509-517.

[12] B. S. Suh, G. Sinha, M. D. Manjrekar and T. A. Lipo, "Multilevel Power Conversion - An Overview of Topologies and Modulation Strategies," *in Proceedings of the 6th International Conference on Optimization of Electrical and Electronic Equipments*, Vol. 2, 1998, pp. AD-11 -AD-24.

[13] B. R. Lin and D. J. Chen, "Power Factor Correction Based on Diode Clamped Rectifier," *International Journal of Electronics*, Vol. 88, 2001, pp. 595-614.

[14] Z. M. Salameh, M. A. Casacca and W. A. Lynch, "A Mathematical Model for Lead-Acid Batteries," *IEEE Transactions on Energy Conversion*, Vol. 7, 1992, pp. 93-97.

[15] PSIM User's Guide, *Powersim Inc.*, 2001-2003.