Analog Blocks Design Automation

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Abstract: - The purpose of this paper is to present an automated design methodology for analog blocks. This method focuses on analog blocks design parameters automatic generation according to specific design constraints. This method is based on analog circuits' mathematical models. These models are generated thanks to a "Design Of Experiment" (DOE) technique. The DOE technique takes as input electrical simulation results of a given circuit for different component geometries. DOE generates polynomial equations of the circuits' outputs. Using these equations and according to given design specifications, the methodology provides the most suitable design parameter values. This efficient methodology reduces extensive simulations to find the right design parameters with respect to circuit accuracy.

Key-Words: - Analog circuits, design automation, modelling, Charge Pumps (CP), Current References (CR).

1 Introduction

The design of analog circuits becomes a complex process. Some analog circuits such as Charge Pumps (CP), Current References (CR) or RF amplifiers are widely used in the IC market. These circuits may have few transistors; however the design of such circuits over voltage and temperature variations may require tremendous simulation times due to precise modeling of all the circuits' elements. Besides, designers have to deal with technology scaling and low-power circuits' specifications to touch the growing embedded device market. In this context, a new design solution is proposed to deliver optimum performances for analog functions.

From a designer point of view, once a design topology is selected, design consists usually in tuning design component parameters in order to reach the desired electrical specifications. This design strategy forces designers to handle dozens of variables and parameters to implement analog functions.

Previous studies propose several methods for automated synthesis of analog circuits [1]–[5]. In [1], a method based on transistors' size optimization is presented. In this method, important parameters others than transistor geometries are ignored which limits the optimization process. In [2], the author presents a generic method for analog design optimization using the Tabu Search heuristic. The goal is to minimize a given cost function which depends on a set of designer specifications. The main limitation of this method is the large number of simulations or measurements to perform in order to minimize the cost function. Indeed, the author needs few hundred inputs (measurements or simulation results) to optimize each of the ten design parameters. Other methods focus on the development of analytical models dedicated to analog circuit's optimization. These models allow a good understanding of circuits and can be used to determine the optimal parameter values. However, the use of analytical models to optimize a circuit is not a generic method and models generation consumes huge time.

The aim of the presented design methodology is to optimize an analog circuit design under specific constraints. Analog circuits' components (including passive and active elements) as well as extrinsic parameters (like the supply voltage) can be considered by the methodology.

To validate this approach, two application examples are proposed. In the first application, CP circuit design parameters are automatically generated according to specific design constraints like

maximum output voltage HV or minimal consumption current I_{SUNK}. The second application proposes a CR circuit design parameters automatic generation according to specific design constraints. In this case, constraints like a stable output current I_{REF} (i.e small temperature β_T and supply voltage β_V dependency factors) and also a minimal consumption current are considered.
Circuit design parameters are automatically generated thanks to "Design Of Experiment" (DOE) technique. DOE generates circuit's models to link design parameters to specific circuit outputs.
This paper is organized as follows. Section II gives an overview of the automated design methodology. In section III, the DOE technique is detailed in order to explain the generation of analog circuits' models. In practical terms, the effects (main effects and interactions) of design parameters on the circuit output are explored using a DOE technique. Section IV is dedicated to two application examples (CP and CR circuits). Finally, Section V gives some concluding remarks.

2 Analog blocks design methodology

2.1 Design methodology

The design flow presented Fig.1 generates design circuit parameters values according to a given output target (i.e. specifications of the circuit). Then, a DOE technique is used to generate a map of simulations. From the simulation results, DOE builds a polynomial model of the considered circuit outputs. During the last step of the flow, the polynomial model of the considered output generates a list of all the possible sets of circuit parameters values that meet the specifications.

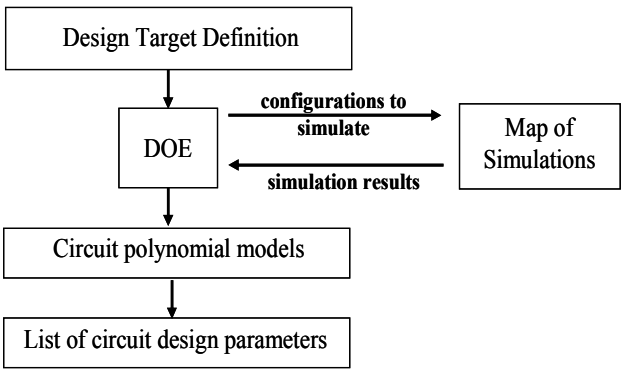

Fig.1 Design methodology presentation

With this approach, the use of polynomial models reduces the amount of analysis required to find suitable circuit parameters.
This methodology is applied to two specific circuit topologies: a charge pump circuit and a current reference circuit.

2.2 Charge pump circuit (CP)

When dealing with CP circuits, constraints as design robustness, maximum output voltage, minimal consumption current, and maximal power efficiency have to be taken into account during the design process. Most high voltage generators are based on the Dickson CP [6]. However, as supply voltage being scaled down, the pumping efficiency of the Dickson CP is severely degraded.
An optimized strategy for designing these circuits is proposed in [7], with an analytical model. In this model, efficient design parameters can be computed for a chosen technology.
CP circuit performances are affected by threshold voltage, reverse current and body effect. That is why others architectures like the NCP-2 [8] or the CTS [9] have been developed to overcome these limitations.
The complete design scheme of a CP circuit needs an optimization step, with global simulations which take into account all effects. CP simulation is time consuming because a small time step is needed due to the high input clock frequency. The optimization of CP designs with several parameters to determine could take a long time, even if an approximation value is defined for the main parameters.

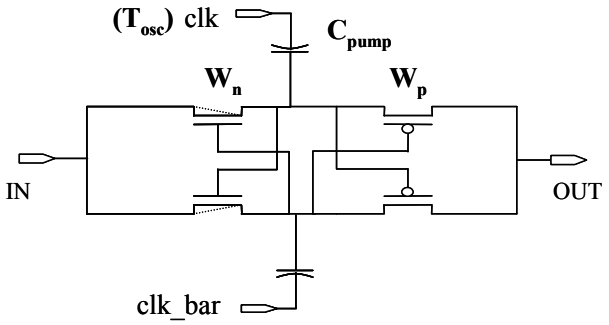

Fig.2 Charge Pump CTS elementary stage

In this work, a CP design methodology is presented for the CTS structure shown in Fig.2 which currently presents the best choice for low voltage and low current circuits. In a first approximation, we assume that the CP outputs (HV and I_{SUNK}, presented in Fig.3) depend mainly on the two NMOS transistors widths W_n, the two PMOS

transistors widths W_p, the value of the pump capacitors C_{pump} and also the input clock period T_{osc}. These four parameters W_n, W_p, C_{pump} and T_{osc} are chosen as CP input parameters.
The simulation context is defined by the different elements surrounding our 10 stages CTS CP. In order to be as close as possible to the product working conditions, simulations are performed by including in the design of the CP, a clock driver and an output charge as shown in Fig.3.

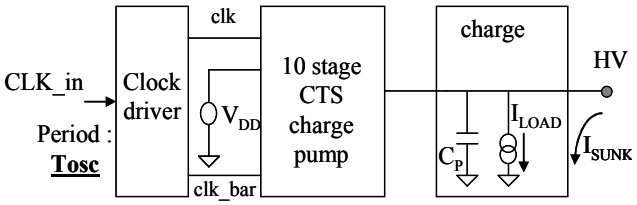

Fig.3 High voltage generator circuit

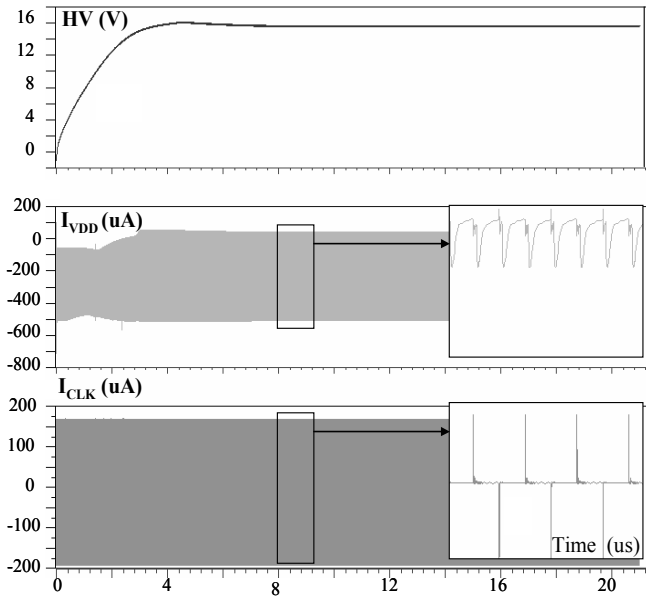

Fig.4 Charge pump outputs simulation results

CP output curves, obtained for nominal values of input parameters are shown Fig.4, after transient simulations. The first response is the HV voltage. The second response is the consumption current which is obtained by adding the average current I_{Clk} sunk to the clock and the average current I_{VDD} sunk on V_{DD}. The total consumption current for a given load and a given supply voltage V_{DD} is called I_{SUNK}. Knowing CP critical outputs, effects of CP input parameters on the circuit outputs can be evaluated.

2.3 Current reference circuit (CR)

In CR circuits, specific constraints like small temperature voltage and supply voltage dependency factors have to be taken into account during the design process.
As CP circuits, CR circuit design needs an optimization step, with a limited number of simulations. In this study, a CR design methodology is presented for the CMOS structure given Fig.5. In the proposed CR circuit a current mirror imposes equal currents in the two branches of the circuit. Transistor N_4 works as an active resistance (below saturation) and is biased by 2 additional MOSFETs N_3 and P_3 in order to provide a suitable gate voltage for N_4 [10]. In this kind of structure, the W/L ratio of each transistor has to be monitored as well as possible because it impacts directly the CR outputs.

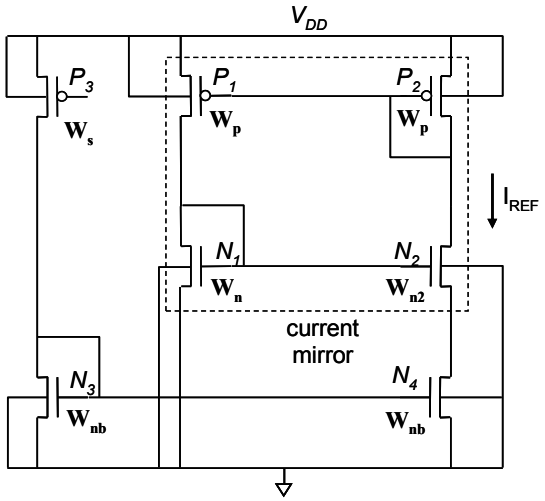

Fig.5 Current reference circuit

In a first approximation, we assume that the CR output I_{REF} depends mainly on the transistors widths W_s, W_p, W_n, W_{n2} and W_{nb}. These five parameters, shown Fig.5, are chosen as the CR input parameters. CR reference outputs curves, obtained for nominal values of input parameters are shown Fig.6, after DC simulations. If we consider that the current I_{REF} increases linearly with the temperature and the supply voltage V_{DD}, two factors can be extracted from the CR simulation results: the temperature dependency factor β_T and the supply voltage dependency factor β_V. Another important parameter is the total consumption current called I_{SUNK}, obtained for a given load and a given supply voltage V_{DD}. I_{REF}, β_T, β_V and I_{SUNK} are considered as the CR outputs.

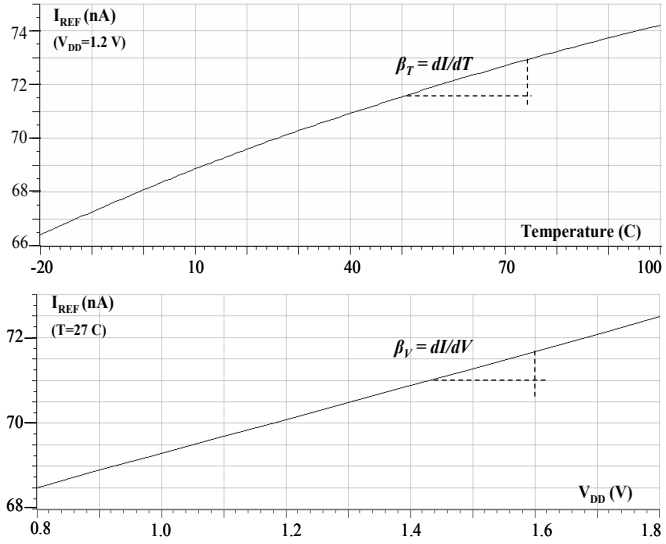

Fig.6 Current reference outputs

3 Analog bocks models

3.1 Design of experiment methodology

To link all circuit parameters P_i to a specific output O_i, any possible variations of all P_i parameters has to be considered. It clearly appears that a classical approach based on changing one parameter at a time for all other possible parameter values is intractable in number of experiments to perform. For example, considering 100 possible values for "m" parameters leads to perform 100^m simulations to build a database. Although this approach is very accurate, it requires several thousands of simulations.

To pass over this limitation, a technique based on "Design Of Experiment" (DOE) is used. DOE methods use probabilities and statistics to define the minimum number of experiments needed to identify significant cause-and-effect relationships between a given number of factors and one or more responses. Mathematically, DOE methods are developed to identify efficient experimental designs. Choosing an experimental design depends on the objectives of the experiment and the number of factors.

Doehlert [11] suggests using a polynomial model to approximate the response. This polynomial model is computed using a Response Surface Methodology (RSM). RSM is concerned with the modelling of one or more responses to the settings of several explanatory variables. The nature of the function relating the responses to the variables is assumed to be unknown and the function or surface is modelled empirically using a first or a second-order polynomial model. The fundamentals of RSM are set out in the seminal papers of Box and Wilson [12] and Box and Draper [13] and in the books by Box and Draper [14] and Khuri and Cornell [15]. RSM is a combination of experimental and regression analysis and statistical inferences [16].

The broad aims of RSM are to investigate the nature of the response surface over a region of interest and to identify input factors combinations associated with maximum or minimum responses. In fact, this technique can be simplified huge number of experiments where it saves time and the cost of the experiments. In Doehlert designs, experimental points are uniformly placed in the experimental domain. This design should be sufficient to fit a quadratic model thanks to RSM, that is, one containing squared terms and products of two factors.

3.2 Circuit polynomial model

In our case, experiments are in fact a set of simulations, thus this technique is here called "Design Of Simulation" (DOS). DOS allows having a complete knowledge of the selected circuit outputs (responses) in the domain of variation of the considered input parameters (factors). This domain of variation is called sphere of knowledge. We assume that a given circuit design topology is selected and that the most significant design parameters are known. RSM approximates a given circuit output value 'O_i' in the form of polynomial function of independent variables P_i, P_j coming from a limited number of simulations. In practical terms, a Doehlert design is selected to define all the circuit's configurations to simulate. With this information, a map of simulations is built around N configurations defined with different values of the input parameters, as shown Table I.

The minimal number of simulations to perform is given by the Doehlert design according to the number of input parameters.

TABLE I MAP OF SIMULATION EXAMPLE

n°	Input parameters				outputs		
	P_1	**P_2**	**….**	**P_I**	**O_1**	**…**	**O_J**
1	P_{11}	P_{12}	….	P_{1I}	O_{11}	…	O_{1J}
2	P_{21}	P_{22}	….	P_{2I}	O_{21}	…	O_{2J}
3	P_{31}	P_{32}	….	P_{3I}	O_{31}	…	O_{3J}
:			:			:	
:			:			:	
N-1	P_{N-11}	P_{N-12}		P_{N-1I}	O_{N-11}	…	O_{N-1J}
N	P_{N1}	P_{N2}		P_{NI}	O_{N1}	…	O_{NJ}

Therefore, N electrical simulations of the circuit are automatically performed. From the result of these simulations (i.e. O_i extraction), RSM uses a multi-

regression algorithm to extract the polynomial model of each output. The general form of the polynomial model is given by equation (1).

$$O_i = b_0 + \sum_i b_i.P_i + \sum_i b_{ii}.(P_i.P_i) + \sum_{ij} b_{ij}.(P_i.P_j) \quad (1)$$

The confidence on each O_i equation is given by the study of residuals, i.e. the difference between values obtained by the equation and the ones obtained by simulation.

In this study, if the CP circuit is considered, the outputs O_i are I_{SUNK} and HV. If the CR circuit is considered, the outputs O_i are I_{SUNK}, I_{REF}, β_T and β_V. In the same manner, the parameters P_i are W_n, W_p, C_{pump} and T_{osc} for the CP circuit and W_s, W_p, W_n, W_{n2} and W_{nb} for the CR circuit.

Knowing that, the main objective is to generate polynomial models using classical DOE and RSM techniques, then use these models to help with circuit parameter selection (e.g., sizing). This technique is applied to two specific circuit topologies to speed up the circuit design and to provide optimisation tool in the same time.

Fig.7 illustrates the different steps of the polynomial model generation technique in the case of the CP circuit. Advantages offered by the polynomial model are listed below:

- A simple polynomial expression which allows fast computing time,
- A limited number of simulations are necessary, allowing a short generation time. This property can be used to automatically fast calibrate the model to switch from one technology to another,
- The validation of the model is achieved by monitoring the output accuracy (residuals study).

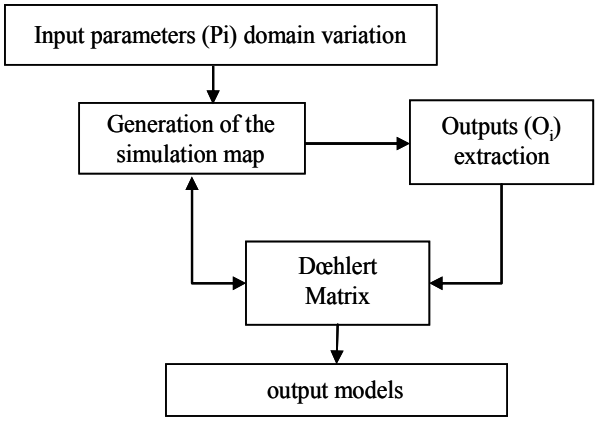

Fig.7 Model generation block diagram

4 Application examples

4.1 Application example 1: Charge pump

4.1.1 CP polynomial model

The CP polynomial model is built using a DOE technique. Table II lists the 21 input parameters values configurations to simulate. From the result of these simulations, the polynomial model of each considered output (HV or I_{SUNK}) is extracted.

The domain of variation of each CP input parameter related to their nominal value is given in Table III.

TABLE II CP MAP OF SIMULATIONS

n°	CP Input parameters				CP outputs	
	C_{pump}	W_n	W_p	$T_{osc}/2$	HV	I_{SUNK}
1	510	4.3	1	2.75	15.0	195.8
2	500	4.1	1	2.75	15.0	200.1
3	190	1.7	1	2.75	16.5	99.8
:	:				:	
:	:				:	
21	350	3	1	2.79	16.7	141.7

TABLE III CP INPUT PARAMETER DOMAIN VARIATION

	C_{pump}	W_n	W_p	T_{osc}
Nominal	270 fF	3.2 µM	1 µM	2.75 ns
Δ	± 160 fF	± 1.5 µM	± 0.8 µM	± 0.28 ns

The confidence on the 2 CP polynomial equations is given by the study of residuals. The maximal difference for HV is 0.27V and 0.45µA for I_{SUNK}. It is important to notice that these values are obtained from corner cases at the limit of the sphere of knowledge. They represent respectively less than 1.5% and 0.3% of error compared to the simulated values. Residuals and the rectilinear normal plot, presented in Figure 8 confirm these results for the HV output.

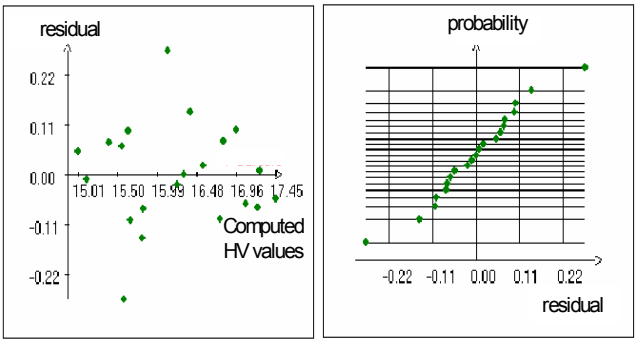

Fig.8 HV residuals and normal plot

Fig.9 gives an illustration of the HV polynomial model processing. In this example, the evolution of the HV output versus C_{pump} and T_{osc} parameters is shown (the other parameters being set at their nominal values). With such a representation, the impact of each CP parameter can be easily evaluated by considering one output at a time as a function of two input parameters. The first information given by this representation is the existence of an optimal HV value which is obtained for large time periods T_{osc} and important C_{pump} values. From a robustness point of view, sensitivity to T_{osc} and C_{pump} variation is acceptable inside the maximal HV area.

In Fig.10, an illustration of the I_{sunk} polynomial model processing is given. Impact of C_{pump} and T_{osc} parameters on the CP consumption current can be graphically evaluated.

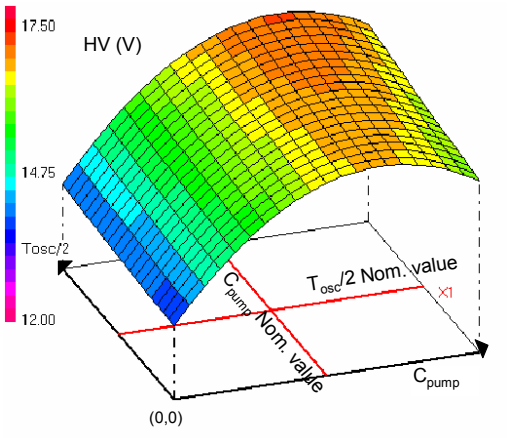

Fig.9 HV response versus T_{osc} & C_{pump}

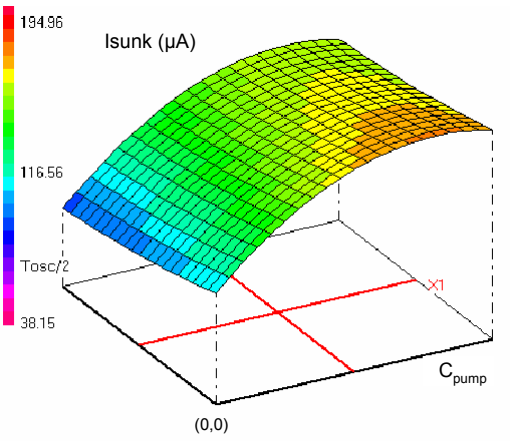

Fig.10 I_{SUNK} response vs T_{osc} & C_{pump}

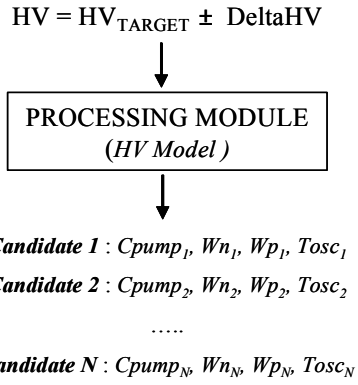

Fig.11 HV Candidates generation

In Fig.11, the HV CP polynomial model is used to generate a list of all possible CP parameter configurations that meet the targeted HV value. These configurations are called candidates. The HV window variation DeltaHV is set in function of the wanted accuracy in order to limit the number of candidates.

4.1.2 CP Design methodology

To validate the design methodology approach, a numerical application based on the high voltage generator circuit presented in Fig.3 is proposed. In this study, a CP output HV equals to 17 V ±15mV is targeted.

The first step of the design methodology consists in building a global database made of the combination of the four input parameters. This is done by varying each parameter step by step for all other possible parameter values, in the domain of validity of the HV polynomial model (the step of variation of the input parameters is given by design rules). Thus, a global database of 8 860 candidate configurations with their corresponding output values is generated (Fig.11). Then, from this initial database, 22 configurations that meet the targeted HV value are extracted by the processing module.

Fig.12 shows the 22 candidates parameters values generated by the processing module. For each of the 22 candidates, (represented on the abscissa) the corresponding CP parameters are given. For example, candidate 10 is associated with a value of 430fF for C_{pump}, 1.8µm for W_n, 1.6µm for W_p and 186MHz for F_{osc}. With this information, the designer is able to choose the most suitable set of design parameters (among the 22 proposed).

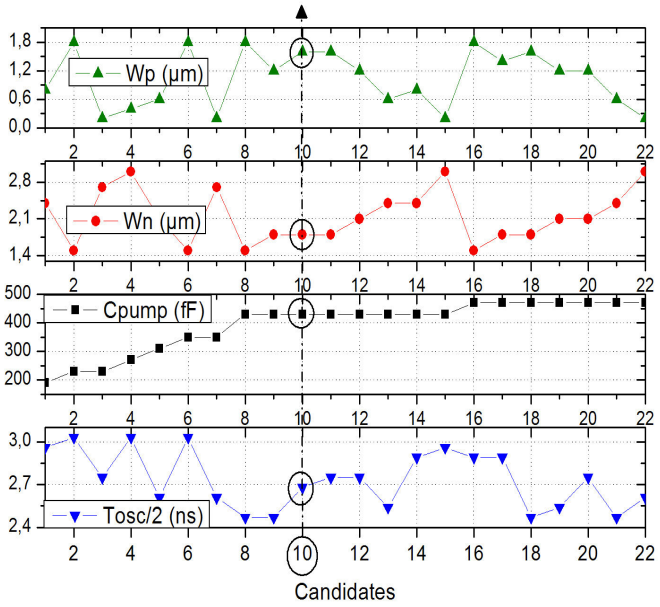

Fig.12 Candidate's parameters for HV = 17V±15mv

It is also possible to consider other CP outputs like the CP power efficiency η. η is defined as the ratio between the output power P_{OUT} delivered to the load and the input power P_{IN} obtained from the supply (i.e. by knowing HV and I_{SUNK}). In Fig.13, I_{SUNK} and η outputs are given for each candidate.

In this representation, candidate 10 exhibits 188.6µA for the consumption current and a power efficiency equals to 6.8%.

Concerning the HV robustness criteria (related to its nominal value), the impact of a +10% variation of one input parameters (the other parameters being set at their nominal values) is evaluated on the HV output. The robustness rating is given in Fig.14 for each 22 candidate parameters. If candidate number 4 is considered, it appears clearly that this candidate is robust regarding C_{pump}, F_{osc} and W_p but very sensitive regarding W_n.

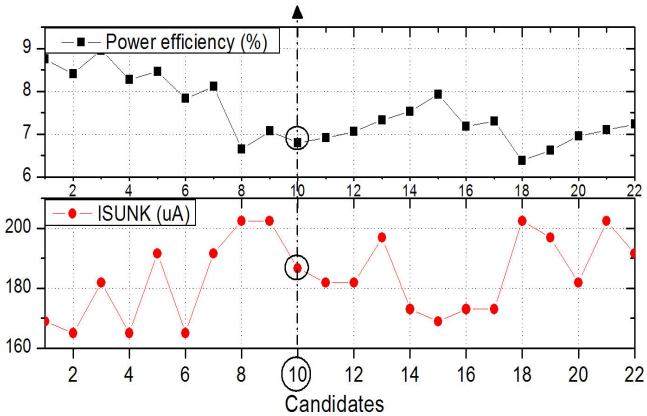

Fig.13 I_{SUNK} & η outputs

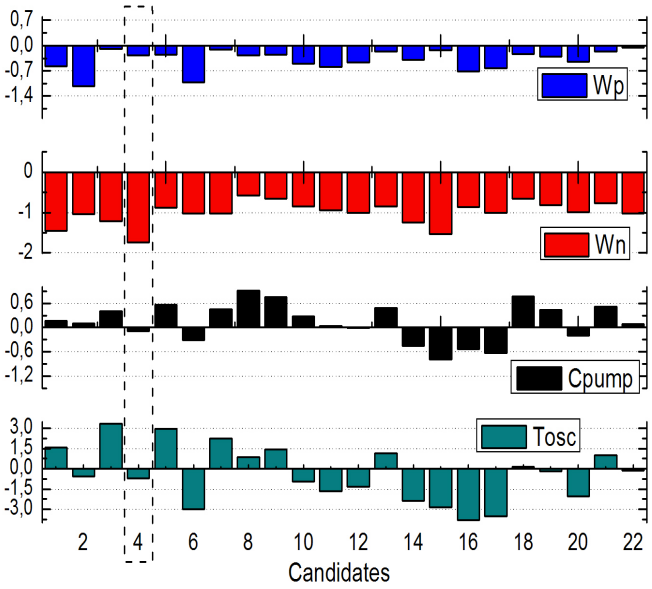

Fig.14 Candidate's robustness

4.2 Application example 2: Current reference

4.2.1 CR polynomial model

To build the CR model, 31 input parameters values configurations are generated and simulated. Table IV lists the 31 configurations to simulate. The domain of variation of each CR input parameter related to their nominal value is given in Table V.

The CR outputs residual study gives excellent results: the maximal differences are 1.2nA for I_{REF}, 5.4nA for I_{SUNK}, 0.096pA/C for β_T and 0.09nA/V for β_V. These values represent respectively less than 0.014%, 0.019%, 0.015% and 0.022% of error compared to the simulated values.

TABLE IV CR MAP OF SIMULATIONS

n°	CR Input parameters					CR outputs			
	W_s	W_p	W_n	W_{nb}	W_{n2}	I_{REF}	β_T	β_V	I_{SUNK}
1	18	7.5	37	167	0.55	95.8	10.4	5.25	419.5
2	12	7.5	37	167	0.55	46.6	5.28	3.00	167.3
:	:	:	:	:	:	:	:	:	:
30	15	7.5	35	145	0.64	66.8	7.46	4.25	265.9
31	15	7.5	35	169	0.55	71.6	7.98	4.04	285.0

TABLE V CR INPUT PARAMETER DOMAIN VARIATION

	W_s	W_p	W_n	W_{n2}	W_{nb}
Nominal	15µm	7.5µm	37.5µm	167µm	550nm
Δ	± 20%	± 20%	± 20%	± 20%	± 20%

Fig.15.a,b,c,d give an illustration of the CR polynomial model outputs I_{REF} (a), I_{SUNK} (b), β_V (c) and β_T (d) versus different input parameters.

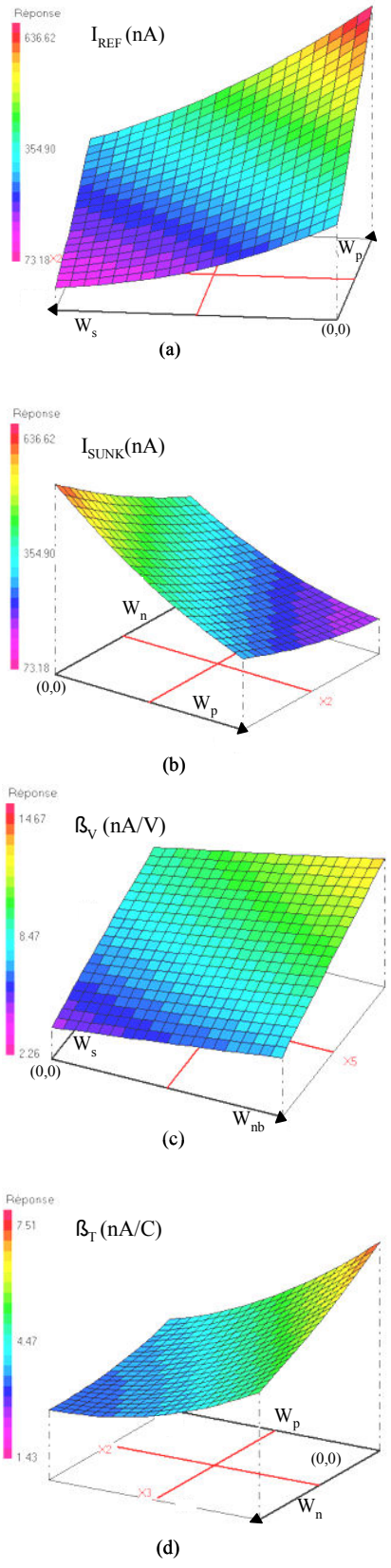

Fig.15 CR responses vs CR transistor widths Wp & Wn

Fig. 16 shows the I_{REF} polynomial model processing step, used to generate candidates according to a given I_{REF} target value.

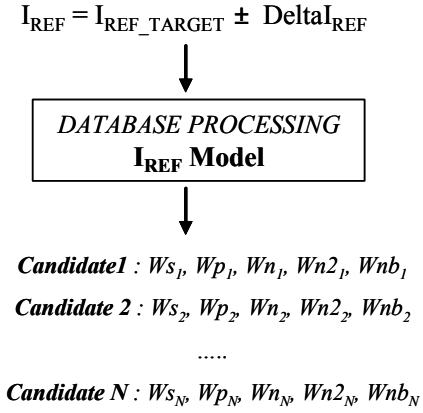

Fig.16 I_{REF} Candidates generation

4.2.2 CR Design methodology

To validate the CR design methodology approach, a numerical application based on the CR circuit presented in Figure 5 is proposed. In this study, we target a CR output current I_{REF} equals to 70nA. Then, thanks to our design methodology, one can try to minimize the CR consumption current I_{SUNK} and the CR dependency factors of the considered output current I_{REF}.

For this application example, a global database of 55296 candidates' configuration with their corresponding output values is generated (Fig.16). Then, from this initial database, 20 configurations that meet the targeted I_{REF} value are extracted by the processing module. Fig.17 shows the 20 candidates parameters values generated by the processing module. In this application example, candidate 6 is associated with a value of 0,44µm for W_{nb}, 13.5µm for W_s, 6.2µm for W_p, 39.6µm for W_n, 187.6µm and for W_{n2}.

In Fig.18, other CR outputs I_{SUNK}, β_V and β_T are given for each candidate. These outputs are computed using the I_{SUNK}, β_T and β_V models. In this representation, candidate 6 exhibits 321nA for I_{SUNK}, 8.1pA/C for β_T and value of 3.5nA/V for β_V. Concerning the I_{REF} robustness criteria, the impact of a +10% variation of one input parameter is evaluated on I_{REF} output. The robustness rating is given in Fig.19 for the 20 candidates. We can notice that I_{REF} variation trend is positive for W_n and W_p but negative if we consider W_{n2}, W_s and W_{nb} parameters.

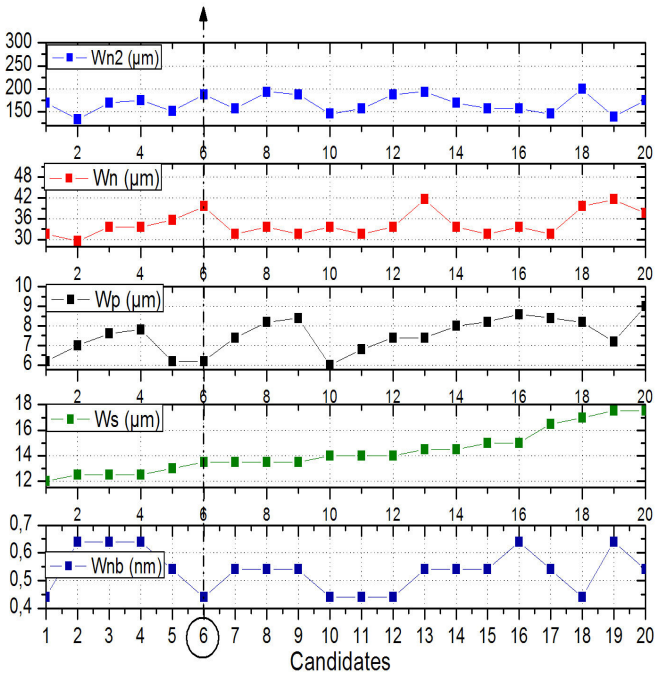

Fig.17 Candidates' parameters for IREF = 70nA±0.5nA

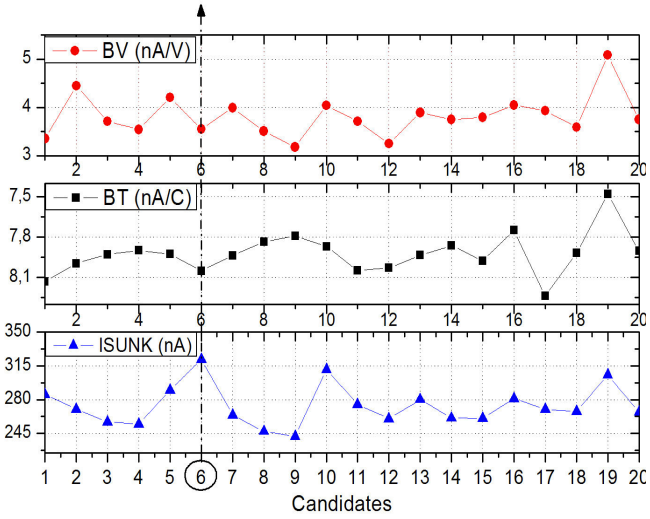

Fig.18 Candidates' outputs

From a design point of view, all these information are very useful to quickly find suitable design parameters configurations to fulfil design specifications. Besides, the design robustness criterion is also considered by the methodology to propose a reliable design solution.

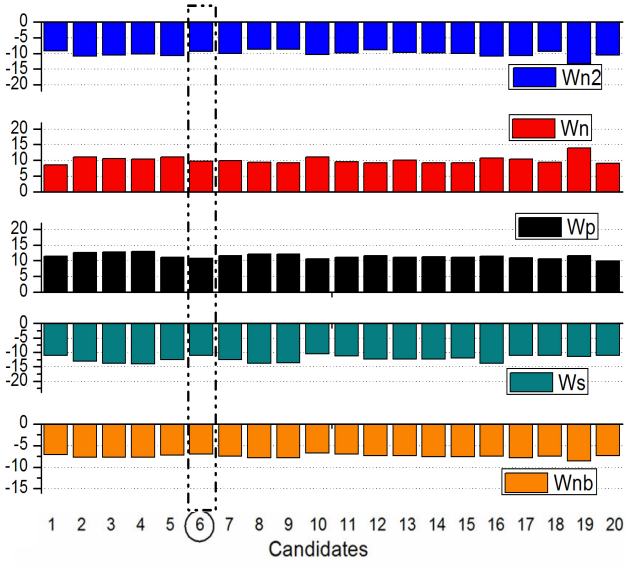

Fig.19 Candidates' robustness

5 Conclusion

In this paper, an efficient design methodology for analog circuits is presented. Knowing that analog circuit performances are strongly dependant on design parameters, the proposed design strategy is very useful to speed up analog blocks design. This method takes advantage of design of experiments. The first step of the methodology consists in identifying design parameters which have a significant effect on the circuit responses. Then, by running a sequence of suitable simulations, a second-order polynomial model is used to fit the circuit responses evolution within the sphere of knowledge. Accuracy of the model is checked by the study of residuals. In this design methodology a limited number of parameters are considered. It is also possible to evaluate analog blocks outputs for an exhaustive list of input parameters to obtain a global analog circuit model. It will result in an increase of the number of simulations to perform in order to build the polynomial model.

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