

# Design and Analysis of SOP-HMIC Transceiver with Integrated T/R Switch

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*Abstract:* - The demand for higher performance systems that are smaller and have the potential to be more cost effective has lead the hardware designers to adopt integration of many components and modules in a package (SOP) or on a chip (SOC). Two compact SOP (single-substrate) SO-HMIC transceivers with integrated T/R switch modules for high-resolution sensor application have been demonstrated. These modules contain singly-balanced diode mixer; using either rate-race or Lange coupler; lowpass filter, 7-dB power splitter using branch coupler and T/R switch. A new and efficient methodology is investigated for the design of microstrip T/R switch. The components of the modules are designed using the full-scale computer simulation program performed with the authors, while they are analyzed and optimized using the Aplan V7.61 software. The analysis of the designed transceiver modules is introduced which reflects a good performance and achieves a higher efficiency.

*Key-Words:* Computational Microstrip Circuit Design, Microwave Circuits and systems, Computer Aided Design (CAD)

## 1 Introduction

Recently many works have been performed for the design and fabrications of the individual parts of the microwave transceiver circuit such as amplifiers, oscillators and mixers using microstrip technique [1-6]. In the beginning of 1990, the works of fabrication of a complete microstrip transceiver has been started especially for the military applications. This paper is considered as an extension of the previous work that produce a perfect and reliable SOP transceiver with integrated T/R switch (TRS) to be used in military and civilian applications.

## 2 SOP-HMIC Transceiver with Integrated T/R Switch

Figure 1 shows the block diagram of the L-band sensor including the designed SOP-HMIC transceiver with integrated TRS module. The sensor comprises a 4-GHz microstrip negative-resistance oscillator (NRO), 4-GHz broadband microstrip

amplifier (BMA) and the transceiver module with integrated TRS which consists of a 7-dB power splitter using microstrip branch coupler (MBC), singly balanced diode mixer (SBDM) with 4-port rate-race or Lange coupler, microstrip low pass filter (LPF) and TRS [1-2].

The input signals for the 4-port ring hybrid are: 1) the reference LO input signal comes from 4-GHz NRO through the coupled port of 7-dB MBC and 2) the received RF signal comes from antenna through TRS and 4-GHz BMA [7-15]. The IF output signal is extracted from the mixer output through microstrip low-pass filter (LPF). The transmitted CW signal is directed from NRO to the antenna through the direct port of the 7-dB branch coupler and TRS. The design of the individual components of the L-band SOP-HMIC transceiver module with integrated TRS is performed completely with the aid of the full-scale computer simulation program developed by the authors [16-18] while the analysis and optimization are performed using the Aplan V7.61 software [19].

The microstrip substrate parameters with 50-Ω normalized impedance are: relative permittivity ( $\epsilon_r$ )

= 2.2, substrate height (H) = 0.7874 mm, and conductor thickness (T) = 0.005 mm.

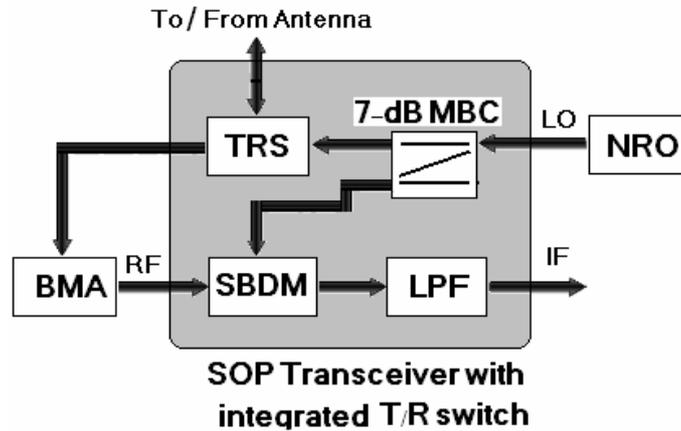


Fig. 1: Block diagram of L-band sensor including SOP-HMIC transceiver with integrated TRS.

### 3 Design of 7-dB MBC

The 7-dB MBC is used to direct the NRO output to the antenna through the TRS and to couple a reference signal to the SBDM [9-14]. The developed full-scale computer simulation program is used to design the 7-dB branch coupler operated at central frequency of 4 GHz. As a result of the developed program, the parameters of the 7-dB branch coupler are: width of series lines  $W_1 = 2.837\text{mm}$ , length of

series lines  $L_1 = 13.646\text{mm}$ , impedance of series lines =  $44.73\Omega$ , width of branch lines  $W_2 = 0.6925\text{mm}$ , length of branch lines  $L_2 = 14.198\text{mm}$ , and impedance of branch lines =  $100.1483\Omega$ . Figure 2 shows the Aplac configuration of the designed 7-dB MBC [15, 16]. Figure 3 shows the variation with frequency of  $|S_{21}|$ ,  $|S_{31}|$ , and  $|S_{41}|$  for the designed 7-dB MBC.

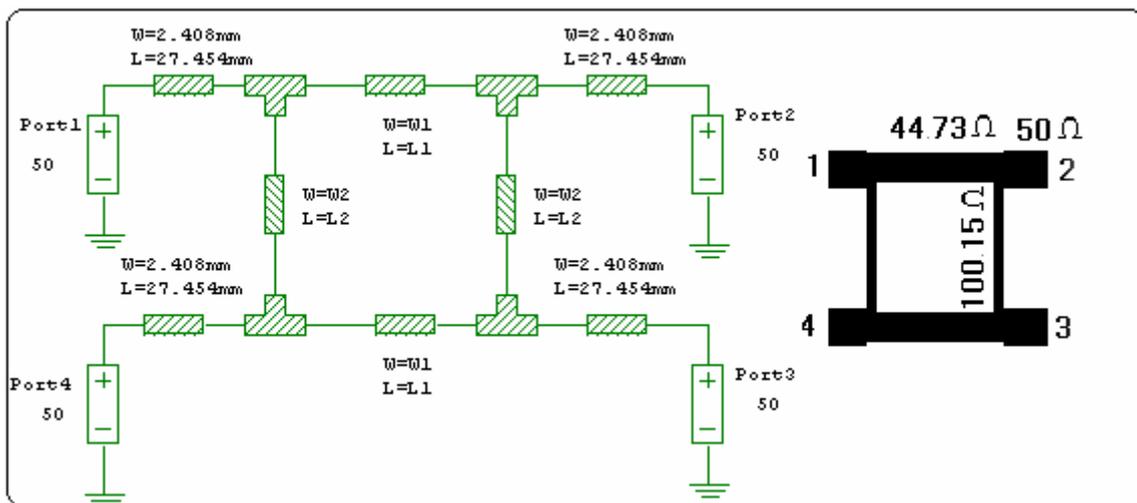


Fig. 2: The Aplac configuration of the 7-dB MBC.

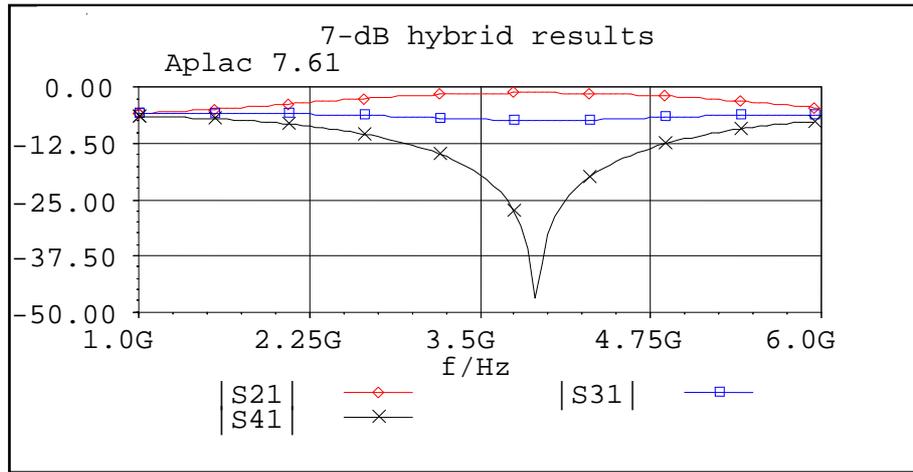


Fig. 3:  $|S_{21}|$ ,  $|S_{31}|$ , and  $|S_{41}|$  versus frequency for the designed 7-dB MBC.

### 4 Design of Microstrip Singly-balanced Diode Mixer

The design of a microstrip mixer is performed using the developed full-scale computer simulation program. The design is performed for a singly

balanced diode mixer with the following two stages [9-14]: 1) Design of hybrid coupler (rate-race or Lange coupler), 2) Design of matching circuit that matches the diode input impedance to the coupler.

#### 4.1 Design of rate-race coupler

The rate-race coupler is designed for the coupling factor  $C = 3$  dB at the operating frequency of 4 GHz.

As a result of the developed program, the parameters of the rate-race are [9-14]: total length of the rate-race line = 83 mm, length of  $(\frac{1}{4} \lambda_g)$  circular lines (R) = 13.94 mm, length of  $(\frac{3}{4} \lambda_g)$  circular lines = 41.81 mm, width (WR) of rate-race lines = 1.36 mm and impedance of circular lines = 70.75  $\Omega$ .

Figure 4 shows the Aplac configuration of the rate-race hybrid operated at 4 GHz. Figures 5 shows  $S_{21}$ ,  $S_{31}$ , and  $S_{41}$ , versus frequency for the rate race coupler operated at 4 GHz using Aplac V7.61 software.

It is seen that the values of  $S_{21}$  and  $S_{31}$  for the directed (port 2) and coupled (port 3) ports equal to 3dB while the port 4 is isolated ( $S_{41} > 55$  dB).

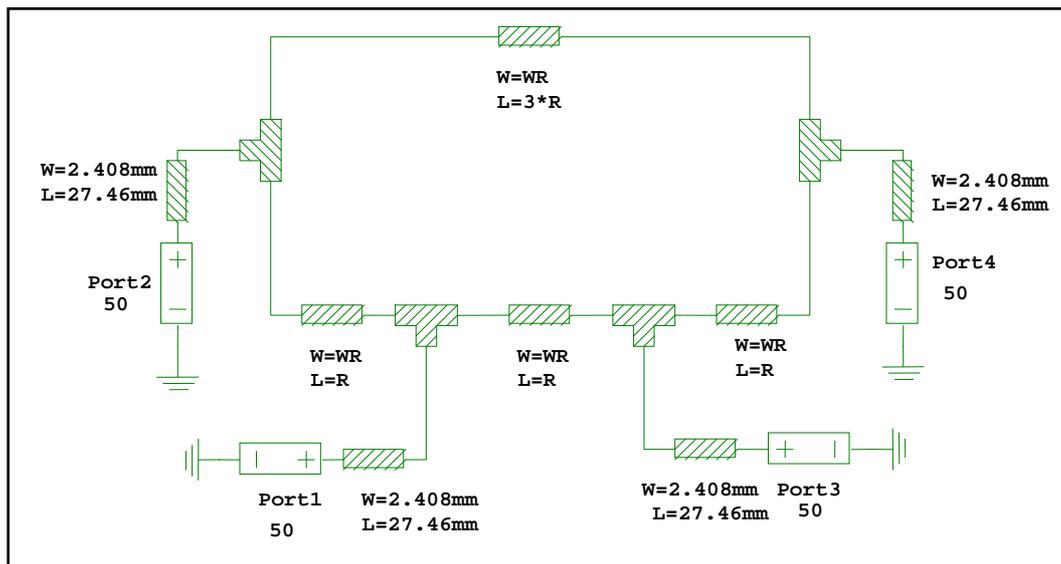


Fig. 4: Aplac configuration of the rate-race hybrid operated at 4 GHz.

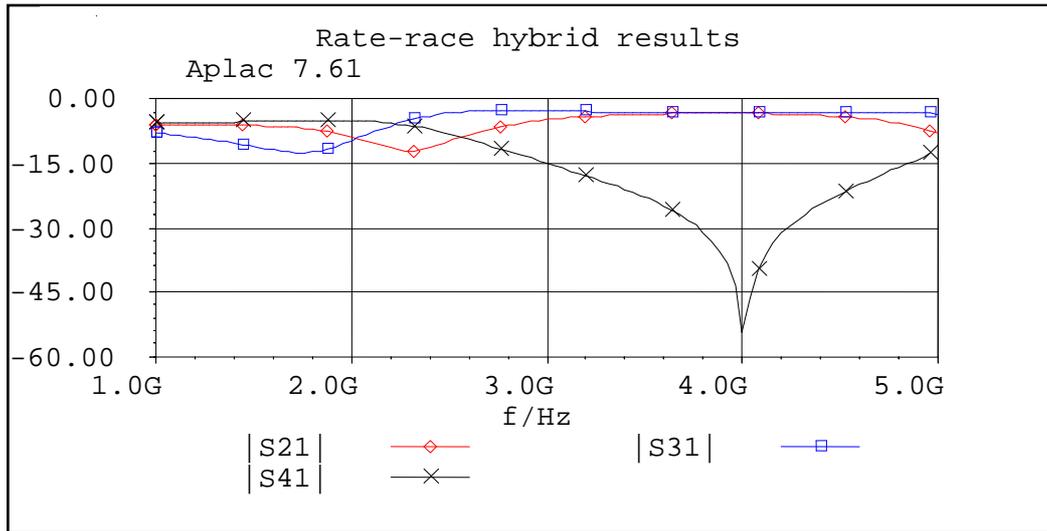


Fig. 5:  $|S_{21}|$ ,  $|S_{31}|$ , and  $|S_{41}|$ , versus frequency for the rate race coupler operated at 4 GHz.

### 4.2 Design of diode matching circuit

The Schottky barrier diode (5082-2765) is used for the design of the mixer [20-21]. The diode has the following parameters:  $R_J = 258 \Omega$ ,  $C_J = 0.255 \text{ pF}$ ,  $L_P = 0.435 \text{ nH}$ ,  $C_P = 0.085 \text{ pF}$ ,  $R_S = 14.5 \Omega$ , and the ideality factor = 1.02. The diode matching circuit is designed at 4 GHz. As a result of the developed program, the normalized input impedance and the

input reflection coefficient are:  $Z_{in} = 52.92 - j88.498 \Omega$ , and  $\Gamma_{in} = 0.65 \angle 47.42^\circ$ .

For the calculated normalized impedance and the input reflection coefficient, the lengths of and widths of the diode matching circuit are: length of series line = 13.854 mm, length of open circuit single stub = 9.118 mm, and width of series and shunt stub = 2.408 mm. Figure 6 shows the circuit layout of the designed 4-port-rate-race coupler with diode matching circuits.

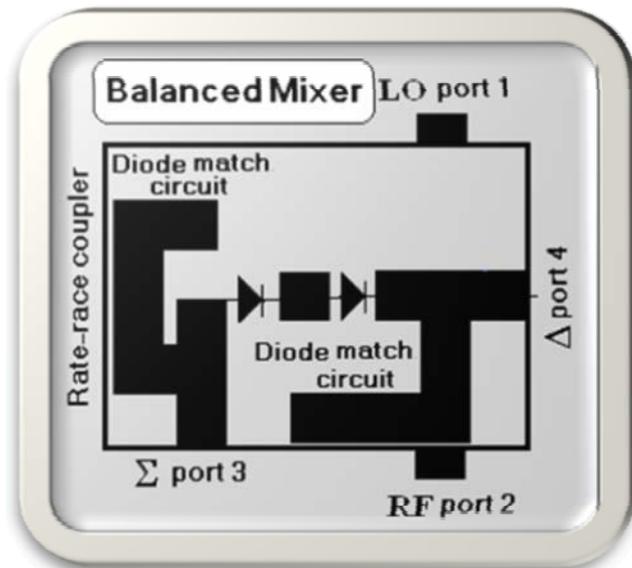


Fig. 6: Circuit layout of the designed 4-port rate-race coupler with diode matching circuits.

## 5 Design of LPF

The maximally flat lowpass prototype filter is used in the design of the LPF with the following

specifications: [9-13, 22-23]: the operating frequency,  $f_o = 4$  GHz, the cut-off frequency,  $f_c = 0.75$  GHz, the characteristic impedance of the series inductive is  $120 \Omega$ , and the characteristic impedance of the shunt capacitance is  $20 \Omega$ . One section maximally flat LPF is considered. As a result of our developed program, length ( $L_L$ ) and width ( $W_L$ ) of the inductive microstrip line are 17.755 mm and 0.45 mm, respectively. Length ( $L_C$ ) and width ( $W_C$ ) of the capacitive microstrip line are 32.407 mm and

8.069 mm, respectively. The attenuation at the operating frequency is 43.62 dB. The properties of a microstrip LPF are analyzed by computing the electromagnetic field distribution in the device across a spectrum of frequencies (1– 10) GHz. Figure 7 and 8 show the Aplac configuration and distributed/lumped description of the designed maximally-flat LPF. Figure 9 shows  $S_{21}$  (dB) and  $S_{11}$  (dB) versus frequency for the designed LPF.

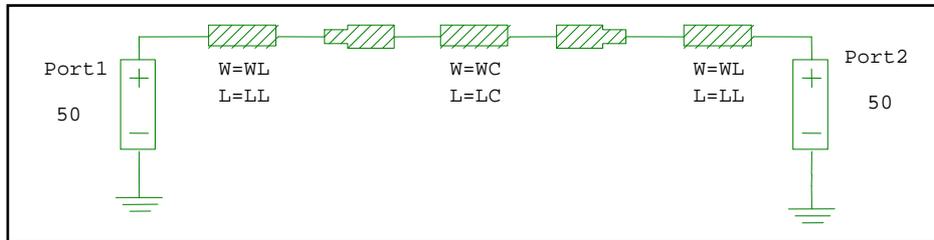


Fig. 7: The Aplac configuration of the designed LPF

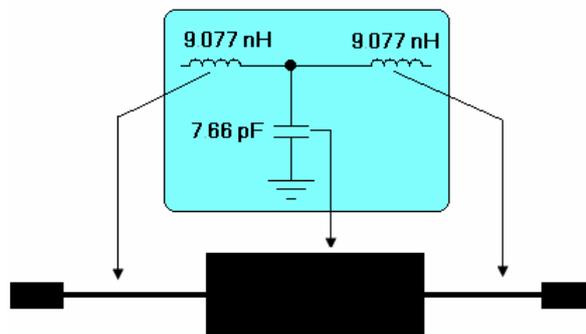


Fig. 8: The distributed and lumped one-section maximally flat LPF.

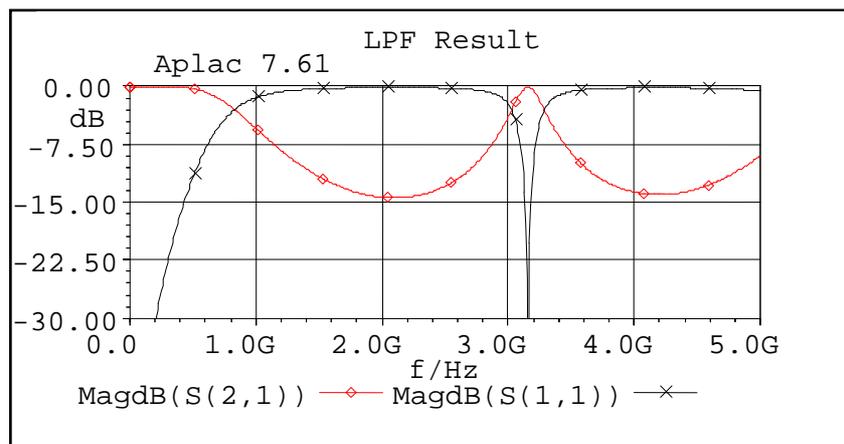


Fig 9:  $S_{21}$  (dB) and  $S_{11}$  (dB) versus frequency for the designed LPF.

### 5.1 Design of singly-balanced diode mixer with LPF using rate-race coupler

The final layout out of the designed singly-balanced mixer using rate-race coupler is analyzed and optimized using Aplac V7.61 software. Figures 10 and 11 show the Aplac configuration and AC

schematic circuit description of the final singly-balanced diode mixer with LPF. The circuit parameters are optimized using Aplac optimization package. The optimized circuit parameters are:  
Diode matching circuit:

- Length ( $L_{SE}$ ) and width ( $W_{SE}$ ) of the series lines are 9.088mm and 2.408 mm, respectively.
- Length ( $L_{ST}$ ) and width ( $W_{ST}$ ) of the open/single shunt stubs are 45.127 mm and 2.408 mm, respectively.

Rate-race coupler:

- Length of ( $1/4 \lambda_g$ ) circular lines ( $R$ ) = 11.11 mm,
- Width ( $W_R$ ) of rate-race lines = 1.364668 mm,

LPF circuit

- Length ( $L_L$ ) and width ( $W_L$ ) of distributed inductive lines are 20.751mm and 0.44571 mm, respectively.

- Length ( $L_C$ ) and width ( $W_C$ ) of the distributed capacitive line are 36.959 mm and 8.069 mm, respectively.

Figures 12 through 14 show VSWR,  $|S_{11}|$  and down conversion loss at RF-port for LO powers 5-15 dBm. Figure 15 and 16 show the waveform and spectrum of the IF output signal. Figure 17 shows the IF output power sweep for LO powers 5-15dBm. For the LO powers 5-15 dBm; as shown in figures; the VSWR is  $< 2.5:1$ , return loss is  $> 7\text{dB}$ , and the down conversion loss  $\cong 7\text{dB}$ .

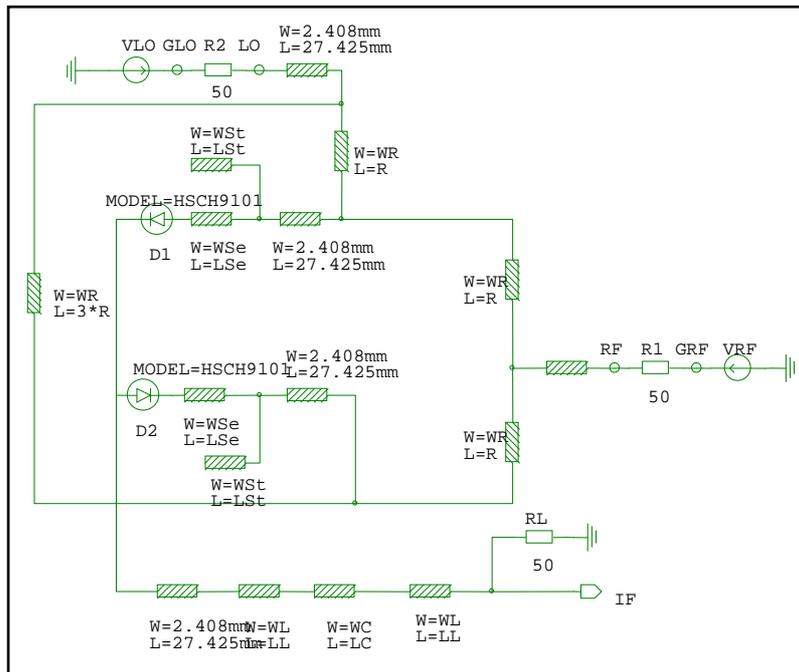


Fig. 10: The Aplac configuration of the final singly-balanced diode mixer with LPF.

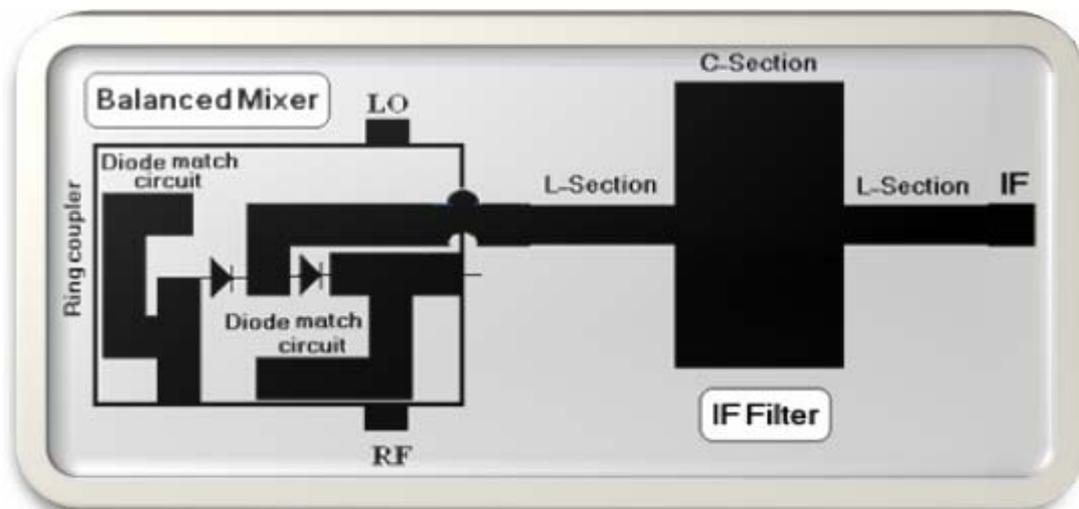


Fig. 11: AC schematic circuit description of the final singly-balanced diode mixer with LPF.

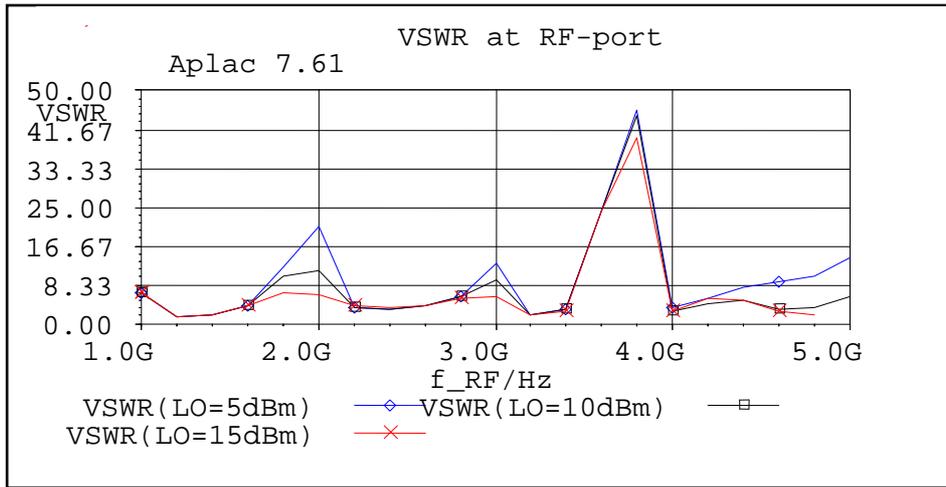


Fig.12: VSWR at RF-port at downconversion for LO powers 5-15dBm.

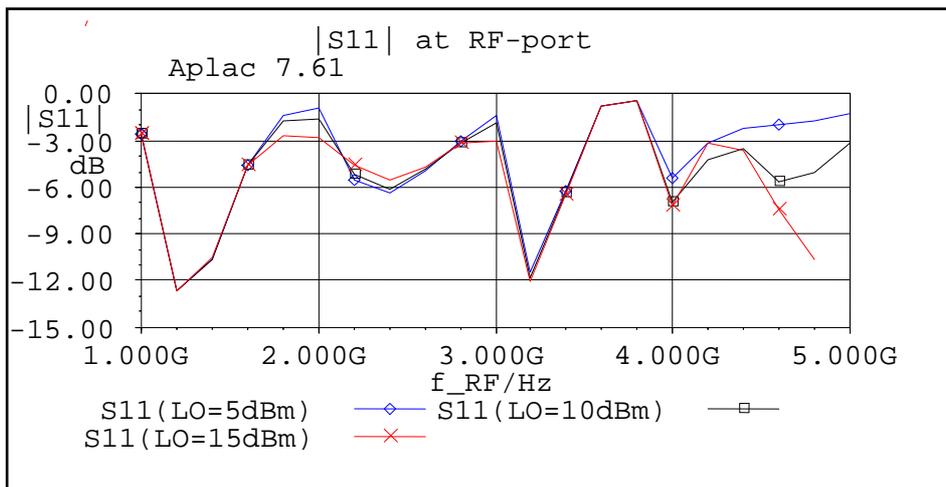


Fig. 13: |S11| at RF-port at downconversion for LO powers 5-15dBm.

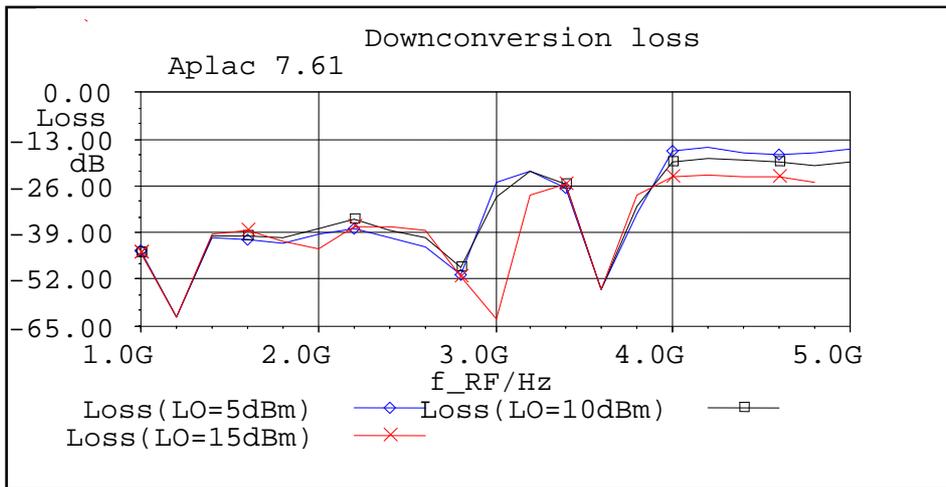


Fig. 14: Downconversion loss for LO powers 5-15dBm.

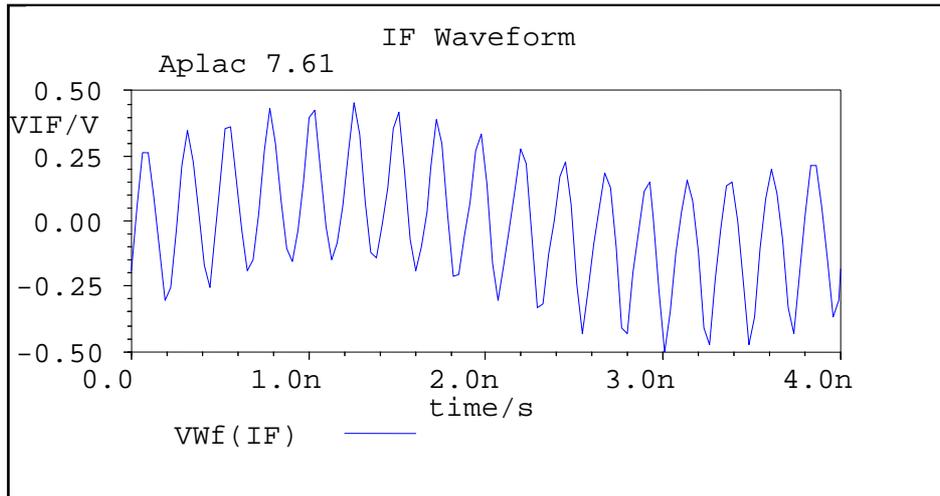


Fig. 15: The IF output waveform.

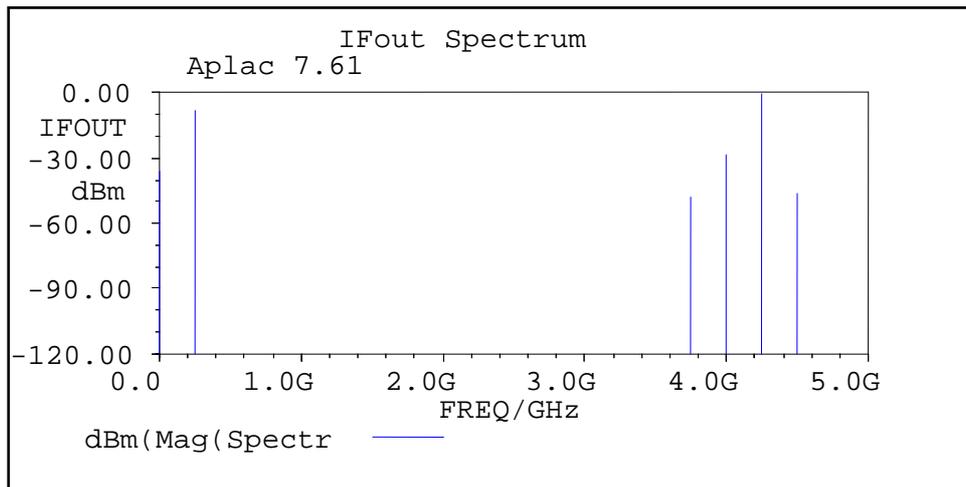


Fig. 16: The spectrum of the output signal for the designed SBDM.

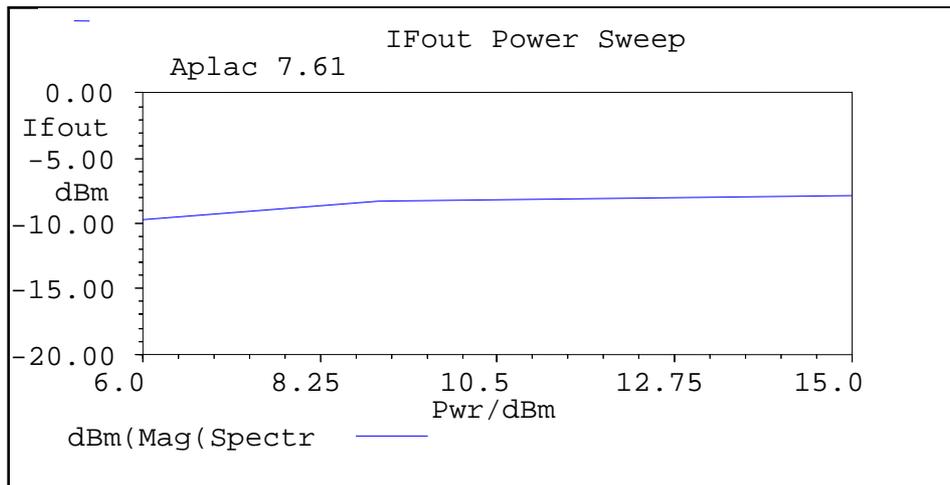


Fig. 17: IF output power sweep for LO powers 5-15 dBm.

**5.2 Design of singly-balanced mixer with LPF using Lange coupler**

The singly-balanced mixer can be implemented using Lange coupler instead of rate-race coupler [9-

14]. Figures 18 and 19 show the Aplac configuration and the AC schematic circuit description of the designed singly-balanced diode mixer using Lange coupler. The circuit is designed using the developed program and analyzed/optimized using Aplac V7.61. The designed circuit parameters are:

Diode matching circuit:

- Length ( $L_{SE}$ ) and width ( $W_{SE}$ ) of the series lines are 13.854 mm and 2.408 mm, respectively.
- Length ( $L_{ST}$ ) and width ( $W_{ST}$ ) of the open/single shunt stubs are 9.117 mm and 2.408 mm, respectively.

Lange coupler:

- Length ( $L_{Lange}$ ) and width ( $W_{Lange}$ ) of the strip line ( $L_{Lange}$ ) are 13.47 mm and 1.457 mm, respectively.

LPF circuit:

- Length ( $L_L$ ) and width ( $W_L$ ) of distributed inductive lines are 17.755 mm and 0.44571 mm, respectively.
- Length ( $L_C$ ) and width ( $W_C$ ) of the distributed capacitive line are 32.407mm and 8.069 mm, respectively.

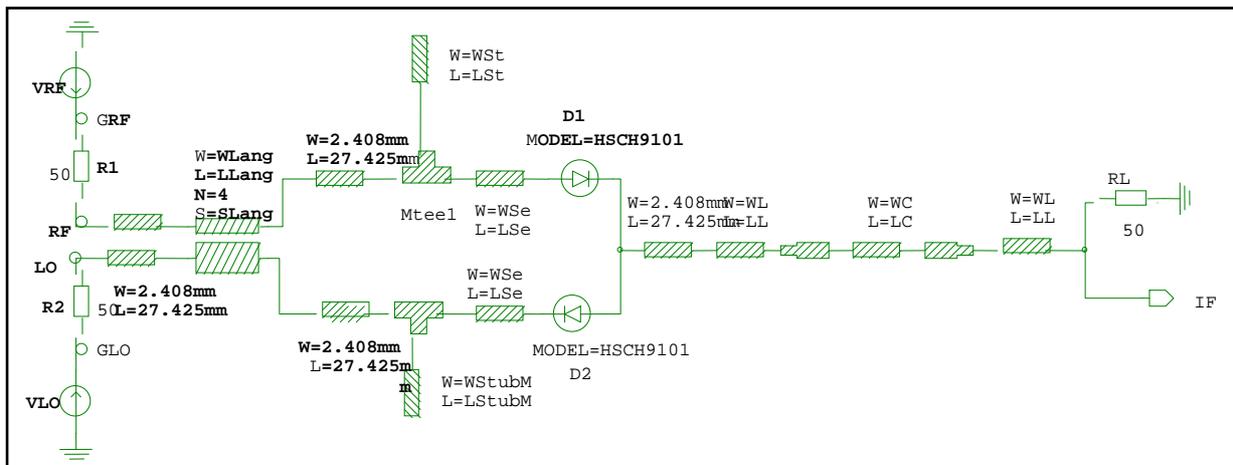


Fig. 18: the Aplac configuration of the final singly-balanced diode mixer using Lange coupler.

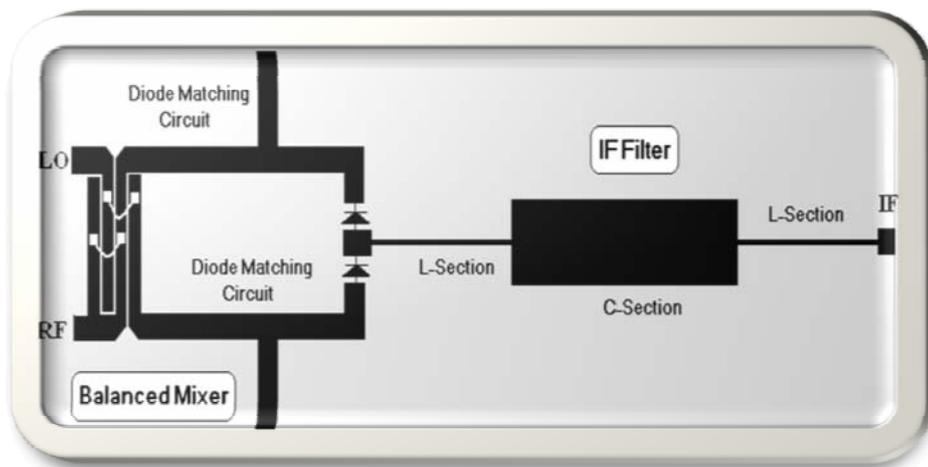


Fig. 19: The AC schematic circuit description of the final singly-balanced diode mixer using Lange coupler.

Figures 20 through 22 show VSWR,  $|S_{11}|$  and down conversion loss at RF-port for LO powers 5-15 dBm. Figure 23 and 24 show the waveform and spectrum of the IF output signal. Figure 25 shows the IF

output power sweep for LO powers 5-15 dBm. For the LO powers 5-15 dBm; as shown in figures; VSWR is  $< 2.5:1$ , the return loss is  $> 7$  dB, and the down conversion loss  $\cong 20$  dB

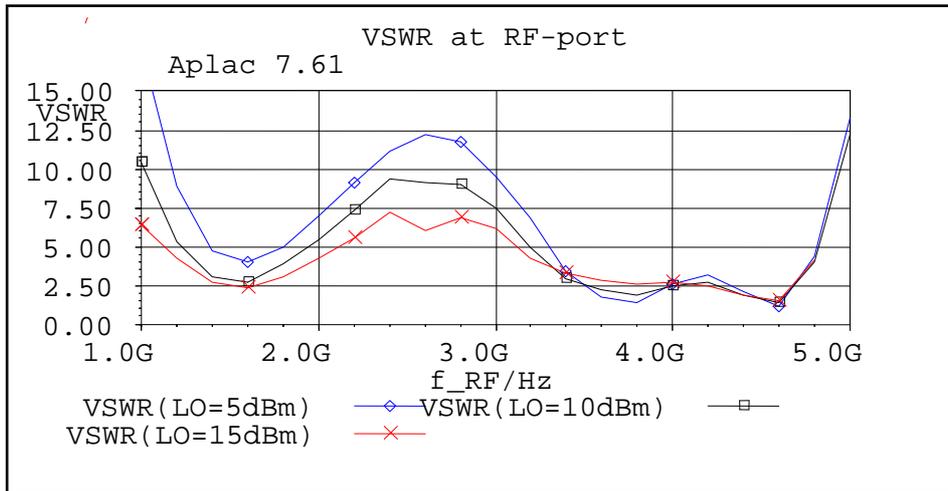


Fig.20: VSWR at RF-port at downconversion for LO powers 5-15dBm.

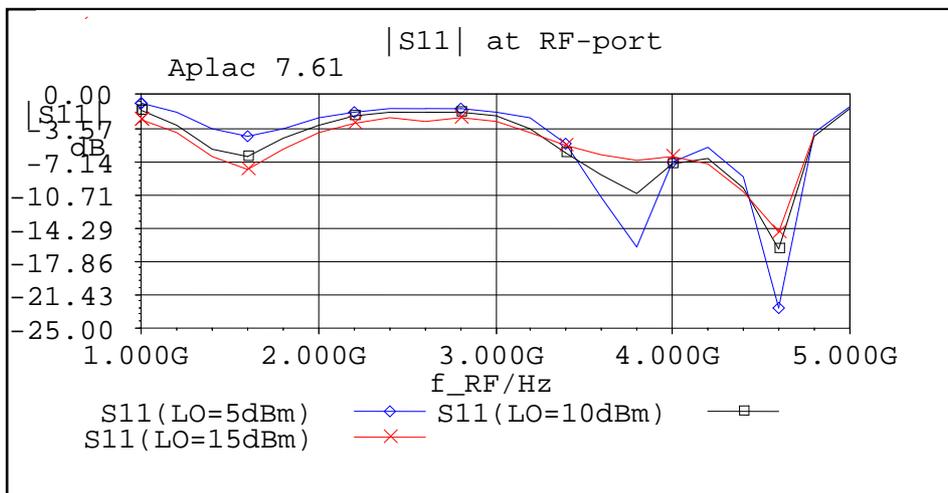


Fig.21: |S11| at RF-port at downconversion for LO powers 5-15dBm.

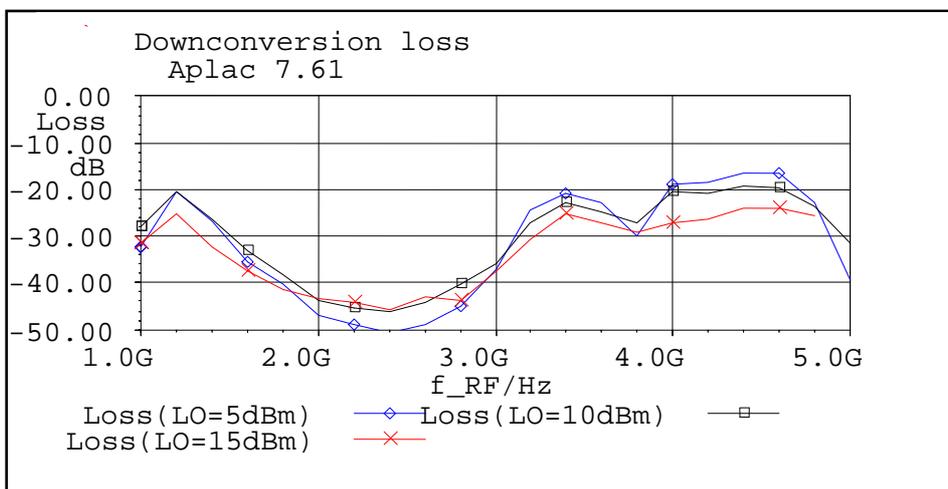


Fig.22: Downconversion loss for LO powers 5-15dBm.

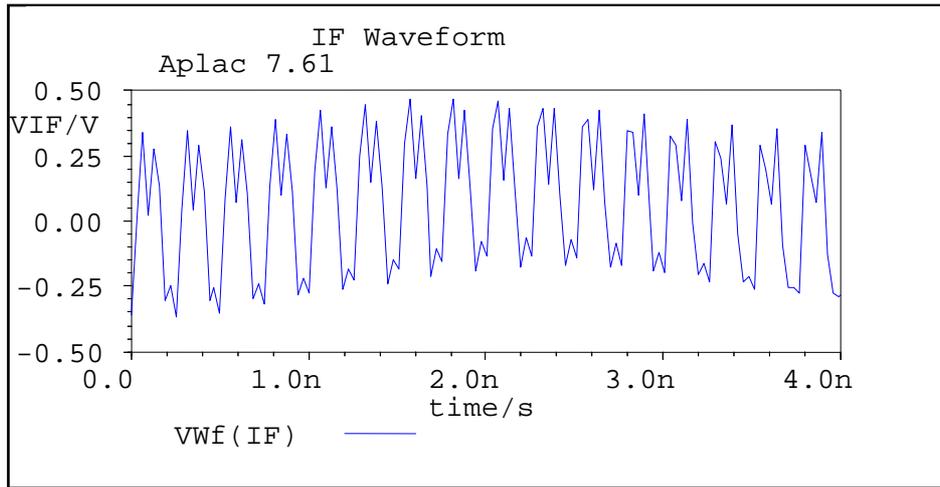


Fig. 23: The IF output waveform.

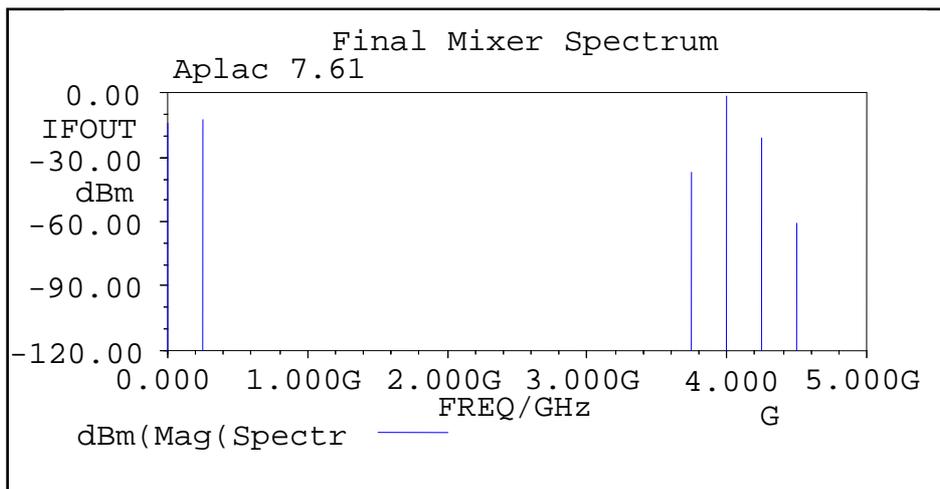


Fig. 24: The spectrum of the output signal for the designed SBDM.

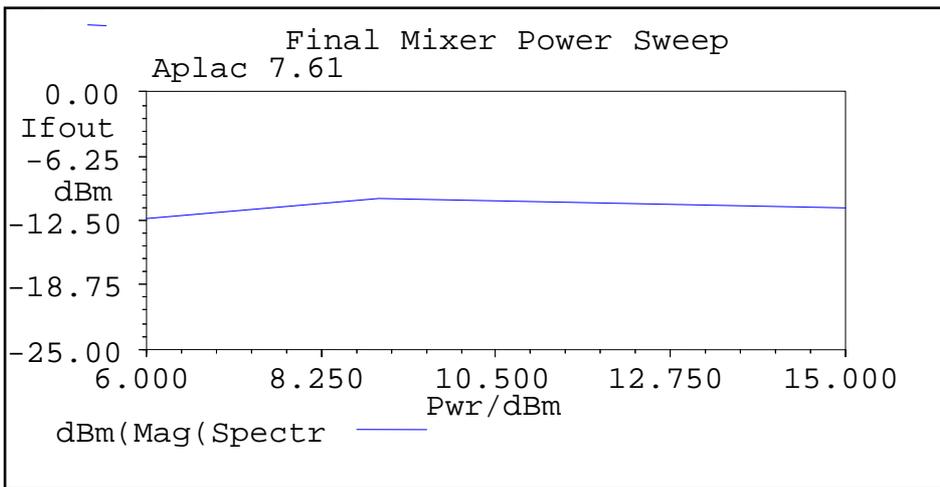


Fig. 25: IF output power sweep for LO powers 5-15 dBm.

### 6 Design of Distributed TRS

One of the most important building blocks for today's wireless communication equipment is a high performance RF switch. Mainly, the TRS are a class

of Tuned-shunt SPDT Switch, used by designers of Communications Transceivers to alternately connect the transceiver's antenna to either the Transmitter or to the Receiver [23-29]. The SPDT switch utilizes a

microwave PIN diode as a semiconductor device that operates as a variable resistor at RF and microwave frequencies. A PIN diode is a current controlled device whose structure comprises a region of high resistivity intrinsic material sandwiched between a region of P-type semiconductor and N-type semiconductor. When the PIN diode is forward biased, charge carriers are injected into the I region lowering its resistance. When the diode is zero-biased or reverse biased the I region is of high resistance, in the region of several kilowatts.

An ideal TRS is characterized by: 1) Low insertion loss in the selected transmission path to minimize receiver noise figure and maximize transmitter power delivered to the antenna, 2) High off-state isolation in the deselected transmission path to reduce interactions and the potential of the high-

power transmitter damaging sensitive receiver circuitry, 3) High-power handling capability to support longer-range operation, 4) Fast transitions between switching states to reduce radar blind times and increase throughput in communication applications, 5) Low cost to reduce implementation expenses, 6) Small physical size to support tight-fitting and portable applications, and 7) Simple drive/control circuit requirements to reduce complexity and power consumption.

In this paper, the TRS is implemented using a tuned-shunt SPDT switch with PIN diode HP 5082-3040. The design methodology adopted is to absorb the off-state capacitance of the PIN diode into a LPF structure. The design methodology; depicted in Figure 26; has mainly five steps.

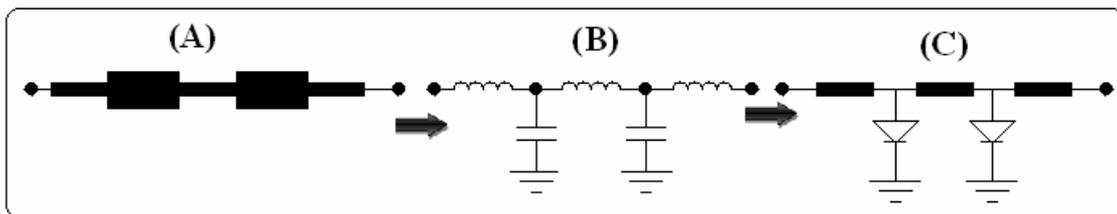


Fig. 26: The design methodology path: (A) Distributed LPF, (B) Equivalent lumped LPF, (C) LPF with high impedance series transmission line and shunt PIN diodes.

The starting step is to design a maximally-flat microstrip LPF with cut-off frequency slightly above the required operating frequency. The authors developed computer simulation program and Aplac V7.61 software are used to design, analyze and optimize the distributed LPF. Table 1 illustrates the

designed parameters of the distributed LPF operated with cut-off frequency 7 GHz. Figure 27 and 28 show the Aplac configuration of the LPF and the performance of the distributed LPF.

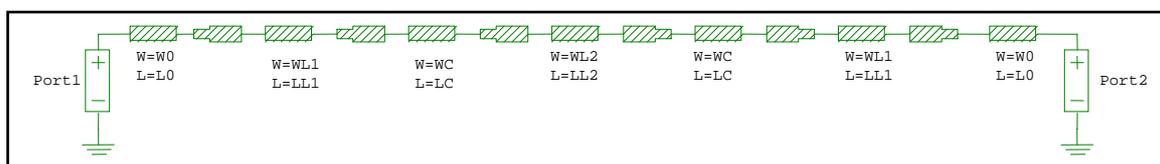


Fig. 27: Aplac configuration of the distributed LPF.

Table 1: The designed parameters of the distributed LPF

Parameters	Value
Length of branch distributed inductive line ( $L_{L1}$ )	1.336 mm
Width of branch distributed inductive line ( $W_{L1}$ )	0.445 mm
Length of inside distributed inductive line ( $L_{L2}$ )	5.286 mm
Width of inside distributed inductive line ( $W_{L2}$ )	0.445 mm
Length of distributed capacitive line (LC)	2.352 mm
Width of distributed capacitive line (WC)	8.060 mm

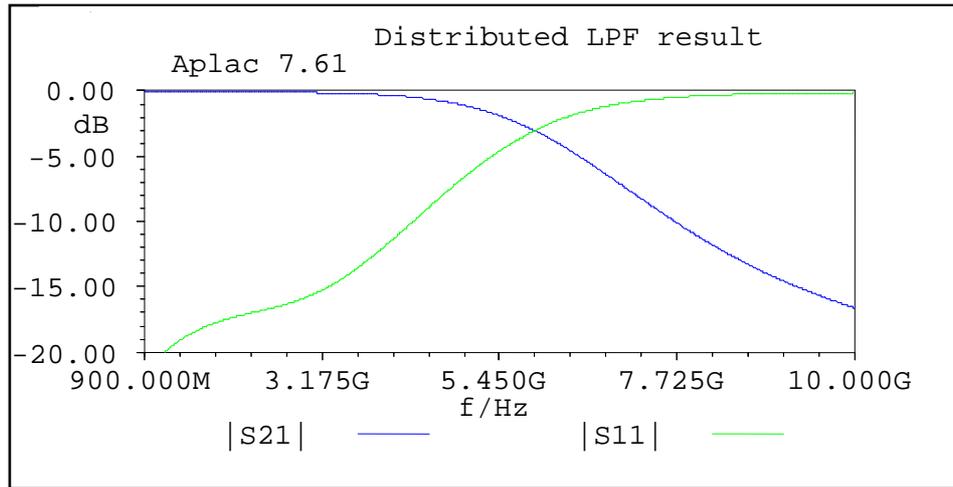


Fig. 28: |S11| and |S21| of the distributed LPF.

The second step is to calculate the lumped elements of the LPF so as to get the value of the shunt capacitance of the LPF. Table 2 illustrates the

designed parameters of the lumped LPF. Figure 29 shows the Aplac configuration of the lumped LPF.

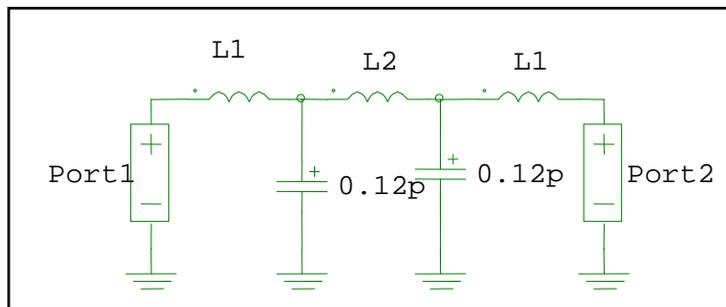


Fig. 29: Aplac configuration of the lumped LPF.

Table 2: The designed parameters of the lumped LPF

Parameters	Value
Inductance of the branch distributed inductive line (L1)	200.005pH
Inductance of the inside distributed inductive line (L2)	2.767nH
Capacitance of the distributed capacitive line	0.12pF

The third step is to select the proper PIN diode whose off-state capacitance near the value of the

shunt capacitance of the LPF and then to replace all of the shunt capacitors with off-state capacitances of the selected PIN diode and then calculate the LPF performance. The silicon PIN diode HP 5082-3040 (off-state capacitance = 0.2 pF and  $R_s = 11 \Omega$ ) is selected for the TRS application. The LPF with PIN

diode instead of capacitive distributed line is designed and analyzed using the developed computer simulation program and Aplac software. Figure 30 and 31 show the Aplac configuration and the performance results of LPF with series distributed inductive lines and shunt PIN diodes. As shown in figure, the insertion loss < 1.7 dB and the return loss > 6 dB over the range (0-10GHz).

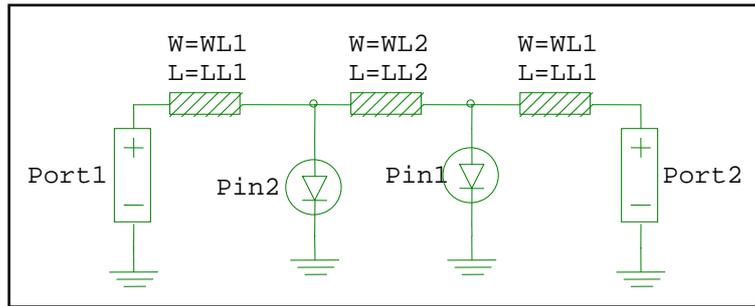


Fig. 30: ApIac configuration of the LPF with series distributed inductive lines and shunt PIN diodes.

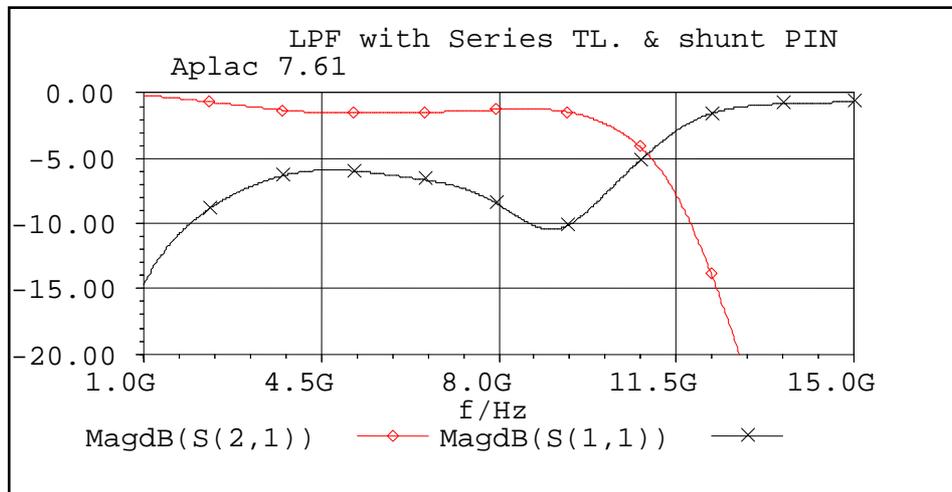


Fig. 31:  $|S_{11}|$  and  $|S_{21}|$  of the LPF with series distributed inductive lines and shunt PIN diodes.

The fourth step is to optimize the performance of the LPF with series distributed microstrip inductive lines and shunt PIN diodes. The Filter optimization is performed using the Aplac optimization package. Table 3 illustrates the optimized parameters of the

distributed LPF. Figure 32 shows the optimized performance of LPF with series distributed microstrip inductive lines and shunt PIN diodes. As shown in the figure, the insertion loss  $< 0.6$  dB, and the return loss  $> 14$  dB.

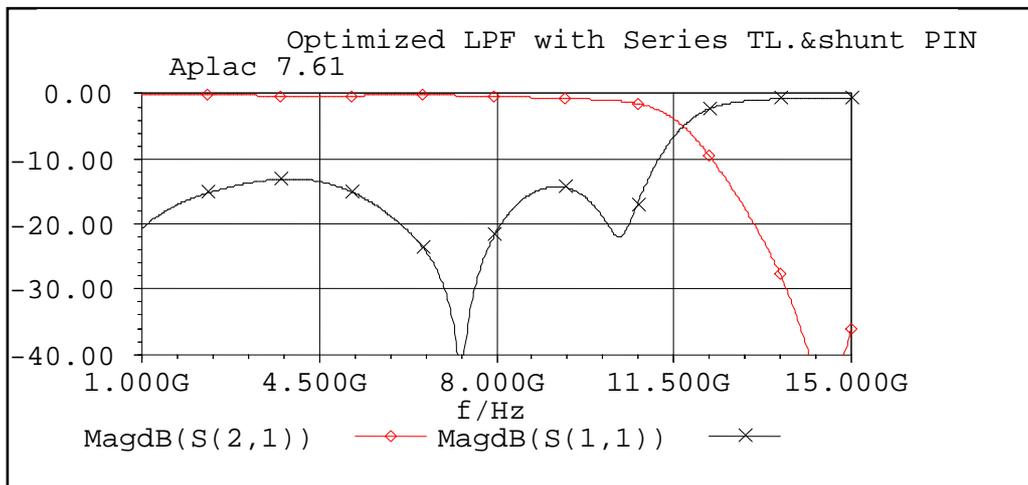


Fig. 32: Optimized  $|S_{11}|$  and  $|S_{21}|$  versus frequency of the LPF with series distributed inductive lines and shunt PIN diodes.

Table 3: The optimized designed parameters of the distributed LPF

Parameters	Value
Length of branch distributed inductive line ( $L_{L1}$ )	1.336 mm
Width of branch distributed inductive line ( $W_{L1}$ )	0.445 mm
Length of inside distributed inductive line ( $L_{L2}$ )	5.286 mm
Width of inside distributed inductive line ( $W_{L2}$ )	1,445 mm
Length of distributed capacitive line ( $L_C$ )	2.352 mm
Width of distributed capacitive line ( $W_C$ )	8.060 mm

The final fifth step is to add the required biasing components to control the diodes operation. Figure 33 shows the AC schematic diagram of the TRS with

the biasing networks. When positive bias is applied to bias TX port and negative bias is applied to bias RX port, diodes D1 and D2 are forward biased into a low resistance state, while diodes D3 and D4 are

reverse biased into a high resistance state. The RF power flows from antenna port to RX port. When positive bias is applied to bias RX port and negative bias is applied to bias TX port, Diodes D3 and D4 are forward biased into a low resistance state, while diodes D1 and D2 are reverse biased into a high resistance state. The RF power flows from antenna port to TX port 1.

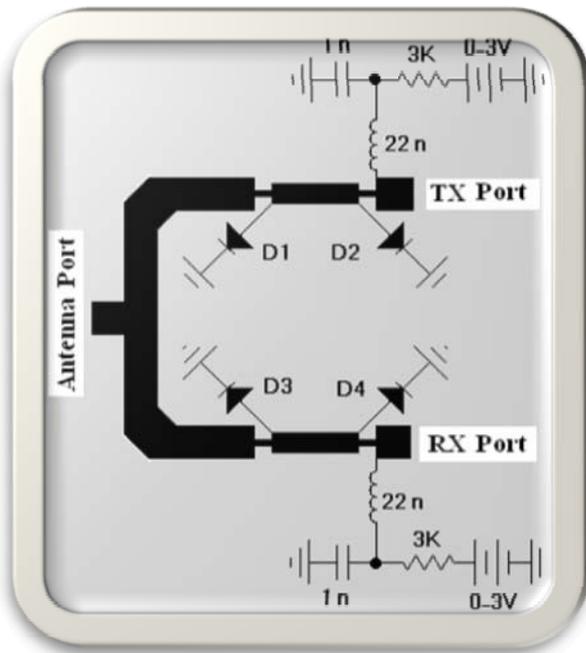


Fig. 33: The AC schematic diagram of the TRS with the biasing networks

### 7 Final AC Schematic Diagrams of SOP-HMIC Transceiver Modules

Figures 34 and 35 show the final AC schematic

diagram of the designed SOP-HMIC transceiver modules with integrated TRS using rate-race and Lange couplers.

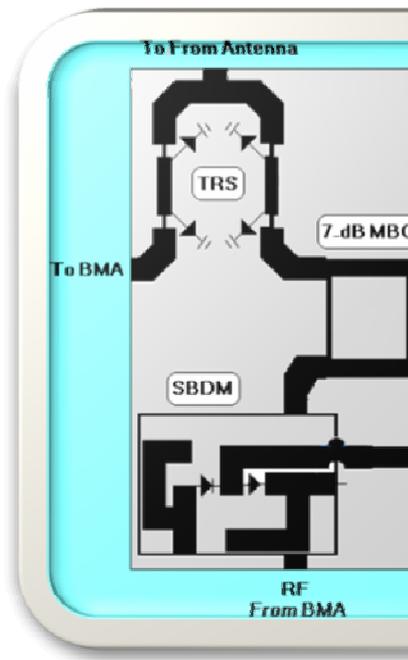


Fig. 34: the final AC schematic diagram of the designed SOP-HMIC transceiver module with integrated TRS using rate-race coupler.

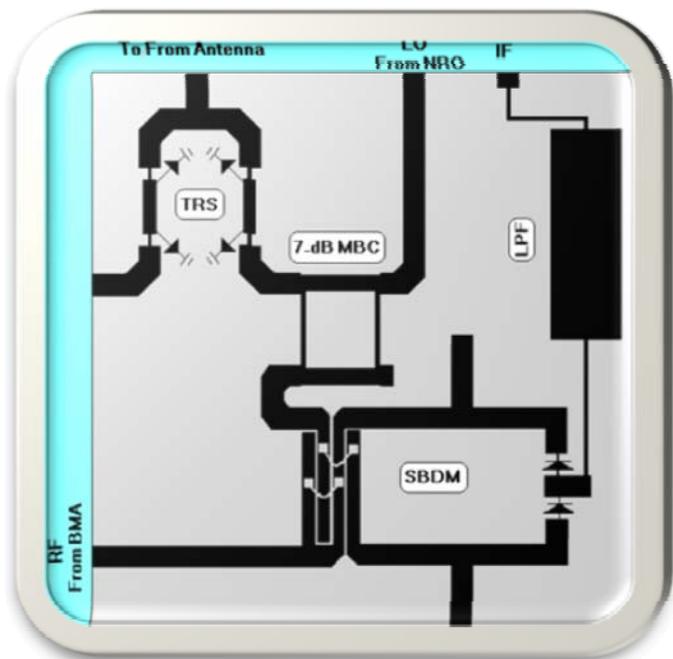


Fig. 35: the final AC schematic diagram of the designed SOP-HMIC transceiver module with integrated TRS using Lange coupler.

## 8 Conclusion

Distributed microwave integrated circuits have been increasingly adopted in many electronic systems

such as communication, radar, electronic warfare, navigation, surveillance, and weapon guidance systems. These systems are mostly military in nature and have been supported strongly by the defense community. This work presented a complete design, analysis and optimization of SOP-HMIC transceiver modules. The modules contain 7-dB splitter using branch coupler, singly-balanced diode mixer using either rate-race or Lange coupler, maximally-flat LPF, and TRS. A full-scale computer simulation program developed by the authors is used for the designed modules. The designed modules are analyzed using the APlac V7.61 microwave package. A new approach for designing of the TRS is proposed. This approach depends on the design of distributed LPF, calculates the value of the capacitance of the capacitive microstrip line, replaces this capacitance with a proper PIN diode, and finally optimized the LPF with distributed inductive line and PIN diode for a certain performance. The complete design and analysis of the individual components are presented. The complete layouts of the designed transceiver modules are introduced. The designed module can be used in many applications, including: wireless communications, radar systems (ground based, airborne, personal vehicles), target detection and identification, deep space communications, and radio spectrometry.

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