The Circuit Design of Current-Mode Image Sensor Embedded Smooth Spatial Filter With Flash A/D Converter

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Abstract: - The paper presents a current-mode CMOS image sensor embedded smooth spatial filter algorithm with a flash analog-to-digital (A/D) converter. The sensor includes a 66×66 pixel array with an on-chip 6-bit A/D converter that can identify the output value of pixels in gray level resolution. The last row of pixel cells (1 ×66) based on the double sampling is used for reducing fixed pattern noise (FPN). Processing circuits are dedicated for the spatial filter algorithm and support reusability to increase the image processing speed and to reduce the design complexity and chip area. The sensor chip has been designed and implemented in TSMC 0.35μm 2P4M CMOS mixed-mode process. Experimental results show that each pixel occupies a area of 15.8μm×10.6μm with a fill factor of 37.2%. The power consumption is 35.15mW when the sensor operates at 175 frames/second.

Key-Words: - Image senser, smooth spatial filter, Flash A/D converter, pixel cell, CMOS process.

1 Introduction

Charge-coupled devices (CCDs) give superior image quality and their technologies are used for high resolution image sensors. Unlike CCD, CMOS image sensor [1] can be fabricated by the standard CMOS process. It has the advantages of low power consumption, high frame rates, and easy integration with other back-end processing circuits [2].

There are extensive research efforts [3,4,5] to enhance the performance of CMOS image sensor by adopting better designs of digital and analog circuits. Especially, they concentrate the designs of active pixel sensor (APS) to improve its function. Some literatures [6,7] associate a CMOS image sensor with analog-to-digital (A/D) conversion in advance. They integrate image sensor, A/D converter, and back-end imaging processing circuits into a chip using the advanced technologies of semiconductor fabrication. Moreover, the approaches of embedding analog mask filter in a CMOS image sensor [8,18] can reduce cost and improve the captured speed and simplex design.

Recently, many literatures associated different new developed technologies, for example, low-noise readout [19,20], time-to-first spike arbitration [21], in-pixel ADC [22], and dynamic extension, into a CMOS image sensor for improving their performance.

In this paper, a CMOS image sensor embedded *smooth spatial filter* (SSF), an effective image preprocessing algorithm, is implemented in TSMC 0.35um 2P4M CMOS mixed-mode process. It not only successfully integrates back-end circuits including *transimpedance amplifier* and *analog-to-digital converter*, but also increases the efficiency of the use of the chip area and improves the readout speed around 175 frames per second. The structure using the SSF through a 3×3 in-pixel matrix can suppress fixed pattern noise by the current-mirror judgment mechanism, the manner is simply. The sensor chip identifies the outcome value of pixels in gray level resolution. It can be embedded in system-on-a-chip (SOC).

The remainder of this paper is organized as follows. Section 2 gives the architecture of proposed CMOS image sensor. The architecture consists of two major parts, front-end and back-end circuits. The designs of front-end and back-end circuits are presented in details in Section 3 and Section 4, respectively. The chip implementation of whole architecture is stated in Section 5. Finally, the conclusion for the proposed image sensor is remarked in Section 6.

2 The Architecture of Proposed Image Sensor

The architecture of our proposed image sensor is shown in Fig. 1 and the sensor can be realized in a standard 0.35μm CMOS process. The block diagram of the sensor consists of two parts, front-end and back-end circuits. The front-end part is the major body of the sensor that includes a 66×66 pixel array, row selector, column-processing circuit, and column selector. The back-end part contains the post-

processing circuit, transimpedance amplifier (TIA), and 6-bit analog-to-digital converter (ADC).

The sensor operation is performed in three simplified steps. First, the electrons excited by light are collected and converted into an electrical signal with noise reduction by pixel array in the front-end part. Then, the electrical signal is transferred to the post-processing circuit of the back-end by column and row selectors to be a proper analog output. At the end, the output signal is completely converted to be a digital code by TIA and ADC.

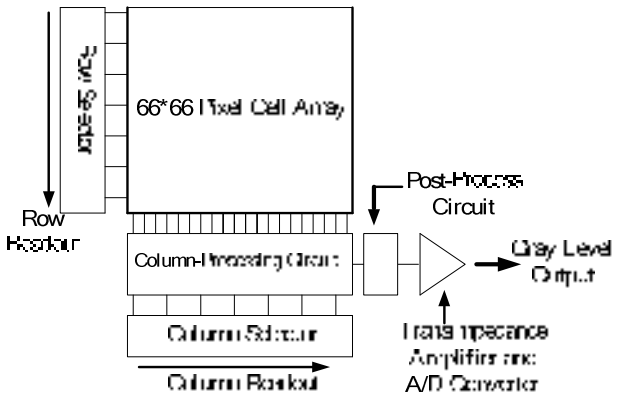


Fig. 1 The architecture of our proposed image sensor.

The architecture presents an embedded smooth spatial filter (SSF) which is an effective image preprocessing algorithm. Generally, a picture is composed of m × m pixels, every central pixel f_0 in 3×3 group matrix of pixels as shown in Fig. 2 is often affected by the surrounding pixels because the overall picture must be smooth. The image quality is improved using a decision algorithm to determine the output. The binarization approach for the output has been presented in [8]. We improve the approach with reading the output of pixels in gray level resolution. A central pixel f_0 is compared with the average of the surrounding pixels, $f_1, f_2, \ldots$, and f_8, to determine that f_0 should be represented as a digital code.

$$\frac{1}{8}\sum_{i=1}^{8} f_i - f_0 \geq 0 \Rightarrow \text{Output gray level} \qquad (1)$$

where f_i is the pixel value of a picture, and f_0 is determined by comparing the central pixel, f_0, with the average of the surrounding pixels. Then, the 3×3 group matrix is computed, one column to the right of the last one.

For the architecture, the column-processing circuit is used to sum electrical signals from pixels in a 3×3 matrix which is determined by the above spatial filter algorithm. The post-processing circuit receives the original pixel value and the average pixel signal around the central pixel to determine the central pixel value. Row and column selectors are used to determine three rows' and columns' pixel signals in each readout cycle. The selected nine signals are summarized by column-processing circuit. Finally, the column selector transfers the summarized value to next process. Therefore, the proposed architecture can support reusability to increase the image processing speed, and to reduce the chip area and the complexity of design circuits.

f_1	f_8	f_7
f_2	f_0	f_6
f_3	f_4	f_5

Fig. 2 A 3×3 matrix of pixels with the central pixel f_0.

3 The Design of Front-End Circuits

In the proposed architecture of image sensor shown in Fig. 1, the front-end part is the major body of the sensor which embedded an effective image preprocess of smooth spatial filter algorithm. The front-end circuits include a 66×66 pixel array, row selector, column-processing circuit, and column selector. These circuits are designed in details as the following subsections.

3.1 Pixel Cell

Figure 3(a) shows our proposed pixel cell which is modified from [8] that the reset transistor of the circuit is replaced by a NMOS structure. The pixel cell consists of three stages, a $n+_{\square Psub}$ type of photo-diode and a reset transistor (Mr), a source follower (Mt) and a current mirror (M1-M3), and row selectors (M4-M5) based on current-output cells. An output current *out1* is used as the input path *input1* of post-processing circuit. An *out2* is used as the column current path *Icolumn* of column-processing circuit.

The readout operation based on the current mode is simpler rather than that of the voltage mode. It can usefully reduce circuit complexity and increase readout speed. However, the current readout mode has the major drawback of larger *fixed pattern noise* (FPN) in the pixel cell which should be reduced in advance.

Figure 3(b) presents the layout of proposed pixel cell which occupies 15.8um×10.6um. The cell includes seven transistors and a photodiode with a fill factor of 37.2%. A metal layer shielding is used to cover on the layout of the pixel cell excluding the photodiode that prevents noise sensing caused by incident light.

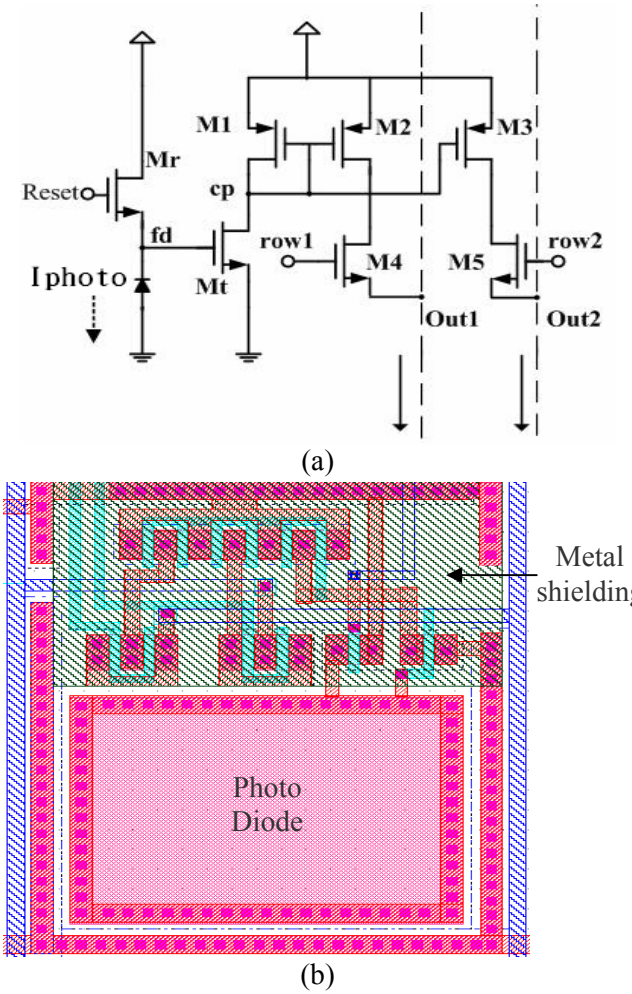


Fig. 3 (a) The circuit and (b) layout of proposed pixel cell.

Figure 4 shows the simulation result of a pixel cell. The result shows that illumination intensity converts the photocurrent from 50*n*A to 350*n*A to correspond to the weak light to the strong. A cycle from reset to exposure takes 5*m*s only.

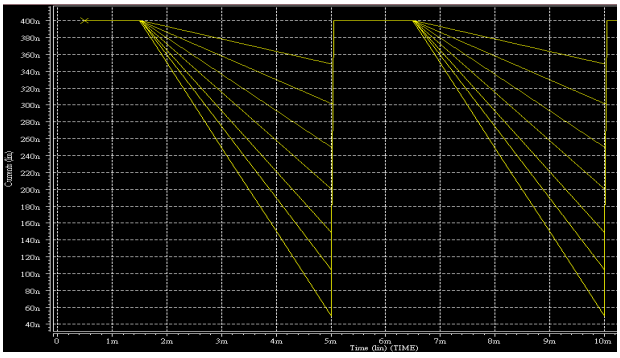


Fig. 4 Illumination vs. photocurrent of a pixel cell.

Basically, FPN exists in pixel output values due to the device geometry and the interconnect variation. We employ the correlation double sampling technique referred from the literatures [9,10] to eliminate the column FPN. At the bottom of the pixel array, the last row of pixel cells (1×66) which is shielded over its entire area from incident light by a metal layer is specifically added for the purpose of FPN reduction. The readout signal from the shielded row of cells remains as a reference value. As the incident light excises the photodiode to generate a photocurrent, after exposure and readout, the control signals determine which pixel signal and which pixel-shield signal is read out. The signal readout is transferred to the subtraction unit in the column-processing circuit. Since the two signals pass through a single readout circuit, the variations of FPN in the readout are cancelled by the subtraction operation.

3.2 Column-Processing Circuit

Figure 5 shows the column-processing circuit that controls signal currents from pixels and transfers the currents to the post-processing circuit by row and column selectors. The signal current *Icolumn*(*i*) is transferred from the current path *out2* of the selected pixel cell. A group of columns can be selected by the column selector via control signals *Ccol*(*i*) and an output current is then transferred to the post processing circuit.

As shown in Fig. 5, the current on *output1* path is the sum of *column1*, *column2*, and *column3*. It includes signals which consist of nine pixels combined with three rows and three columns. Then, the current on *output2* is the sum of *column2*, *column3*, and *column4*. Thus, the complete output results have good reusability and decrease the circuit complexity for chip design.

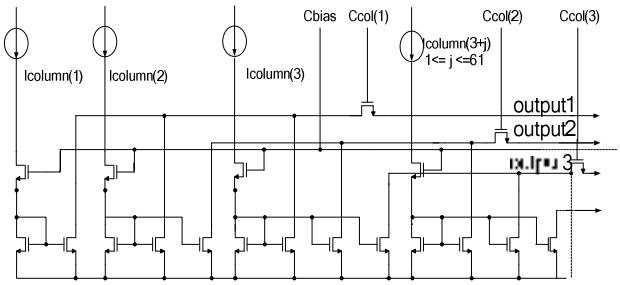


Fig. 5 Column-processing circuit.

3.3 Row and Column Selectors

The row selector is composed of D-type flip-flops and logic gates to form a shift register. The operation of row selector must be complied for the spatial filter algorithm. Row selector controls three rows at the same time to obtain the photocurrent. Figure 6 shows the simulation result, Line1 shows that row1, row2, and row3 turn on at the same time and Line2 shows that row2, row3, and row4 turn on at next same time. It satisfies smooth spatial filter algorithm. The difference of column selector from the row selector is only that controls single switch at a given time.

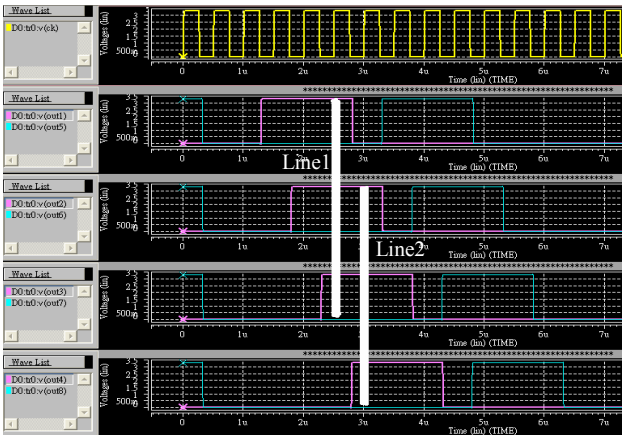


Fig. 6 The simulation of row selector.

4 The Design of Back-End Circuits

The back-end part is tightly followed the electrical signal outputted from the front-end part. Then, the signal is transferred to be a proper analog output by the post-processing circuit. And then the analog signal is converted to be digital codes by TIA and ADC. These circuits are implemented in details as the following subsections.

4.1 Post-Processing Circuit

Figure 7 shows a post-processing circuit. The *input1* comes from the current path *out1* of a pixel cell which is the value of central pixel. Another *input2* comes from the output current path of column-processing circuit which is the sum of nine pixels. They are transformed together to the output in the circuit. We can obtain the output result of the difference from the two input signals and then determine whether the central pixel in the 3×3 matrix is a value in output current. Bias voltages Vb1 and Vb2 are used to control the output current. The current is then transferred as the input of transimpedance amplifier.

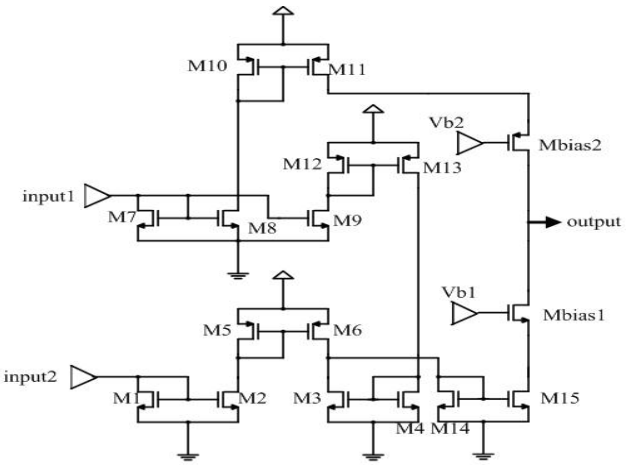


Fig. 7 Post-processing circuit.

4.2 Transimpedance Amplifier

Figure 8 shows the transimpedance amplifier (TIA) that consists of four stages, bias network, regulated cascode (RGC), current amplifier, and output buffer. The input current *Iin* comes from the output of post-processing circuit and the output voltage *Vout* is used to ADC for converting digital codes.

Bias network provides reference currents. The regulated cascode [11] is used as an input current buffer to create lower input impedance. The current amplifier is a current mirror. The current gain is determined by the respective ratio of W/L and is relatively stable over temperature and process variations. The voltage buffer with lower output impedance converts the input current to output voltage by the feedback resistor (Mr).

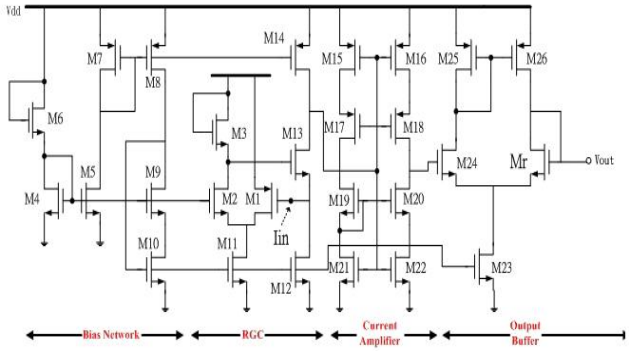


Fig. 8 Transimpedance amplifier.

Figure 9 shows the simulation result for TIA. The input currents of 50*n*A to 350*n*A are converted to be the output voltages of 0.75V to 3.05V, respectively, which can be applied to A/D converter for digital codes.

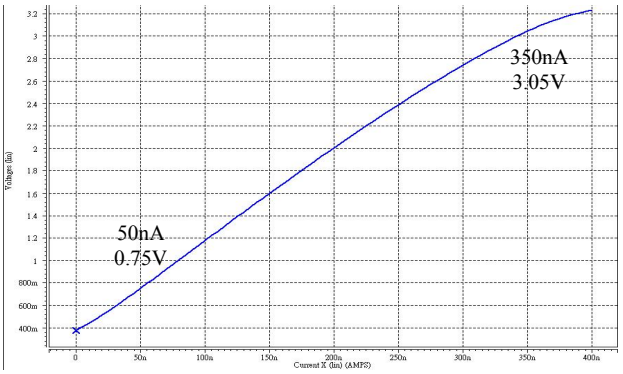


Fig. 9 The simulation of transimpedance amplifier.

4.3 Flash A/D Converter

A/D converters (ADCs) are important components which provide data conversion between analog and digital signals in a mixed-circuit system. A traditional flash ADC structure shown in Fig. 10 is the architecture of A/D converters that has high-speed data sample rate, but low resolution and large chip

area along with much power dissipation [12,13]. It consists of two major parts, resistor-based network and encoder. The resistor-based network provides different referred voltages for making the comparison of the input to their referred voltages in a number of operational amplifiers (comparators). The pattern called a thermometer code outputted from the comparators corresponds to an analog input. The encoder is followed to generate the digital binary code according to its input thermometer code.

It is noted that a bubble error may be occurred on a thermometer code because of unpredictable process variation, which cause the thermometer code possible unknown. If an unknown code outputted from comparators is directly passed through the encoder, the possible meta-stability errors [14] should be created. Thus, the bubble error corrector is required before the encoding to correct the thermometer code.

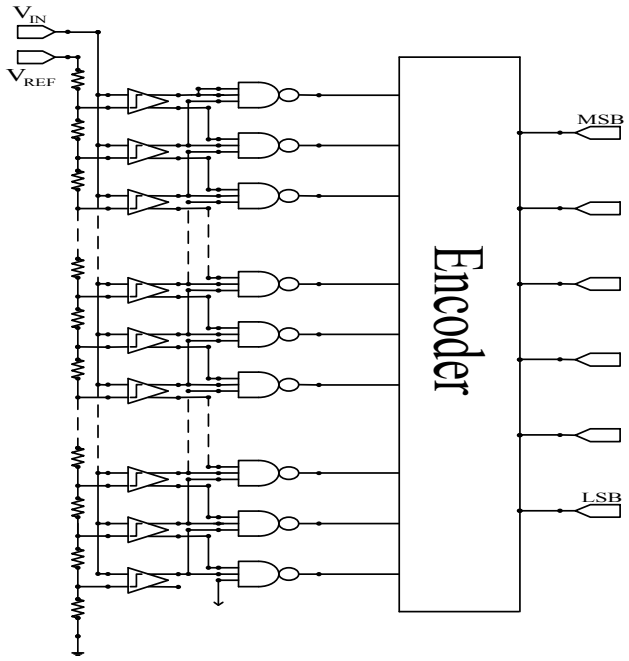


Fig. 10 A traditional flash ADC architecture.

4.3.1 Proposed Flash A/D Converter

A low-resolution flash ADC is often considered as the post process to convert an analog output to be a digital code in a SoC application, such as a CMOS image sensor. But, the comparators shown in the flash ADC architecture still cost too large area and lead much power consumption [15,16]. Figure 11 shows our proposed 6-bit CMOS flash ADC modified from the bisection approach [17].

In Fig. 11, we divide 63 comparators into eight groups and separate them into four regions. Each region covers two groups and four regions 1, 2, 3, and 4 stand for comparators 1~16, 17~32, 33~48, and 49~63, respectively. Three comparators, com1, com2, and com3, are created to redistribute the input operating voltages for controlling four regions. The outputs generated from three comparators can select one of four regions to work by comparing the input voltage. It means that only a quarter of whole comparators in the flash ADC are operated in every clock cycle. With the above approach, those un-operated comparators are turned off such that the ADC can save much power consumption. For example, when the input voltage Vin is located on the region1, the output(-) of the comparator com1 is high and sets only all compactors1~16 on and their output patterns are sent to the bubble error correction and encoder for generating a binary code. Other three regions including comparators 17~63 are turned off to reduce power consumption.

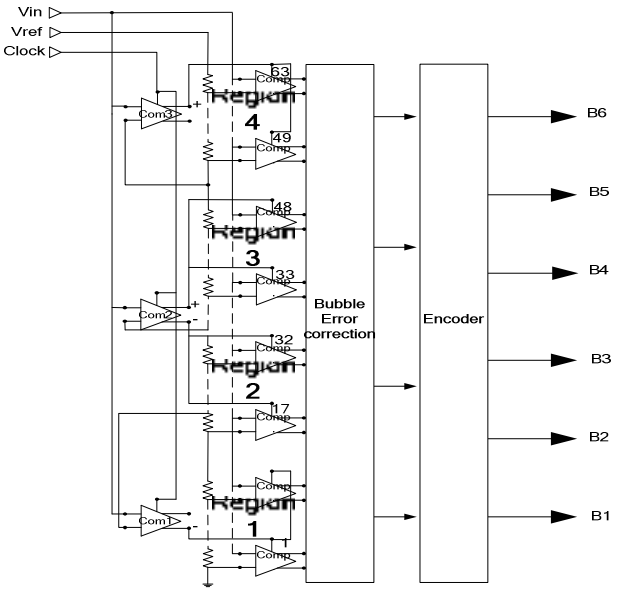


Fig. 11 The proposed 6-bit flash ADC.

4.3.2 Power-Gated Comparator

It is noted that all comparators shown in Fig. 11 are the power-gated comparators. Each comparator can be worked or not by controlling a power-switch device. The power-gated comparator referred from [12] is also designed for the requirement of low power consumption in our flash ADC.

Figure 12 shows the comparator that composes of a power-switch transistor (M11), a positive-feedback latch (M1~M4), resetting transistors (M5 and M8), input transistors (M6 and M9), and current cutting transistors (M7 and M10) with feedback inverters (Inv1and Inv2). When the clock is high, the comparator works in a resetting mode. The power switch transistor M11 is off and the latch transistors M1 to M4 are also off. Meanwhile, the resetting transistors M5 and M8 are on and their output signals V_{out+} and V_{out-} are pulled down to ground at the same time. This cause the inputs of two feedback inverters Inv1and Inv2 are set to be low. Thus, the input

voltage Vin cannot be made for the comparison with the reference voltage Vref.

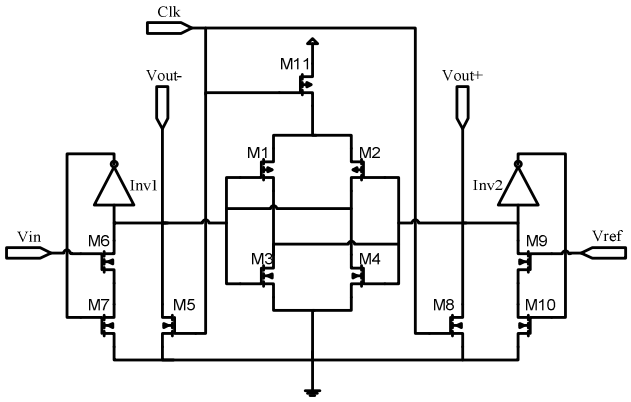


Fig. 12 Power-gated comparator.

When the clock is low, the comparator works in operational mode. M11 is on and M5 and M8 are off. The latch transistors M1 to M4 are followed on. This cause that one of output signals V_{out+} and V_{out-} is high and another is low at the same time. For example, when Vin > Vref, the equivalent on-resistance of the input transistor M6 is light larger than that of another input transistor M9. Thus, the V_{out+} is high and the V_{out-} is low.

4.3.3 Bubble Error Corrector

Figure 13 shows the architecture of a thermometer code generation. A thermometer code composed of series 0 and 1 is created from the comparators. Due to the comparison characteristics of the resistor-based network and comparators, a series of 0 or 1 must be kept successive, that is, no any 0 (1) can be interleaved into a series of 1 (0). However, an unusual single "0" or "1" called a bubble error sometimes exists in a thermometer code. That is, a 0 (1) is interleaved into a series of 1 (0). Figure 14 illustrates an example, the thermometer code of 001111 is normal, but the code of 001011 has a bubble error. The error would cause that the ADC output generates a missed code.

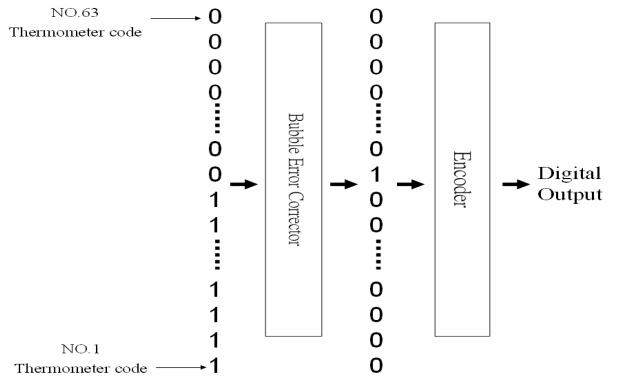


Fig. 13 The generation of a thermometer code.

Figure 14 shows the simply combinational logic of "011" pattern called a bubble error corrector which is inserted between the comparators and the encoder to detect and correct the bubble error effect. From the figure, the output of "011" pattern is 001000 if the input is a normal code of 001111 or either a bubble error code of 0010111.

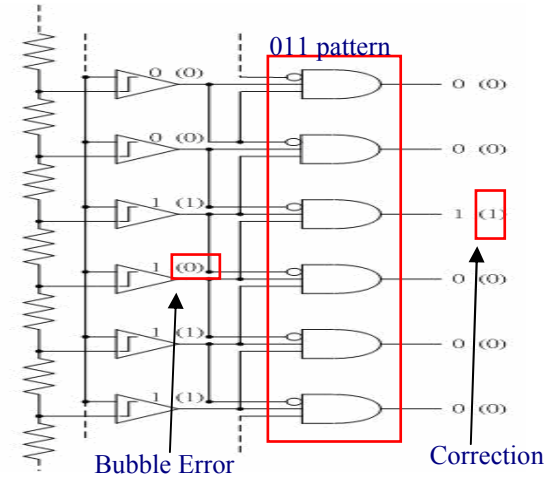


Fig. 14 The bubble error corrector

4.3.4 Encoder

The bubble error corrector outputs a correct code that has only a "1". An encoder is used to encode the correct code to be a corresponded binary code. Figure 15 shows our encoder that consists of NMOS switches, PMOS switches, and inverters. A PMOS device and an inverter located on the top of each column are used as pull up and inverted output, respectively. The NMOS devices in each row are used for encoding a unique logic "1" outputted from the bubble code corrector. For a 6-bit ADC, there are up to 6 output columns and 63 output rows.

When NMOS devices in a row are on, the output correct code from the bubble error corrector is encoded to be a binary code that is outputted from the inverters in all columns. For example, the first row comes from the 63rd output of the bubble error corrector that is a unique logic 1 of 63 outputs, thus the binary output code is 111111. Similarly, the last low is presented the binary code of 000001.

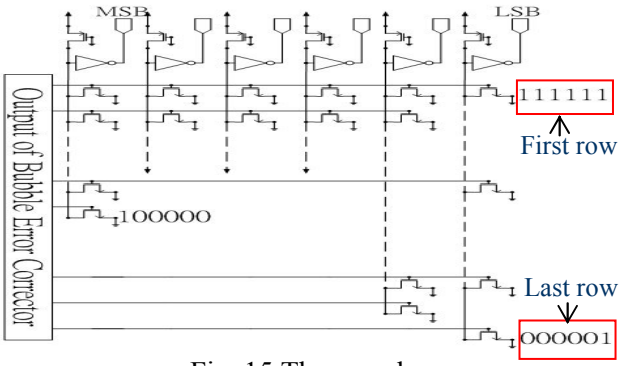


Fig. 15 The encoder.

5 Chip Implementation

The proposed sensor chip has been implemented in a 0.35μm 2P4M CMOS process. The Hspice simulation includes two major parts of front-end and back-end circuits. We have simulation results from the front-end circuits introduced in subsections 3.1-3.3 to the post processing and transimpedance amplifier (TIA) presented in subsections 4.1-4.2 of back-end circuits. The output electronic analog voltage from the TIA is the range of 0.75V to 3.05V, as shown in Fig. 9. The voltage can be used as the analog input of the proposed flash A/D converter and the converter can output digital codes. Thus, we first make the simulation of our flash A/D converter and then do the simulation of whole integrated system of our image sensor as the following two subsections.

5.1 Results of Flash A/D Converter

Table 1 summaries the comparison in simulation results of power consumption, DNL, and INL at the same condition of TSMC 0.35μm CMOS process, 6-bit resolution, clock rate of 200MHz, and input range of 0-2V for the traditional flash ADC of Fig. 10, bisection approach [17], and our ADC. We carefully resize all the comparators to reduce power dissipation as possible such that our proposed ADC can save up to 32.6mW (40.75mW-8.15mW) and 52.61mW (60.76mW-8.15mW) in power consumption than that of bisection and traditional approaches, respectively. Although the distributed control approach may take extra little latency, the sampling rate of 200MHz can satisfy the operation of our column selector.

Table 1 The comparison of our proposed flash ADC with the traditional and bisection ADCs.

	Traditional of Fig. 10	Bisection[17]	Ours
Technology	0.35um TSMC	0.35um TSMC	0.35um TSMC
Power supply	3.3V	3.3V	3.3V
Resolution	6 bits	6 bits	6 bits
Input analog range	0-2V	0-2V	0.75V-3.05V
Power consumption	60.76mW @200MHz	40.75mW @200MHz	8.15mW @200MHz
DNL	0.2LSB/ -0.3LSB	0.5LSB/ -0.3LSB	0.5LSB/ -0.5LSB
INL	0.2LSB/ -0.3LSB	0.4LSB/ -0.6LSB	0.8LSB/ -0.6LSB
Core size	-	0.7×0.8 mm^2	0.71×0.63 mm^2

The simulation result of our power-gated comparator is shown in Fig. 16. Since the threshold voltage Vth of a typical MOS device is 0.8V, it will limit the input range of the comparator even if the analog input of our ADC is added. If the reference voltage Vref is less than 0.8V, the comparator would not work. Thus, we set Vref to be 0.8V. The input voltage Vin of the comparator is set from 0.75V to 3.05V (i.e., a dc offset is provided to the Vin 0~2V). From the figure, when Vin > Vref, the positive-terminal output signal Vout+ is high and its output follows the clock, but the negative-terminal output signal Vout- keeps low at this time period. When Vin < Vref, the output signal Vout- is high and also follows the clock, but the Vout+ is forced to be low at the time.

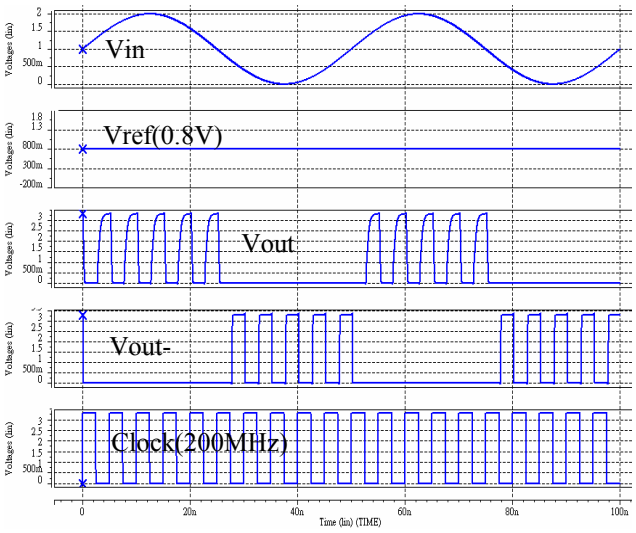
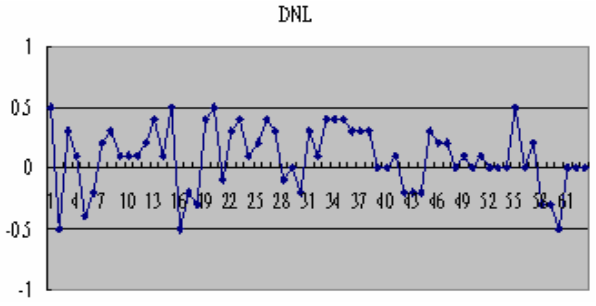
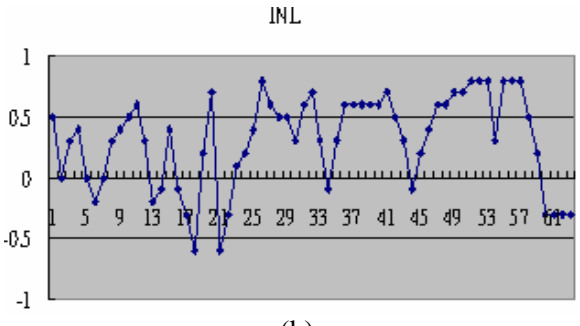


Fig. 15 The results of our power-gated comparator.

Figures 16(a) and 16(b) show the results of DNL (Differential Non-Linearity) and INL (Integral Non-Linearity), respectively, of the proposed ADC. The DNL and INL are 0.5LSB/-0.5LSB and 0.8LSB/-0.6LSB, respectively. Their linearity are controlled within ±1LSB.



(a)



(b)

Fig. 16 (a) The DNL and (b) the INL of our proposed ADC.

The ENOB (Effective Number Of Bits) and SNR (Signal Noise Ratio) for an ADC are the other important characteristic. The relation between ENOB and SNR is presented as below.

$$ENOB = \frac{SNR - 1.763}{6.02} \quad (2)$$

Figure 17 presents the SNR simulation of the proposed ADC using the FFT analysis. The result shows that the SNR is 37.1dB in the working frequency of 400KHz, and then the ENOB is 5.87 bits.

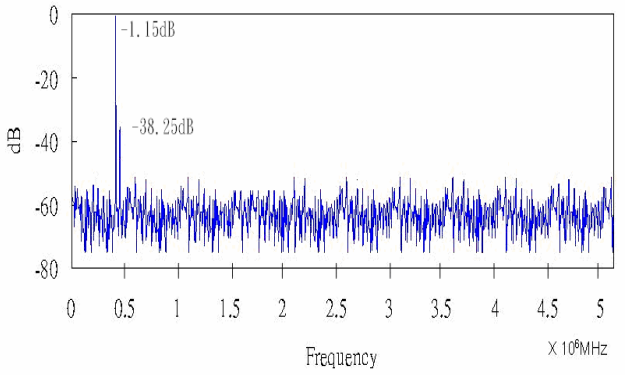


Fig. 17 The SNR of our proposed ADC.

Figure 18 shows the physical layout of our flash ADC which occupied the size of 0.71×0.63 mm^2.

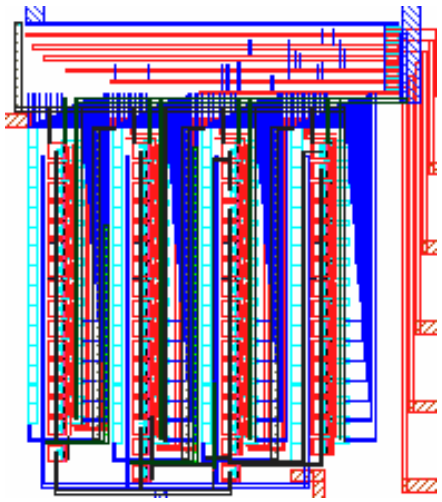


Fig. 18 The physical layout of our proposed ADC.

5.2 Results of Integrated Image Sensor

The simulation results of whole chip are shown in Figure 19. The results show the complete digital codes from LSB to MSB transferred the weak to strong photocurrents in gray level resolution, e.g., the output codes 000000 and 111111 are represented for the 64 column pixels' value of the 1st- and 64th rows, respectively. The total integration time is around 5.7ms. The maximum frame rate is up to 175 frames per second.

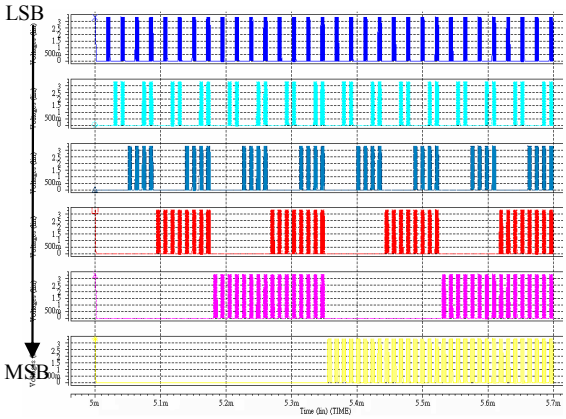


Fig. 19 The simulation result of whole chip.

Table 2 summarizes the specification of our proposed sensor chip. The power consumption is 35.15mW at the clock rates of 2MHz for row selector and 200MHz for ADC. Table 3 shows our design in comparison with other image sensors and we have lower power consumption as well as higher frame rate.

Table 2 Specification of our proposed sensor chip.

Technology	TSMC 0.35μm CMOS, 2P4M,
Supply voltage	Vdd=3.3V, Vss=0.0V
Output signal	Digital output (Gray level)
Chip size	4.35mm×4.35mm (include I/O pads)
Core size	3.55mm×3.55mm
Array size	66×66 (Effective array size 64×64)
Pixel size	15.8μm×10.6μm
Fill factor	37.2%
Clock rate	2MHz at row selector (ADC at 200MHz)
Frame rate	175 frames/sec
Power consumption	35.15mW

Table 3 Comparison with other approaches in terms of chip size, speed, and power.

	Fish [10]	Hsiao [8]	Ours
Technology	HP 0.5μm	0.35um 1P4M	0.35μm 2P4M
Output signal	Binary	Binary	Gray Level
Chip size (Pixel array)	3.5×4.3mm^2 (64 × 64)	3.2×3.2mm^2 (66 × 66)	4.35×4.35mm^2 (66 × 66)
Power consumption	28mW(Min.) 36mW(Typical)	71.14mW Row clock at 10MHz	35.15mW Row clock at 2MHz/ADC at 200MHz
Frame rate	30 Frames/sec	32 Frames/sec	175 Frames/sec

Figure 20 shows the physical layout of proposed chip that chip area including the I/O pads is $4.35 \times 4.35mm^2$ and contains the number of 29785 transistors.

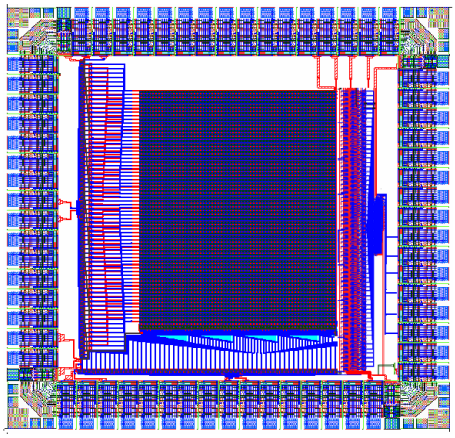


Fig. 20 The physical layout of our proposed chip.

6 Conclusion

The CMOS image sensor based on smooth spatial filter has been developed and implemented in standard CMOS process. Due to new major designs for lower-exposure pixel and low-power ADC, the power consumption of the sensor is 35.15mW at a frame rate 175 frames/sec. In the future, we can extend the SSF algorithm and embed the chip by combining with other applications, such as intelligent vehicle detection and tracking, fingerprint recognition, and surveillance monitoring system, to be a high-performance SOC.

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References:

[1] Chye Huat Aw and Bruce A. Wooley, "A 128*128-Pixel Standard CMOS Image Sensor with Electronic Shutter," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 12, 1996, pp. 1922-1930.

[2] Sunetra K. Medis, Sabrina E. Kemeny, and Russell C. Gee, "CMOS Active Pixel Image Sensors for Highly Integrated Imaging Systems," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 2, Feb. 1997, pp. 187-197.

[3] O. Yadid-Pecht and A. Belenky, "In-pixel autoexposure CMOS APS," *IEEE Journal of Solid-State Circuits*, Vol. 38, Aug. 2003, pp. 1425-1428.

[4] I. Takayanagi, J. Nakamura, E. R. Fossum, K. Nagashima, T. Kunihoro, and H. Yurimoto, "Dark current reduction in stacked-type CMOS-APS for charged particle imaging," *IEEE Electron Devices*, Vol. 50, Jan. 2003, pp. 70-76.

[5] I. Inoue et al, "Low-Leakage-Current and Low-Operating-Voltage Buried Photodiode for a CMOS Imager," *IEEE Electron Devices,* Vol. 50, Jan. 2003, pp. 43-47.

[6] J. Doge, G. Schonfelder, G. T. Streil, and A. Konig, "An HDR CMOS image sensor with spiking pixels, pixel-level ADC, and linear characteristics," *IEEE Circuit and System. II*, Vol. 49, Feb. 2002, pp. 155-158.

[7] L. McIlrath, "A low-power low-noise ltra-wide-dynamic-range CMOS imager with pixel-parallel A/D conversion," *IEEE Journal of Solid-State Circuits*, Vol. 36, May 2001, pp. 846-853.

[8] Pei-Yung Hsiao,Yu-Chun Hsu, Wen-Ta Lee, Chia-Chun Tsai, and Chia-Hao Lee, "An Embedded Analog Spatial Filter Design of The Current-Mode CMOS Image Sensor," *IEEE Consumer Electronics*, Vol. 50, Aug. 2004, pp. 945-951.

[9] Shyh-Yih Ma and Liang-Gee Chen, "A Single Chip CMOS APS Camera with Direct Frame Difference Output," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 10, 1999, pp. 1415 -1418.

[10] Alexander Fish, Dmitry Turchin, and Orly Yadid Pecht, "An APS With 2-D Winner-Take-All Selection Employing Adaptive Spatial Filtering and False Alarm Reduction," *IEEE Electron Device*, Vol. 50, No. 1, Jan. 2003.

[11] I-Hsin Wang, Chung-Shun Liu, and Shen-Iuan Liu, "A low power 5Gb/s transimpedance amplifier with dual feedback technique", *AP-ASIC 2004*, Session 14-6, Aug. 2004, pp. 304-307.

[12] J. Terada, Y. Matsuya, F. Morisawa and Y. Kado, "8-mW, 1-V, 100-Msps, 6-bit A/D converter using a trans-conductance latched comparator," Proceedings of the Second IEEE Asia Pacific Conference on ASIC, Aug. 2000, pp. 53-56.

[13] B. Yu. and Black W. C. Jr., "A 900 MS/s 6b interleaved CMOS flash ADC," *IEEE Custom Integrated Circuits Conference*, May 2001, pp. 149-152.

[14] C. L. Portmann and T. H. Y. Meng, "Power-efficient meta-stability error reduction in CMOS flash A/D converters," *IEEE Journal of Solid-State Circuits*, Vol. 31, Aug 1996, pp. 1132-1140.

[15] P. C. S. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s flash ADC in 0.18 μm CMOS using averaging termination," *IEEE Journal of Solid-State Circuits*, Vol. 37, Dec. 2002, pp. 1599-1609.

[16] K. Uyttenhove and M. S. J. Steyaert, "A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25μm CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 38, July 2003, pp. 1115-1122.

[17] Chia-Chun Tsai, Kai-Wei Hong, Yuh-Shyan Hwang, Wen-Ta Lee and Trong-Yen Lee, "New power saving design method for CMOS flash ADC," *International Midwest Symposium on Circuits and Systems*, July 2004, pp. 371-374.

[18] M. Sakakibara, S. Kawahito, D. Handoko, N. Nakamura, H. Satoh, M. Higashi, K. Mabuchi, and H. Sumi, "A high-sensitivity CMOS image sensor with gain-adaptive column amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 5, May 2005, pp. 1147-1156.

[19] N. Kawai, and S. Kawahito, "Measurement of low-noise column readout circuits for CMOS image sensors," *IEEE Trans. on Electron Devices*,
Vol. 53, No. 7, July 2006, pp. 1737-1739.

[20] Cheon Jimin and G. Han, "Noise analysis and simulation method for a single-slope ADC with CDS in a CMOS image sensor," *IEEE Trans. on Circuits and Systems I*, Vol. 55, No. 10, Nov. 2008, pp. 2980-2987.

[21] C. Shoushun, and A. Bermak, "Arbitrated time-to-first spike CMOS image sensor with on-chip histogram equalization" *IEEE Trans. on Very Large Scale Integration Systems*, Vol. 15, No. 3, March 2007, pp. 346-357.

[22] J. P. Crooks, S. E. Bohndiek, C. D. Arvanitis, R.Speller, H. XingLiang, E. G. Villani, M. Towrie, and R. Turchetta, "A CMOS image sensor with in-pixel ADC, timestamp, and sparse readout," *IEEE Sensors Journal*, Vol. 9, No. 1, Jan. 2009, pp. 20-28.

[23] A. Belenky, A. Fish, A. Spivak, and O. Yadid-Pecht, "A snapshot CMOS image sensor with extended dynamic range," *IEEE Sensors Journal*, Vol. 9, No. 2, Feb. 2009, pp. 103-111.