

# An inversion/non-inversion dynamic optically reconfigurable gate array VLSI

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*Abstract:* Up to now, an optically differential reconfigurable gate array taking a differential reconfiguration strategy and a dynamic optically reconfigurable gate array taking a photodiode memory architecture have been proposed. The differential reconfiguration strategy provides a higher reconfiguration frequency, with no increase in laser power, than other optically reconfigurable gate arrays, however the differential reconfiguration strategy can not achieve a high-gate-count VLSI because of the area occupied by the static configuration memory. On the other hand, the photodiode memory architecture can achieve a high-gate-count VLSI, but its configuration is slower than that of the optically differential reconfigurable gate array using equivalent laser power. So, this paper presents a novel inversion/non-inversion dynamic optically reconfigurable gate array VLSI that combines both architectures. It thereby achieves both advantages of rapid configuration and a high gate count. The experiments undertaken in this study clarify the effectiveness of the inversion/non-inversion optical configuration method.

*Key-Words:* Field programmable gate arrays, Optical reconfigurations, Holographic memories, Optically reconfigurable gate arrays.

## 1 Introduction

Demand for high-speed reconfigurable devices has continued to increase. If a gate array can be reconfigured rapidly, an idle circuit can be removed from the gate array and other necessary circuitry can be programmed onto the gate array at that time, thereby increasing the gate array activity. However, major programmable devices, filed programmable gate arrays (FPGAs) are unsuitable for such a dynamic reconfiguration because FPGAs require more than several milliseconds for reconfiguration [1]–[3].

High-speed reconfigurable devices have been developed: DAP/DNA chips, DRP chips, and multi-context FPGAs [4]–[9]. They package reconfiguration memories and a microprocessor array or gate array onto a chip. The internal reconfiguration memory stores reconfiguration contexts of 4–16 banks, which can be changed from one to another during a clock cycle. Consequently, the arithmetic logic unit

or gate array of such devices can be reconfigured in a few nanoseconds on every clock cycle. However, increasing the internal reconfiguration memory while maintaining the gate density is extremely difficult.

Therefore, to realize both rapid reconfiguration and numerous reconfiguration contexts, an optically programmable gate array (OPGA) has been developed: it combines benefits of a holographic memory and an optically programmable VLSI [10]–[12]. The OPGA architecture achieved an implementation of 100 reconfiguration contexts and a 16–20  $\mu$ s reconfiguration period. In this architecture, rapid reconfiguration was difficult because serial transfers were used to connect photodiode arrays with gate arrays. Moreover, this architecture prevents the use of the gate array during reconfiguration. Therefore, because of the necessity of repeating the reconfiguration cycle, the activity of the OPGA's gate array is decreased considerably. In addition to that weakness, the real gate count of the OPGA-VLSI was too

low. The gate array of the OPGA-VLSI was 80 gates because of its complicated architecture.

Therefore, an optically differential reconfigurable gate array using a differential reconfiguration strategy to achieve a fast reconfiguration capability [13]–[15] has been proposed along with a dynamic optically reconfigurable gate array using a photodiode memory architecture to realize huge-gate-count VLSI [16]–[18]. This differential reconfiguration strategy can offer a higher reconfiguration frequency using no more laser power than that used by other optically reconfigurable gate arrays and the OPGA. However, even though it can achieve a higher gate density than that of OPGA, the differential reconfiguration strategy can not provide a high-gate-count VLSI because of the area occupied by the static configuration memory. On the other hand, the dynamic optically reconfigurable gate array can achieve an extremely high-gate-count VLSI; although it is faster than an OPGA, its configuration is slower than that of an optically differential reconfigurable gate array using equal laser power.

Therefore, to realize both advantages of rapid configuration and high-gate-count, this paper presents a novel inversion/non-inversion dynamic optically reconfigurable gate array VLSI that combines both architectures. This paper describes some experiments that clarify the effectiveness of the inversion/noninversion optical configuration method.

## 2 Conventional optical configuration architectures

### 2.1 OPGA

An OPGA was the world's first ORGA [10]–[12]. An OPGA consists of a holographic memory, a laser array, and an optically reconfigurable gate array VLSI. The OPGA architecture has achieved an implementation of 100 reconfiguration contexts and a 16–20  $\mu$ s reconfiguration period. Such OPGA architectures presented the possibility of providing a virtual gate count that is much higher than those of currently available VLSIs.

#### 2.1.1 Gate density issue

However, although a large virtual gate count can be realized using the large storage capacity of a holographic memory, the actual gate count of OPGA-VLSI was 80 gates, which is very small because of its complicated architecture: the OPGA-VLSI comprises photodiode arrays with latches to store a context temporarily, gate arrays with SRAMs to store a context, and serial transfers between the photodiode arrays and gate arrays. An optical configuration context is first detected on a photodiode array and stored on latches in the photodiode array. Then, the stored configuration context is transferred from latches in the photodiode array to the SRAM in a gate array. Finally, the gate array operates based on the context stored in the SRAM. Because of its complicated architecture, reconfiguration circuits without a photodiode array typically occupy more than one-third of the VLSI chip area.

#### 2.1.2 Configuration speed and overhead issues

This architecture presents configuration speed and overhead issues. This architecture used serial transfers to connect photodiode arrays to gate arrays. For that reason, the reconfiguration period was limited to 16–20  $\mu$ s. Moreover, this architecture prevented the use of the gate array during reconfiguration because the serially transferred configuration context is invalid until it is completed. Consequently, the OPGA-VLSI required a 16–20  $\mu$ s halt of the gate array for each reconfiguration procedure. Repeating the reconfiguration cycle extremely decreases the activity of the OPGA's gate array.

### 2.2 ODRGA

#### 2.2.1 Fast configuration advantage

Optically Differential Reconfigurable Gate Arrays (ODRGA) have been developed to accelerate the reconfiguration frequency [13]–[15]. Figure 1 shows that each reconfiguration circuit consists of a photodiode, a refresh transistor, toggle flip flops, and XOR circuits. In the

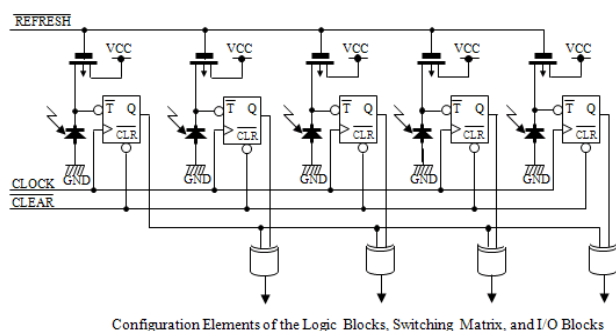


Figure 1: Conventional optical differential reconfiguration circuit with four configuration bits.

ODRGA-VLSI, photodiodes are placed near and directly connected to programming elements of a programmable gate array through static configuration memory, thereby perfectly removing serial transfers. Consequently, the ODRGA-VLSI can be reconfigured perfectly in parallel with no overhead. The reconfiguration frequency is much higher than that of the OPGA. Moreover, the differential reconfiguration architecture of ODRGA-VLSIs offers an advantage of further increasing the reconfiguration speed compared to other ORGAs using equivalent laser power [15]. The diffraction light intensity from a holographic memory is inversely proportional to the number of bright bits included in a configuration context. The bright bits mean the state '1' of bits of the configuration context. The reconfiguration speed can be increased with no increase of laser power if the number of bright bits can be decreased. Heretofore, the reconfiguration speed of an ODRGA-VLSI has been measured in nanoseconds by exploiting the architecture [15].

### 2.2.2 Gate density issue

By removing serial transfer circuits and double configuration memories, the area of reconfiguration circuits without photodiodes was reduced to 24.9% of the area of the entire VLSI chip, which is less than that of the OPGA. However, the static configuration memory prevented realization of high-gate-count ORGA-VLSIs.

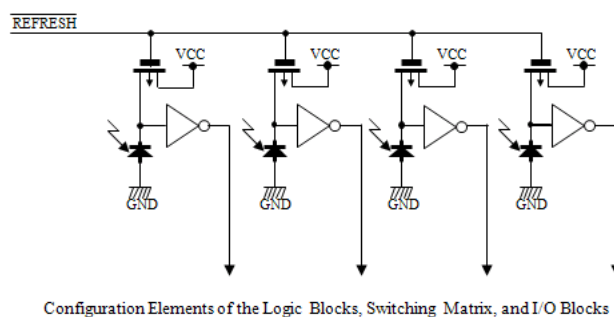


Figure 2: Conventional optical dynamic reconfiguration circuit with four configuration bits in a DORGA-VLSI.

## 2.3 DORGA

### 2.3.1 Gate density advantage

To realize a high-gate-count ORGA-VLSI, a Dynamic Optically Reconfigurable Gate Array (DORGA) architecture was proposed [16]–[18]. The architecture perfectly removes static configuration memory to store a context and uses the junction capacitances of photodiodes as dynamic configuration memory, as depicted in Fig. 2. A 0.35  $\mu\text{m}$  CMOS process 11,424-gate-count DORGA-VLSI has been fabricated [18]. In addition, larger-gate-count VLSIs will be increasingly available through the use of more advanced process technologies.

### 2.3.2 Reconfiguration frequency

However, this architecture can not reduce the number of bright bits in a configuration context. Therefore, using equivalent laser power, the reconfiguration frequency of a DORGA-VLSI is lower than that of an ODRGA-VLSI. This is an important weakness of DORGA-VLSIs.

## 3 Novel inversion/ noninversion configuration method

This paper presents a proposal of a novel inversion/noninversion optical configuration method to realize the two advantages of fast

configurations and high gate count. The inversion/noninversion optical configuration method can perfectly remove static configuration memory and can reduce the number of bright bits in a configuration context.

### 3.1 Generation of an optical configuration vector

In this strategy, configuration data for logic blocks, switching matrices, and I/O blocks are divided into small segments. For the small segments, the inversion/noninversion optical configuration method is applied. The following discussion uses bit-length  $N$ , which indicates the number of bits included in a small segment. A configuration vector used for programming a gate array and an optical configuration vector, the information of which are programmed onto a holographic memory, are signified respectively as an  $N$ -dimensional vector and  $N+1$ -dimensional vector, as the following.

$$= (1, 2, \dots, N), \quad (1)$$

$$= (1, 2, \dots, N, N+1), \quad (2)$$

Therein, each element of the vectors takes a binary value  $\{0,1\}$ . The optical configuration vector is defined in the following equation.

$$(1, \dots, N) = \oplus N+1, \quad (3)$$

In that equation, is a certain configuration context and  $N+1$  is an inversion bit included in an optical configuration vector, and  $\oplus$  signifies an exclusive OR operator. The role of the inversion bit  $N+1$  is to determine whether an optical configuration is executed based on a certain configuration context or its inversion context. The inversion bit is defined in the following equation.

$$N+1 = \begin{cases} 1 & : \sum_{i=1}^N i \geq \lfloor \frac{N}{2} + 1 \rfloor, \\ 0 & : \text{otherwise.} \end{cases} \quad (4)$$

In that equation,  $\lfloor \frac{N}{2} + 1 \rfloor$  denotes that  $\frac{N}{2} + 1$  is rounded down to the nearest whole number. Consequently, a calculated optical configuration vector including an inversion bit is programmed onto a holographic memory as a segment of a configuration context.

#### 3.1.1 Operation in a VLSI

In advance, an optical configuration vector, which is calculated using Eqs. (3) and (4), is programmed onto a holographic memory. In the case of reconfiguration, the optical configuration vector, including an inversion bit  $N+1$  is read out from the holographic memory and is programmed onto an ORGA-VLSI. A configuration vector in a segment of a gate array on the ORGA-VLSI is generated by calculating exclusive OR operations between a received optical configuration vector  $(1, \dots, N)$  and an inversion bit  $N+1$  as follows.

$$= (1, \dots, N) \oplus N+1. \quad (5)$$

#### 3.1.2 Estimation

As explained previously, in a holographic configuration, reducing the number of bright bits included in a configuration context can increase the reconfiguration frequency. Therefore, in this section, the reduction efficiency of the number of bright bits of the inversion/noninversion configuration method is discussed. Here, it is assumed that configuration contexts are given continuously for an ORGA-VLSI and that they uniformly include all possible patterns. For example, regarding 4-bit configuration, all possible patterns include the 16 patterns of "0000", "0001", ..., and "1111".

Under such a condition, the reduction efficiency of the number of bright bits in a configuration context of conventional ORGAs is estimated first. The average number of 1s corresponding to laser irradiation is calculated by counting bit 1 of all possible vectors and dividing it by  $N2^N$  of the summation of bits of all possible vectors, as in the following equation.

$$ORGA = \frac{\sum_{r=1}^N r \cdot {}_N C_r}{2^N N} = \frac{1}{2}, \quad (6)$$

In that equation,  ${}_N C_r$  is a combination. Similarly, the reduction of the number of bright bits included in a configuration context of the inversion/noninversion configuration method can be estimated as presented in Table 1. The average number of writing '1' corresponding to laser irradiation is calculated by counting '1' bits of all possible vectors and dividing it by  $N2^N$  of

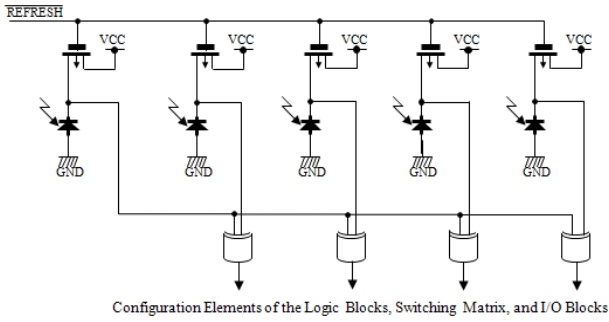


Figure 3: Circuit diagram of an inversion / noninversion dynamic optical configuration circuit including four configuration bits.

the summation of bits of all possible vectors, as shown in the following equation.

$$n_{new} = \frac{\sum_{r=1}^{\lfloor \frac{N}{2} \rfloor} r \cdot N C_r}{2^N N} + \frac{\sum_{r=\lfloor \frac{N}{2} \rfloor + 1}^N (N - r + 1) \cdot N C_r}{2^N N} \quad (7)$$

The first term in the right side of the upper Eq. (7) is identical to Eq. (6). In this case, an inversion bit  $N_{+1}$  is equal to 0. In addition, the second term in the right side of the upper Eq. (7) represents the case in which the inversion bit  $N_{+1}$  is equal to 1. Table 1 shows a calculation example of the number of bright bits in a configuration context including four configuration bits. In this case, the average number of bright bits can be decreased from the 2.0 of conventional ORGAs to 1.526. Using this inversion/noninversion dynamic optical configuration method, in the case of four bits, about 37% of bright bits are removable. Consequently, the reconfiguration frequency can be increased using this method.

## 4 VLSI Design

### 4.1 Inversion/noninversion dynamic optical configuration circuit

Figure 3 portrays a circuit diagram of an inversion/noninversion dynamic optical configuration circuit including four configuration bits. The configuration circuit consists of charge-integrated photo-circuits and exclusive-OR gates. Since the configuration circuit is

Table 1: Effectiveness of the inversion/non-inversion method.

4	3	2	1	5	4	3	2	1	Num. of Bright Bits
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	0	1	0	1
0	0	1	1	0	0	0	1	1	2
0	1	0	0	0	0	1	0	0	1
0	1	0	1	0	0	1	0	1	2
0	1	1	0	0	0	1	1	0	2
0	1	1	1	1	1	0	0	0	2
1	0	0	0	0	1	0	0	0	1
1	0	0	1	0	1	0	0	1	2
1	0	1	0	0	1	0	1	0	2
1	0	1	1	1	0	1	0	0	2
1	1	0	0	0	1	1	0	0	2
1	1	0	1	1	0	0	1	0	2
1	1	1	0	1	0	0	0	1	2
1	1	1	1	1	0	0	0	0	1

Average = 1.526

based on that of DORGA-VLSI, the photodiode is used not only for detecting a configuration context, but also as dynamic configuration memory. Therefore, a static configuration memory is perfectly removed and a high-gate-count VLSI can be realized. The only different point from the reconfiguration circuits of the DORGA-VLSI is that an inversion photodiode and exclusive-OR gates are added. This circuit can execute the procedure shown in Eq. (5) perfectly.

### 4.2 VLSI Design

Of course, since this method necessitates some increase of area compared to that of a conventional dynamic optically reconfigurable gate array, we have designed a dynamic optically

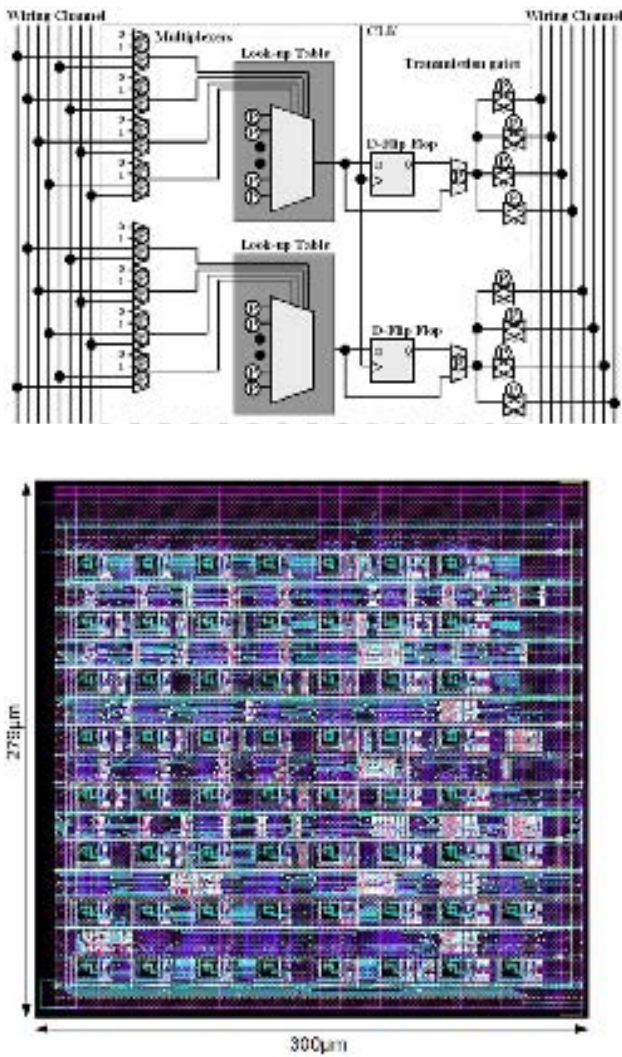


Figure 4: Block diagram and CAD layout of an optically reconfigurable logic block (ORLB) of a DORGA-VLSI.

reconfigurable gate array (DORGA) VLSI and an inversion/non-inversion dynamic optically reconfigurable gate array VLSI under the same condition. Block diagrams of an optically reconfigurable logic block and an optically reconfigurable switching matrix are portrayed in Figs. 4 and 5. The optically reconfigurable logic block consists of two 4-input 1-output look up tables, two delay flip flops, selectors, and transmission gates. In these figures, a P mark designates a photodiode. In addition, the optically reconfigurable switching matrix consists of optically programmable transmission gates. Identical blocks were applied for both VLSI designs. Both chips were designed using 0.35  $\mu\text{m}$  standard CMOS process technol-

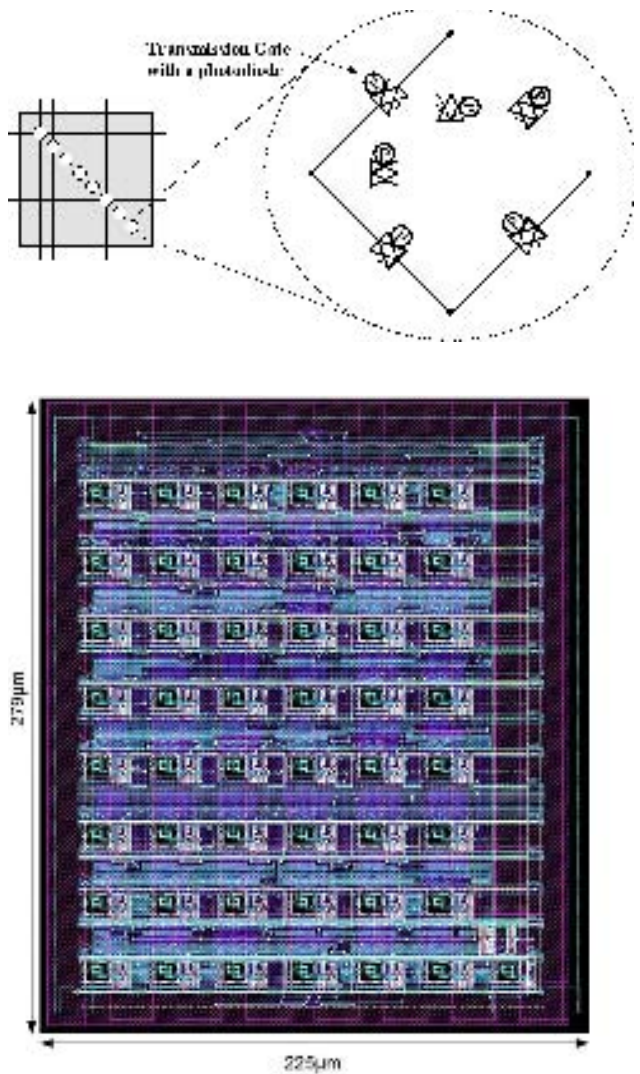


Figure 5: Block diagram and CAD layout of an optically reconfigurable switching matrix (ORSM) of a DORGA-VLSI.

ogy. Voltages of the core and I/O cells were designed identically, using 3.3 V. The acceptance surface size of the photodiode is  $9.5 \mu\text{m} \times 8.8 \mu\text{m}$ . The photodiodes were constructed between N+ diffusion and the P-substrate.

The CAD layouts of an optically reconfigurable logic block and an optically reconfigurable switching matrix of a conventional dynamic optically reconfigurable gate array (DORGA) VLSI are shown in Figs. 4 and 5. In addition, the CAD layout of an optically reconfigurable logic block of an inversion/non-inversion dynamic optically reconfigurable gate array VLSI is depicted in Fig. 6. The reason for applying the new inversion/noninversion configuration method only

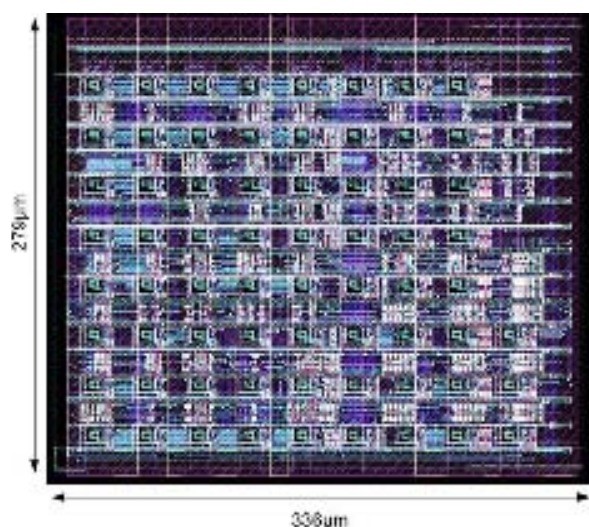


Figure 6: CAD layout of an optically reconfigurable logic block (ORLB) of an inversion/non-inversion dynamic optically reconfigurable gate array VLSI.

to optically reconfigurable logic blocks is that the effect of this inversion/noninversion configuration method can not be expected for switching matrices. A six-transmission cell of a switching matrix, as presented in Fig. 5, is always programmed with a single binary value 1 and the other binary value 0s. Therefore, although the inversion/noninversion configuration method can decrease the number of binary state 1s in the case with many binary state 1s, just like switching matrices, one binary value 1 can not be reduced. Therefore, the inversion/noninversion configuration method was applied only to look up tables of optically reconfigurable logic blocks. An optically reconfigurable logic block and an optically reconfigurable switching matrix of the DORGA-VLSI respectively include 59 photodiodes and 49 photodiodes. The number of photodiodes of an optically reconfigurable logic block of an inversion/non-inversion dynamic optically reconfigurable gate array VLSI was increased to 67.

### 4.3 Area estimation

The cell sizes of an optically reconfigurable logic block and an optically reconfigurable switching matrix of a conventional dynamic optically reconfigurable gate array (DORGA)

VLSI are, respectively,  $300 \text{ } \mu\text{m} \times 279 \text{ } \mu\text{m}$  and  $225 \text{ } \mu\text{m} \times 279 \text{ } \mu\text{m}$ . In addition, the cell sizes of an optically reconfigurable logic block and an optically reconfigurable switching matrix of a new inversion/non-inversion dynamic optically reconfigurable gate array VLSI are, respectively,  $336 \text{ } \mu\text{m} \times 279 \text{ } \mu\text{m}$  and  $225 \text{ } \mu\text{m} \times 279 \text{ } \mu\text{m}$ .

Here, in the case of an island-style gate array, the gate density is calculable using the following equation.

$$d = \frac{gN^2}{A_L N^2 + A_S((N+1)^2 - 4)}. \quad (8)$$

Therein,  $N$  denotes the number of logic blocks,  $g$  is the gate count per logic block,  $A_L$  is the area of a logic block cell, and  $A_S$  is the area of a switching matrix cell. Here, if the number  $N$  is sufficiently large, Eq. 8 can be approximated as the following.

$$d \simeq \frac{g}{A_L + A_S}. \quad (9)$$

Using the logic and switching matrix cell design specifications, the densities of a conventional dynamic optically reconfigurable gate array (DORGA) VLSI and a new inversion/non-inversion dynamic optically reconfigurable gate array VLSI are calculable, respectively, as  $232.1 \text{ gates} / \text{mm}^2$  and  $217.2 \text{ gates} / \text{mm}^2$ . As a result, the increased area of the new inversion/non-inversion dynamic optically reconfigurable gate array VLSI is small: less than 6.5%. That very small area of increase can be ignored, this method is very useful to accelerate the reconfiguration frequency while maintaining its gate density.

## 5 Experiments

### 5.1 Experimental System

The architecture was emulated using a current ORGA-VLSI chip to estimate the effectiveness of the inversion / noninversion dynamic optical configuration method. The experimental system is depicted in Fig. 7. The light source is a He-Ne laser. The respective power and wavelength of the laser are about 30 mW and 632.8

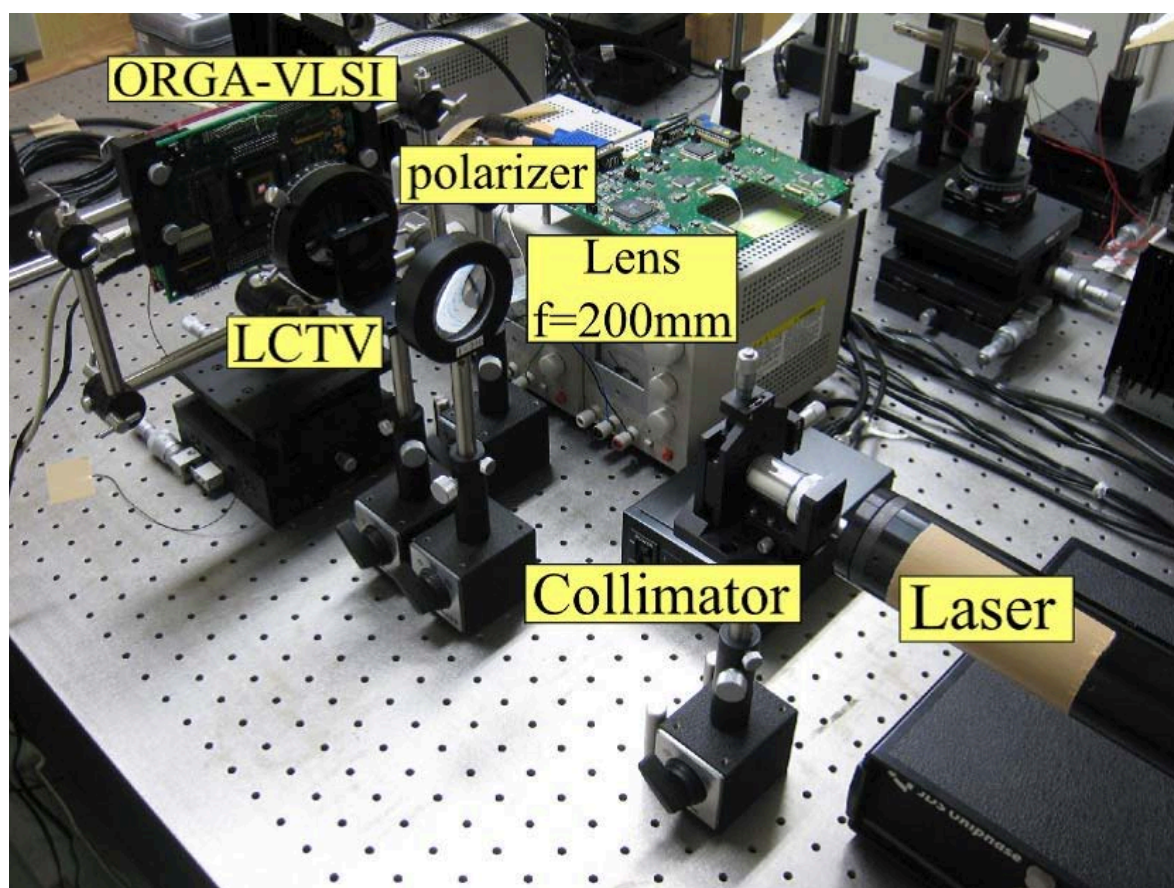


Figure 7: Experimental system.

nm. The laser beam is incident to a holographic memory on a liquid crystal spatial light modulator (LC-SLM). The LC-SLM is a projection TV panel (L3P07X-31G0; Seiko Epson Corp.), which is a  $90^\circ$  twisted nematic device with a thin-film transistor. The panel consists of  $1,024 \times 768$  pixels, each having a size of  $14 \times 14 \mu\text{m}^2$ . Holographic patterns were displayed on the LC-SLM.

## 5.2 Experimental Results

Using the previously explained optical system, reconfiguration periods were measured. The experimental result is shown in Fig. 8. The results show that the reconfiguration of the new method is about 1.2 times faster than that of a DORGA-VLSI. In addition, the gate density was improved to be nearly equal to that of DORGA. This new method was thereby confirmed to provide fast configuration and high-

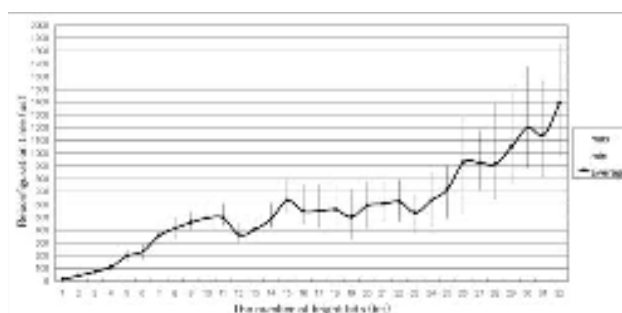


Figure 8: Relationship between the reconfiguration period and the number of bright bits in a configuration context.

gate-count capabilities.

## 6 Conclusion

The world's first optically reconfigurable gate array (ORGA) presented weaknesses in terms of reconfiguration frequency and gate density. Therefore, an optically differential reconfigurable gate array taking a differential reconfiguration strategy and a dynamic optically reconfigurable gate array taking a photodiode memory architecture were proposed. The differential reconfiguration strategy increased the reconfiguration frequency using equal laser power to that used by other ORGAs. Nevertheless, the differential reconfiguration strategy did not produce a high-gate-count VLSI because of the area occupied by static configuration memories. On the other hand, the dynamic optically reconfigurable gate array achieved a high-gate count VLSI. However, the configuration speed of the dynamic optically reconfigurable gate array was slower than that of optically differential reconfigurable gate arrays when using equal laser power. Therefore, to realize both advantages of rapid configuration and a high gate count, this paper has presented an inversion/non-inversion dynamic optically reconfigurable gate array VLSI that combines both the architectures. Area increases are very small: less than 6.5%. However, the reconfiguration frequency of the new method was confirmed experimentally as about 1.2 times faster than that of DORGA-VLSI. These results clarified the effectiveness of the inversion/noninversion optical configuration method.

## 7 Acknowledgments

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### References:

- [1] Altera Corporation, "Altera Devices," <http://www.altera.com>.
- [2] Xilinx Inc., "Xilinx Product Data Sheets," <http://www.xilinx.com>.
- [3] Lattice Semiconductor Corporation, "LatticeECP and EC Family Data Sheet," <http://www.latticesemi.co.jp/products>, 2005.
- [4] <http://www.ipflex.co.jp>
- [5] H. Nakano, T. Shindo, T. Kazami, M. Motomura, "Development of dynamically reconfigurable processor LSI," NEC Tech. J. (Japan), vol. 56, no. 4, pp. 99–102, 2003.
- [6] A. Dehon, "Dynamically Programmable Gate Arrays: A Step Toward Increased Computational Density," Fourth Canadian Workshop on Field Programmable Devices, pp. 47–54, 1996.
- [7] S.M.Scalera and J.R.Vazquez, "The design and implementation of a context switching FPGA," IEEE symposium on FPGAs for Custom Computing Machines, pp. 78–85, 1998.
- [8] S.Trimberger, et al. "A Time-Multiplexed FPGA," FCCM, pp. 22–28, 1997.
- [9] D. Jones, D.M.Lewis, "A time-multiplexed FPGA architecture for logic emulation," Custom Integrated Circuits Conference, pp. 495 – 498, 1995.
- [10] J. Mumbru, G. Panotopoulos, D. Psaltis, X. An, F. Mok, S. Ay, S. Barna, E. Fossum, "Optically Programmable Gate Array," SPIE of Optics in Computing 2000, Vol. 4089, pp. 763–771, 2000.
- [11] J. Mumbru, G. Zhou, X. An, W. Liu, G. Panotopoulos, F. Mok, and D. Psaltis, "Optical memory for computing and information processing," SPIE on Algorithms, Devices, and Systems for Optical Information Processing III, Vol. 3804, pp. 14–24, 1999.

- [12] J. Mumburu, G. Zhou, S. Ay, X. An, G. Panotopoulos, F. Mok, and D. Psaltis, "Optically Reconfigurable Processors," SPIE Critical Review 1999 Euro-American Workshop on Optoelectronic Information Processing, Vol. 74, pp. 265-288, 1999.
- [13] M. Watanabe, F. Kobayashi, "An optically differential reconfigurable gate array and its power consumption estimation," IEEE International Conference on Field Programmable Technology, pp. 197-202, 2002.
- [14] M. Miyano, M. Watanabe, F. Kobayashi, "Optically Differential Reconfigurable Gate Array," Electronics and Computers in Japan, Part II, Issue 11, vol. 90, pp. 132-139, 2007.
- [15] M. Nakajima, M. Watanabe, "A 62.5 ns holographic reconfiguration for an optically differential reconfigurable gate array," IEEE International Conference on Field Programmable Technology, pp. 297-300, 2007 .
- [16] M. Watanabe, F. Kobayashi, "Dynamic Optically Reconfigurable Gate Array," Japanese Journal of Applied Physics, Vol. 45, No. 4B, pp. 3510-3515, 2006.
- [17] D. Seto, M. Watanabe, "A dynamic optically reconfigurable gate array - perfect emulation," IEEE Journal of Quantum Electronics, Vol. 44, Issue 5, pp. 493-500, 2008.
- [18] M. Watanabe, "A 11,424 gate-count zero-overhead dynamic optically reconfigurable gate array VLSI" IEEE International SOC Conference, pp. 75-78, 2007.
- [19] M. Watanabe, F. Kobayashi, "Manufacturing-defect tolerance analysis of optically reconfigurable gate arrays," World Scientific and Engineering Academy and Society Transactions on Signal Processing, Issue 11, Vol. 2, pp. 1457- 1464, 2006.
- [20] M. Watanabe, F. Kobayashi, "High manufacturing defect- tolerance optically programmable architecture," The 5th World Scientific and Engineering Academy and Society International Conference on circuits, systems, electronics, control & signal processing, pp.197-203, 2006.