Digitally Controllable Delay Element Using Switched-Current Mirror

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Abstract: -Controllable delay elements are essential for shifting the edges of signals in many digital and mixed-mode signal processing integrated circuits. Digitally programmable delay elements (DPDEs) are more flexible, less susceptible to noise and exhibit more robustness than their analog counterparts. In this paper, a partially programmable and a fully programmable delay elements are proposed. Together with a switched current mirror, a gate decoupling technique is applied to the former while a Schmitt type inverter is used in the later structure to achieve more significantly reduced static and short-circuit current. The delay elements are implemented in a 0.18um technology and simulation results with a 1V power supply show a more than 40% power saving while operating at a speed of 450MHz in both structures.

Key-Words: - current mirror, delay element, inverter, low power, Schmitt trigger, switched current

1 Introduction

Programmable delay elements (PDEs) are prevalent in many VLSI systems such as delay locked loops, (DLLs), phase locked loops (PLLs), controlled oscillators (CO) and analog-to-digital converters [1-4]. One of the differences between the PDEs and other programmable circuits [5] is that the former can be implemented as partially programmable delay elements (PPDEs) where only one edge of the signal is controlled or fully programmable delay elements (FPDEs) where both the rising and falling edges of the signal are controlled. Additionally both analog and digital solutions can be applied to a partially or a fully programmable delay element. Analog techniques provide a compact design but are not suitable for the digital implementation of previously analog blocks. On the other hand, digitally programmable delay elements (DPDE) provide better noise immunity and are not susceptible to the offset and drift phenomena. Furthermore, DPDEs offer more flexibility and are more robust. Regardless of the control technique and desired flexibility, DPDEs are required to dissipate a negligible amount of the total system power. In addition, the delay must be monotonic with increasing input code.

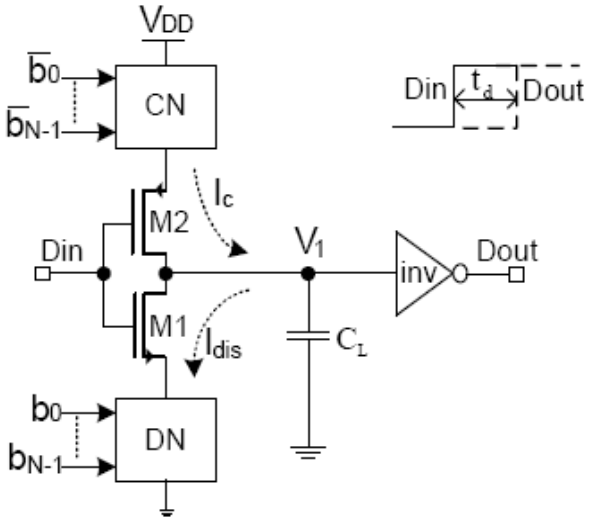
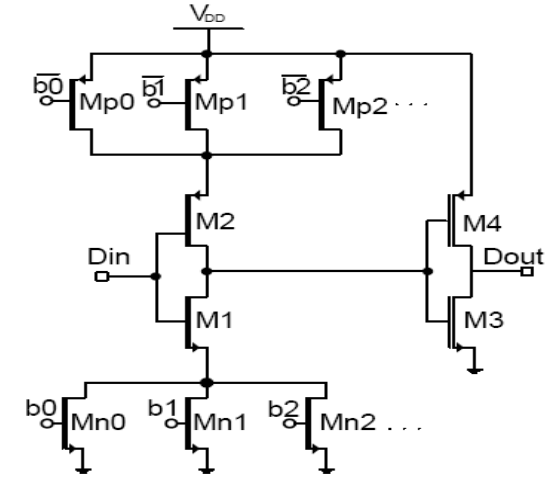


Fig.1 Basic structure of CSI DPDE

In this paper, two low power digitally programmable delay elements are proposed. The partially programmable structure uses a combination of a switched current mirror (CM) and gate decoupling techniques while the fully programmable topology uses switched current mirror and a Schmitt type inverter to reduce power consumption. Section 2 reviews typical current-starved inverter (CSI) based DPDEs;



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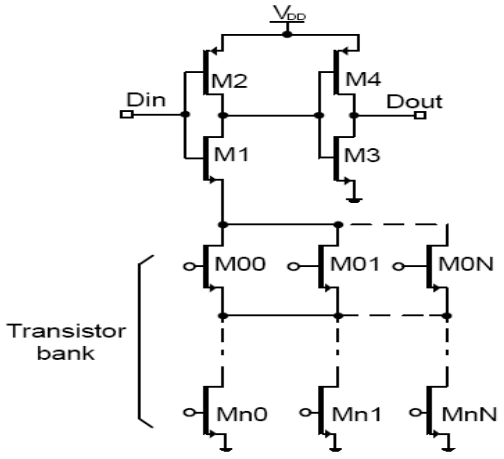


(b)

Fig. 2 Variable Resistance CSI DPDEs (a)Simple Control (b) transistor tank control

The proposed switched current mirror based DPDE is presented in Section 3 while simulation results are provided in Section IV; Conclusions are drawn in Section V.

2 Programmable Delay Elements

A typical CSI based DPDE adopts the structure shown in Fig. 1. It incorporates a regular inverter as the core part to which the input signal, Din, to be controlled is applied and a control part used to manipulate the core. The control part consists of a discharge network (DN) and or a charging network that is controlled by the digital input code. In the case of a partially programmable structure only one of the networks is present. An output inverter, INV, is usually added to achieve rail-to-rail voltages. The aim is to control the delay t_d of the edges of Din. Fig. 2 shows a typical implementations of the control networks using switched transistors [6][7]. Fig.2 (a) uses a single row of transistors while Fig. 2(b) uses a transistor bank. The switching of these transistors control the effective resistances at the source of M1/M2. On the rising edge of Din the parasitic capacitance C_1 at the drain of M1 discharges at a rate depending on the current through M1. On the other hand, this current depends on the resistance seen at the source of M1. The output inverter formed by transistors M3 and M4 then provides rail-to-rail output. On the falling edge of Din, the opposite happens where the capacitance at the drain of M2/M1 is charged towards V_{DD}. The structure is simple and is frequently used in the design of DCOs. In reality, the delay also depends on the parasitic capacitance C_p at the source of M1/M2. On the rising edge of the input signal, charge sharing occurs between the parasitic capacitances at the drain and source nodes of M1. When the the input signal if low, the capacitance at the source of M6 is discharged to ground. Assuming that C_1 is initially charged to V_{DD} during this time, charge conservation gives the final voltage, V_{CF}, on C_1 immediately after charge sharing as

$$V_{CF} = \frac{C_1}{C_1 + C_p} V_{DD} \quad (1)$$

On the other hand, C_p is different and unpredictable for different combinations of control transistors that are turned on. Consequently, it is difficult to guarantee the amount of charge sharing that will occur for any particular combination. Therefore, this delay element has a non-monotonic delay with increasing input code.

This issue has been analyzed in [8] and a new control technique based on current mirrors (CMs), [9,10] has been proposed to achieve monotonic delay. Fig. 3 shows the CM based DPDE. The partially programmable structure is shown in Fig. 3(a) and consists of control transistors (M0, M1, M2), current source transistor M3, current mirror transistors M4 and M5 and the input and output inverters. The input current I_{in} is provided by the current I_0 through M3 and the currents, I_0, I_1 and I_2 through the control transistors. The number of control transistors can be varied as desired. By switching the control transistors on and off, I_{in} can be controlled. This current flows through M4 and is mirrored to M5 according to (2)

$$I_5 = \frac{W_5/L_5}{W_4/L_4} I_{in} \quad (2)$$

where W and L are the width and length of the corresponding transistors, respectively. M5 has the

same width and length as M4 but is smaller than M6. M5 is made smaller than M6 so that the current is controlled by M5 and not M6. The operation of the CM based partially programmable delay element is as follows: When the input signal is low, M6 is off while M7 charges C_{o1} to V_{DD}. As soon as the input goes high, M6 turns on and C_{o1} starts to discharge. When V_1 crosses V_{DD}-V_{TP9}, M9 begins to turn on while M8 begins to turn off and the output assumed to be in saturation for most of the delay time, it experiences velocity saturation [11] and its current is given as

$$I_5 = \frac{k_n W_5}{2L_5}\left(V_{IN} - V_{TN5}\right)\left(1 + \lambda_5 V_{DS5}\right) \quad (3)$$

The parameters k_n and λ_5 denote the process channel effect parameters of M5, respectively. V_{in}, V_{TN5} and V_{DS5} are the gate, threshold and drain-source voltages of M5, respectively. The discharge current of C_{o1} is given as

$$I_{dis} = -C_{o1}\frac{dV_1}{dt} \quad (4)$$

Combining (3) and (4) gives an expression for V_1 as

$$V_1 = (V_{DD} - 1/\lambda_5)e^{-t/\tau_1} - 1/\lambda_5 \quad (5)$$

Where $\tau_1 = C_{o1}/K_1\lambda_5$ and

$$K_1 = \frac{k_n W_5}{2L_5}\left(V_{in} - V_{TN5}\right) \quad (6)$$

The time t_{d1} can now be estimated as

$$t_{d1} = \tau_1 Ln\frac{1 + \lambda_5 V_{DD}}{1 + \lambda_5\left(V_{DD} - |V_{TP9}|\right)} \quad (7)$$

Or more precisely as

$$t_{d1} = \frac{K_3}{\left(V_{in} - V_{TN5}\right)} \quad (8)$$

Where

(9)

Assuming that the current I_5=I_{in} where

$$K_3 = \frac{C_{o1}}{k_n W_5\lambda_5/2L_5}.Ln\frac{1 + \lambda_5 V_{DD}}{1 + \lambda_5\left(V_{DD} - |V_{TP9}|\right)}$$

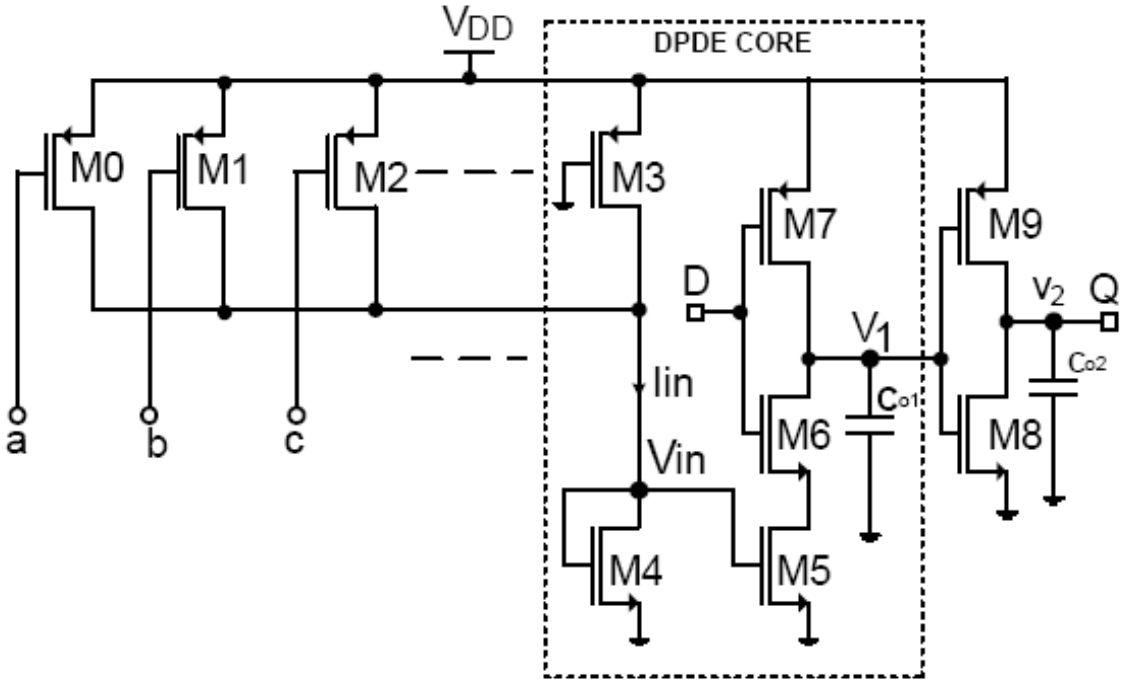
$$I_{in} = I_3 + I_3\sum_{k=0}^{N} 2^k \bar{b}_k \quad (10)$$

capacitance C_{o2} is charged towards V_{DD}. Since the rate of discharge of C_{o1} depends on the current through M5, the delay t_d can be conveniently programmed with the digital input code. The delay t_d is the sum of the time t_{d1} for V_1 to drop to V_{DD}-V_{TP9} and the time t_{d2} for V_2 to rise from ground to $V_{DD}/2$. By equating the currents through M5 and to the discharge current of the capacitance C_{o1}, the time t_{d1} can be obtained. Since transistor M5 is a small and is Where $k = 0,1...N-1$ is the bit number, I_3 is the current through M3 and the second term is the total current through the N control transistors where a control transistor is on if $\bar{b}_k$ =0, and off if otherwise. To estimate the less dominant part of the delay t_{d2}, the current through M9 when it turns on and the charging current of the output capacitance C_{o2} are considered as follows:

$$I_{D9} = \frac{k_p W_9}{2L_9}\left(V_{DD} - V_1 - V_{TP9}\right)^2 = C_{o2}\frac{dV_2}{dt} \quad (11)$$

The expression for t_{d2} can then be obtained by combining (7) and (11). Since t_{d1} is the main and dominant part of the delay due to current starving and depends on V_{in} and therefore I_{in}, it can be concluded that the delay of this delay element monotonic and is not influenced by charge sharing. Furthermore, the design of this delay element is straightforward and the structure is also less susceptible to temperature variations. This delay element has been used in the implementation of a high performance dual loop DLL [12] and an all-digital DLL [13].

A principal drawback of this delay element is that it consumes considerable amount of static and short-circuit power. There are two main sources of current dissipation in the delay elements of Fig. 3. When the input is low, unnecessary static current continues to flow through M4 Fig. 3(a) and when the input signal is high unnecessary static current flows through M5 in Fig. 3(b). Another source of power consumption is the short-circuit current through the output inverter transistors, that is M8&M9 in Fig. 3(a) and M11&M12 of Fig. 3(b). This is an inherent consequence of the current-starving nature of the delay element. Since the voltage V_1 exhibits slow transitions, especially under low charge/discharge current, the output transistors could be turned on simultaneously for a long period of time. This will allow significant direct currents. The static current can be reduced by choosing smaller W/L ratios for the control transistors. However, such a technique may lead to reliability issues and even higher short-circuit current in the output transistors.



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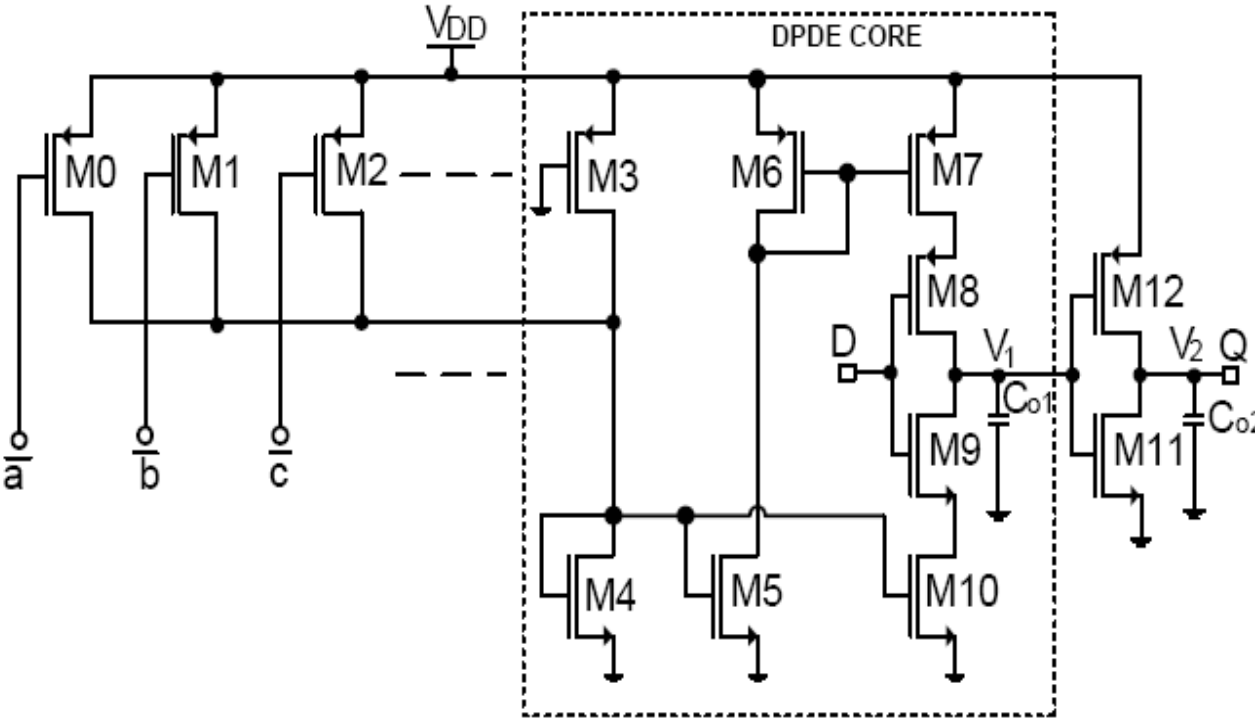


(b)

Fig. 3 Conventional CM DPDE (a) Partially Programmable (b) Fully Programmable

3 Proposed Switched Current Mirror DPDE

Fig. 4 shows the two structures of the proposed delay element. The partially and fully programmable topologies are shown in Fig. 4(a) and Fig. 4(b), respectively. The control method and delay profile are similar to the conventional approach in Fig. 3. The main difference between the proposed structure and the conventional CM delay element architectures of Fig. 3 lie in the power management. In the traditional technique, drain switching is used where the input inverter NMOS is placed at the drain of current mirror transistor M5. In such a case, when the input signal is low, the drain of M5 is discharged to ground. As soon as the input signal turns high, this drain rises to V_{DD}-V_{TN6}. Therefore, M5 starts operating in the linear region before entering saturation. In the proposed partially programmable DPDE shown in Fig. 3(a), source switching, rather than drain switching, technique is used. The input inverter NMOS (M6) is placed at the source of current mirror Transistor M5. This technique allows two improvements in the delay element. Firstly, the sources of the current mirror transistors M4 and M5 can be connected together. In this way when the input signal D is low, there is no static current flow through M4 and current is available only when the input signal is high. A 50% reduction of static current results from this switched current mirror technique. Secondly, since the drain of M5 is at V_{DD} when the input turns high and remains fairly high for most of the delay time t_{d1}, the source switching allows M5 to be in saturation in the beginning and for most of the delay time which improves the current mirroring effect.

Static current is not the only source of power dissipation in the conventional CM DPDE. On the transition edge of the input signal, one of the output transistors begins to turn on while the other begins to turn off. Current starving allows these output transistors to be on simultaneously for a considerable amount of time leading to short-circuit current through the transistors. The short-circuit current in the conventional CM DPDE is due to the fact that the gates of the output transistors are tied together and controlled by the same nodal voltage, V_1. To obviate the direct currents in the output transistors, the gate control voltages of M8 and M9 in Fig. 4(a) are decoupled and separately controlled. While the gate of M9 is directly controlled by the voltage at the output of the input inverter, the output of the extra inverter consisting of M10&M11 is used to control the gate of M8. The source of M11 is connected to the gate of M9. When the input signal turns high, transistor M7 and M11 turn off while M10 quickly turns on and pulls the gate of M8 to ground. Therefore M8 switches off rapidly as soon as the input signal rises and since M9 is switched on by the current starved inverter, no short-circuit current will flow. On the other hand, when the input signal falls, M7 turns on and quickly pulls up the gate of M9. Since M11 turns on only after V_1 is greater than V_{DD}-V_{TP11}, the gate voltage of M8 will lag behind that of M9 so that there is no short-circuit currents through the out put transistors. In the fully programmable delay element of Fig. 4(b) source switching technique has also been used also resulting in considerable static current reduction. However, due to the fully programmable technique, static current needs to flow continuously through the branch consisting of M3, M4, M6. Furthermore, a Schmitt type inverter is used to replace the regular output inverter. The kind of gate decoupling used in the partially programmable delay structure cannot be used in the fully programmable structure because both the rising and falling edge of the input signal need to be controlled. Instead a Schmitt type inverter is employed to replace the regular inverter. The advantage of the Schmitt inverter is that, the low-to-high switching threshold is lower and the switching is faster. Therefore, the time when NMOS and PMOS transistors are both on is very insignificant. There is a possible mismatch in the currents of the current mirror. Considering the single ended structure of Fig. 4 (a) and assuming that M4 and M5 are in saturation, their drain currents are given respectively as

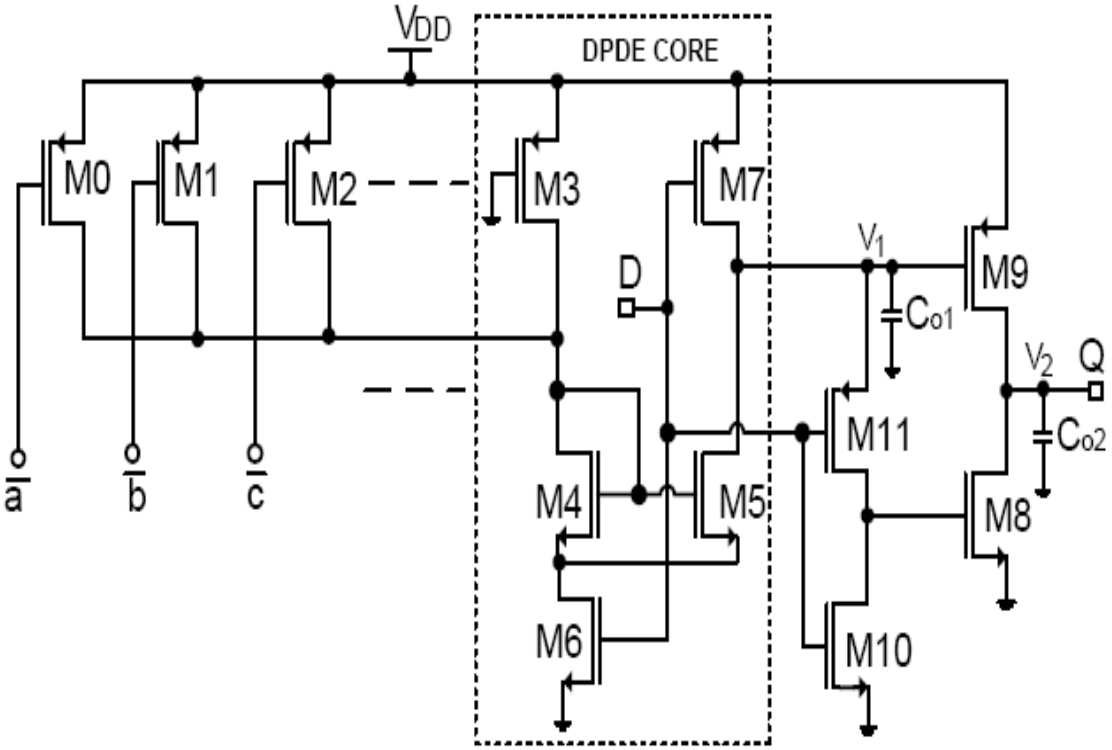
$$I_{D4} = \mu_n C_{ox} \left(\frac{W_4}{2L_4}\right)(V_{IN} - V_{TN})^2 \qquad (12)$$

$$I_{D5} = \mu_n C_{ox} \left(\frac{W_5}{2L_5}\right)(V_{IN} - V_{TN})^2 \qquad (13)$$

Neglecting mismatches in $\mu_n C_{ox}$, the current mismatch can be estimated as

$$\Delta I_D = \frac{1}{2}\mu_n C_{ox}[(V_{IN} - V_{TN})^2 \Delta\left(\frac{W}{L}\right) - 2\frac{W}{L}(V_{IN} - V_{TN})\Delta V_{TH} \qquad (14)$$

Normalizing this current difference to the average drain-source current in the mirror transistor gives



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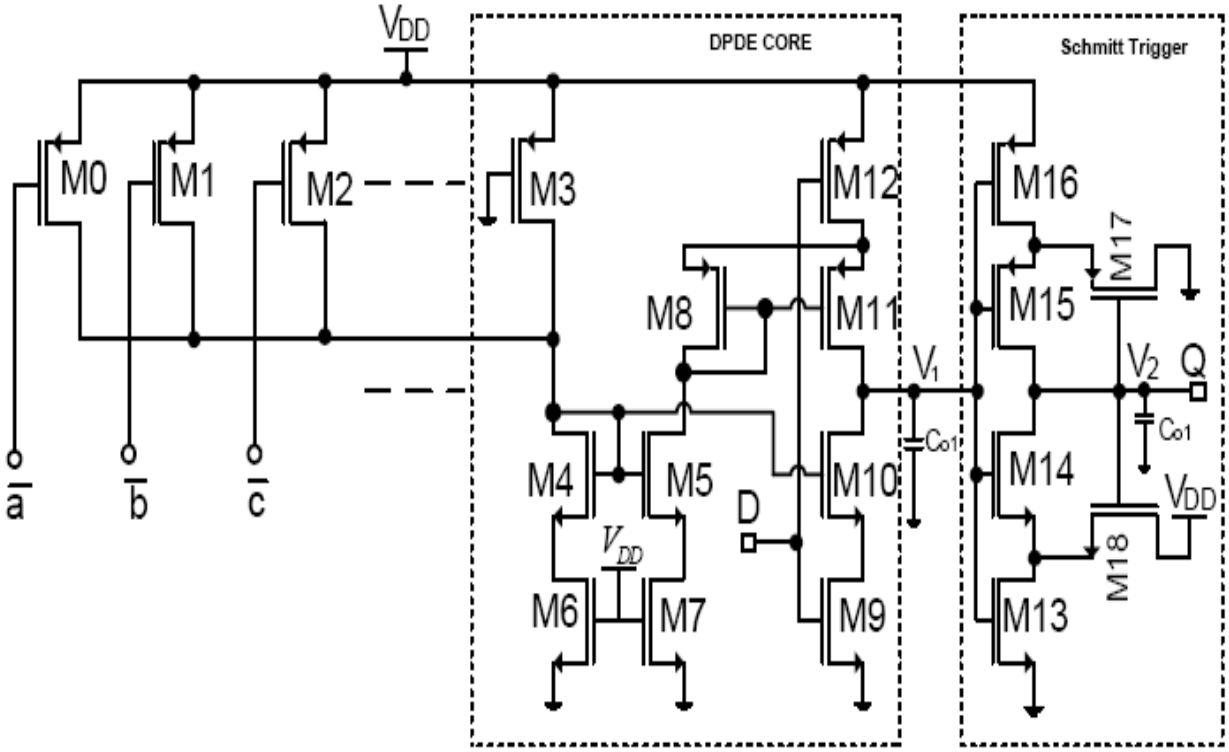

(b)

Fig. 4 Proposed CM DPDE (a) Partially programmable (b) fully programmable

The random physical variables have a normal distribution with zero mean and their standard deviation depends on device area (WL) and device physical distance for pairs of matched transistors [11]. Considering that threshold voltage (ΔV_{TH}) and current factor (β) differences are the dominant sources of mismatch between identical MOS transistors. Therefore, the variance of the relative drain–source current errors can be estimated as

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right)=\sigma^2\left(\frac{\Delta\beta}{\beta}\right)+\left(\frac{g_m}{I_D}\right)^2\sigma^2\left(\Delta V_{TH}\right) \qquad (15)$$

Where the parameter β is the current factor. In practice, it is assumed that the V_{TH} mismatch is dominant over the β mismatch. So the standard deviation of the drain source current mismatch can be estimated as

$$\sigma\left(\frac{\Delta I_D}{I_D}\right)=\frac{1}{\sqrt{WL}}\cdot\frac{2A_{V_{TH}}}{V_{GS}-V_{TH}} \qquad (16)$$

Where the parameter $A_{V_{TH}}$ is a technology constant and is known to scale with gate oxide thickness. Therefore, the mismatch can be reduced by using large current mirror transistors and laying out the devices close to each other.

Combining (8) and (14), it can be seen that though some delay in accuracy results with respect to control code, the circuit still maintains monotonic characteristics which is often more critical. For short channel devices, the I-V characteristics differ from the analysis above because of velocity saturation, mobility degradation due to vertical field and threshold voltage variation with drain-source voltage. The velocity saturated MOS drain current is given as

$$I_{in}=\upsilon_{sat}WC_{ox}\left(V_{GS}-V_{TH}\right) \qquad (17)$$

Where υ_{sat} is the saturation velocity of carriers. Similar derivations show that, the current mismatch follows the same trend as for the square law scenario but is independent of transistor length *L*. Since the current has a linear variation with V_{GS}, the CM DPDE can provide more linear delay in modern technologies. On the other hand, the leakage current in such technologies will tend to be dominant though lower supply voltages can mitigate this problem to an extend.

The maximum and minimum delays of the proposed delay elements are mainly influenced by the current source transistor M3 and control transistors M0-M2, respectively. Therefore, the sizes of these transistors can be determined accordingly. Given the number of required controllable delays k, the number of PMOS controlling transistors N can be determined from $N=Log_2(k)$. M3 is sized to obtain maximum delay and then another transistor, say MT, connected in parallel with M3 is sized to obtain the minimum required delay. This transistor is then broken down into the number of required control transistors having equal lengths. The widths are sized in a binary fashion so that

$$W_T=\sum_{i=0}^{N-1}2^iW_0 \qquad (18)$$

Where, W_T is the width of MT and W_0 is the width of the smallest control transistor. The parameter *i* represents the weight of the control transistor where $W_i=2^iW_0$. The current mirror transistors should be of the same size and non-minimum length to allow more accurate copying while the sizes of the output transistors are determined by the load capacitance.

In the fully programmable DPDE of Fig. 4(b), the transistors of the Schmitt trigger are sized depending on desired switching threshold. The low and high thresholds V_L and V_H are respectively chosen as 0.2V and 0.7V. To compute the corresponding transistor dimensions, the saturation current of M13 and M18 are set to be equal and that of M16 and M17 are also set to be equal giving

$$k_{13}\left(V_H-V_{TN13}\right)^2=k_{18}\left(V_{DD}-V_{S18}-V_{TN18}\right)^2 \qquad (19)$$

$$k_{16}\left(V_{DD}-V_L-\left|V_{TP16}\right|\right)^2=k_{17}\left(V_{s17}-\left|V_{TP17}\right|\right)^2 \qquad (20)$$

The parameter $k_i=0.5\mu_iC_{ox}W_i/L_i$, where μ_i is the mobility of electrons in the case of NMOS or holes in the case of PMOS, V_{TN} and V_{TP} are the threshold voltages of the corresponding NMOS and PMOS transistors, respectively. V_{S18} and V_{s17} are the source voltages of M18 and M17, respectively. The respective switching threshold voltage expressions can therefore be estimated as [13]

$$V_H=\frac{\alpha V_{DD}+V_{TN18}}{1+\alpha} \qquad (21)$$

$$V_L = \frac{V_{DD} - |V_{TP17}|}{1+\beta} \quad (22)$$

Where $\alpha = \sqrt{k_{18}/k_{13}}$ and $\beta = \sqrt{k_{17}/k_{16}}$.
From (21) and (22) the widths of the Schmitt trigger transistors can be estimated. Table I summarizes the dimensions of the designed Schmitt trigger. Minimum lengths are chosen for all the transistors. The parameters α=0.25 and β=1 to satisfy the required switching.

Table I Schmitt Trigger Transistor Sizes

	M13	M14	M15	M16	M17	M18
W(um)	8	16	32	8	8	2
L (um)	0.18	0.18	0.18	0.18	0.18	0.18

The transistors M15 and M16 provide a way of fine tuning the switching threshold.

4 Simulation Results

To verify the effectiveness of the proposed techniques, the design was implemented and simulated in a standard 0.18um 1P6M technology. A voltage supply of 1V was used with an input signal frequency of 450MHz. Fig. 5 shows the gate voltages of M8 and M9 of Fig. 4 (a). On the rising edge of the input signal, the falling voltage on the gate of M8 leads that of M9 so that M8 switches off before M9 switches on and short-circuit current flow is not possible even for the lowest control current. On the other hand, when the input signal falls, the gate voltage of M9 leads that of M8 so that M9 switches off before M8 switches on and direct current is also avoided. The overall effect is that only one output transistor is on at any given time and no direct currents flow. The proposed partially programmable delay element (Fig. 4(a)) was simulated with different input digital codes varying from 0000 to 1111. This input code can be increased as desired. The output voltage variation for the different codes is shown in Figure 6 where the time for the rising edge of the output reduces with increasing input code. To further illustrate this fact, the variation of delay with different input codes is given in Fig. 7. As expected, the delay is monotonic with increasing input code. The delay range is about 350~800ps. To verify the designed switching thresholds of the designed Schmitt trigger, a slowly varying input voltage was used and the effect is shown in Fig. 8. The output switches correctly at 0.2 and 0.7. Fig. 9 shows the output of the fully programmable delay element with a 1V supply. The delay is also monotonic with increasing input digital code. However, it is difficult to achieve symmetrical delays for the rising and falling edges. This is mainly due to the stacking of rising and falling edge control networks. This arrangement forces the sizing of the discharge path transistors to influence the sizing of the charge path transistor and vice versa. Increasing the sizes of the PMOS in the input inverter reduces the delay of the falling edge but increases that of the rising edge. Like wise, increasing the sizes of the NMOS transistors of the input inverter reduces the delay of the rising edge but increases the delay of the falling edge. Table II summarises the performance of the proposed partially programmable delay element and compares it with the conventional structure. The proposed structure dissipates less than 50% power compared with the conventional topology.

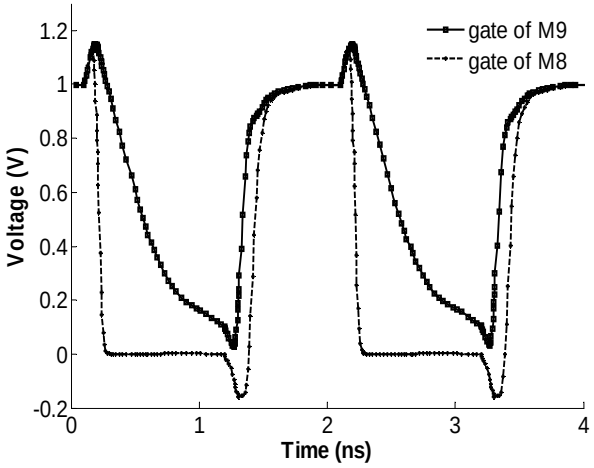

Fig. 5 Gate control voltage of M8 and M9

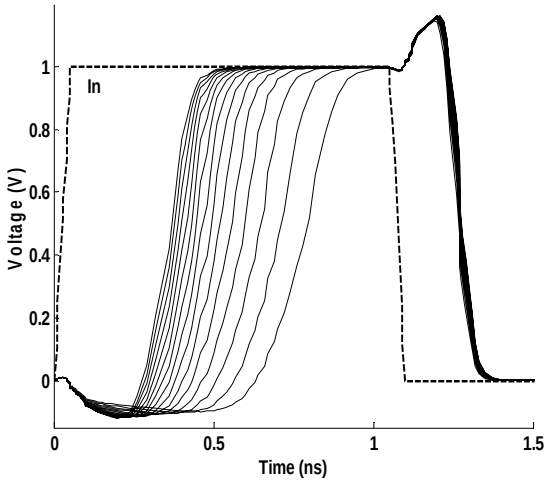

Fig. 6 Output voltage for different codes

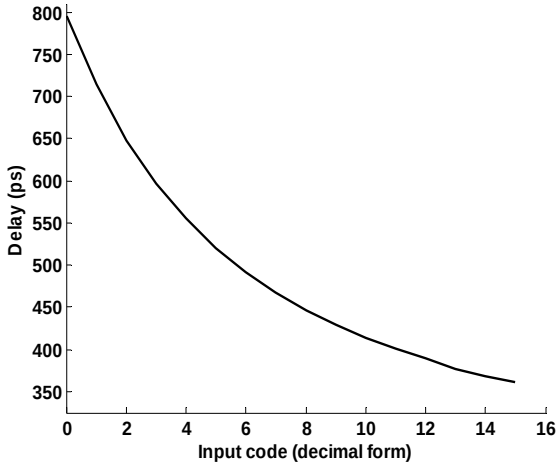

Fig. 7 Delay variation with input code

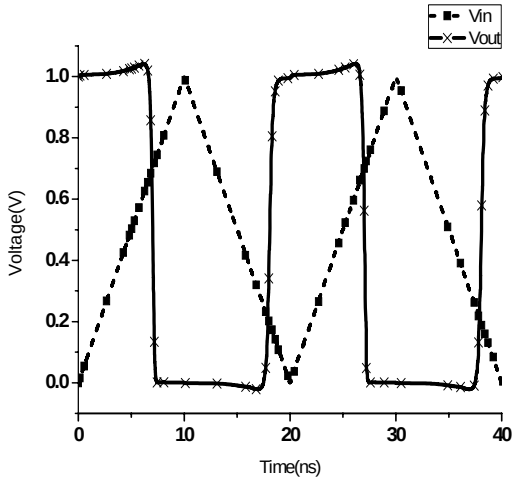

Fig. 8 Schmitt Trigger Transient response

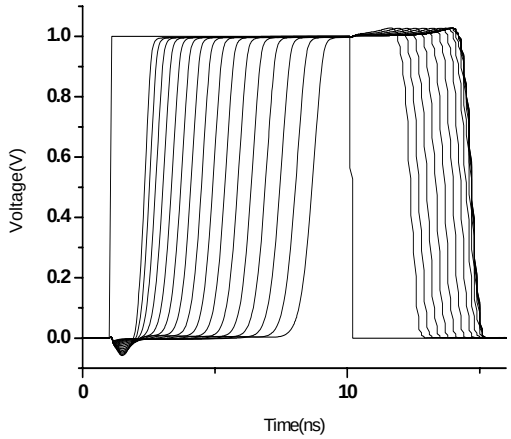

Fig. 9 Transient response of FPDPDE

Table II PPDE Performance Summary

Parameter	**[2]**	**Proposed**
Supply Voltage (V)	1.8	1
Static power (uW)	136	leakage power
Dynamic Power (uW)	75	Maximum=36
Total power (uW)	211	36
Monotonic	Yes	Yes
Speed (MHz)	400	450
Tuning Range (ps)	300~750	350~800

5 Conclusion

Two low power digitally programmable delay elements with monotonic characteristics have been described in this paper. The first structure, referred to as partially programmable DPDE, can be used when only one edge of the input signal needs to be varied while the second structure, referred to as fully programmable DPDE, allows control of both the rising and falling edges of the input signal. The often neglected aspect of short-circuit current in the output transistors have been separately addressed using gate decoupling and Schmitt trigger. Furthermore, switched current mirrors have been used in both structures to reduce or eliminate static current. The two structures are also suitable for many digital and mixed signal circuits where it is needed to adjust the signal period.

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