Applying FPGA-based Chip to Apparent Power and Power Factor Measurement Considering Nonsinusoidal and Unbalanced Conditions

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Abstract: - This paper proposes a field-programmable gate array (FPGA)-based integrated circuit (IC) for computing apparent powers and power factors of power systems. In a nonsinusoidal and unbalanced three-phase power system, the calculation of apparent powers and power factors has many definitions. Load characteristics of harmonic and unbalance can not be expressed in the traditional apparent power and power factor, which only consider the fundamental and three-phase balanced sinusoidal conditions. This paper utilizes the FPGA chip to develop the platform to implement the calculation methods of apparent powers and power factors. The proposed design scheme is developed using the very high speed integrated-circuit hardware description language (VHDL), which provides high flexibility and technology independence. This paper discussed the effective power and power factor, the arithmetic power and power factor, and the fundamental power and power factor. The design of filters for the computation of fundamental frequency components is given. ModelSim is used at first to simulate the calculation of apparent powers and power factors to ensure the accuracy of timing and function. Research results show that the designed chip can compute accurately the apparent powers and power factors considering the effects of nonsinusoidal and unbalanced conditions.

Key-Words: - FPGA, SoC, Power Factor, Harmonic, Unbalanced Power System.

1 Introduction

The nonlinear and fluctuating loads would cause power quality disturbances [1-4]. The value of power factor generally is an important penalty factor in the revenue of electricity customers. However, the traditional power factor definition always assumes that the load condition is sinusoidal. The effects of load unbalance and harmonic distortion are neglected. It has been reported that if traditional electro-mechanical meters are used in circumstances of nonsinusoidal and three-phase unbalanced voltages or currents, the errors can reach 20%~30% [5]. In recent years, there are many discussions regarding the power definitions and calculations [6-11]. Several definitions are given in the IEEE Std. 1459, such as effective apparent power, arithmetic apparent power, and vector apparent power.

Since harmonic pollution, load unbalance, and reactive power fluctuation could affect the power factor values of customers, six different definitions of power factor values have been investigated for the same recorded measurement data of customers in [12]. The different results of calculation are dependent on the load characteristics. In [13], it is shown that the currently used apparent power definitions, namely the Arithmetic VA and the Vector VA, both lack an important property.

The usage and performance of FPGA has risen significantly in recent years for its reconfigurability and flexibility. The FPGA has been applied to analyzing and controlling a power system [14-15]. The major difference between FPGA and DSP-based solutions is that FPGA enables simultaneous execution of all control subroutines, which allows

high performance and novel control methods [16]. While conventional designs are based on functions, FPGA is based on the reuse of IP or the function assembly. When a large system is constructed from a number of macro-modules, IP cores can be used to represent those modules. Several particular functional IP cores such as CORDIC and FFT cores could be developed. VHDL was also employed to model a digital control system at many levels [17]. VHDL can be considered as a combination of sequential, concurrent, netlist, timing specification, and waveform generation languages. It utilizes the top/down design methodology and can be used to model a complete digital electronic system. The design benefits include easy error correction and technology independence. The same algorithm can be synthesized into any other FPGA.

Since good definitions of apparent powers and power factors may well reflect the practical situations of three-phase unbalanced and non-sinusoidal circuits, the effective power, effective power factor, arithmetic power, and arithmetic power factor are investigated in this paper. The calculation algorithms will be implemented by using a FPGA-based chip [18-19]. The methods to obtain the fundamental frequency components are also compared. The effects of nonsinusoidal and unbalanced conditions in a three-phase power system are alsoconsidered.

2 Power Factor Definition

2.1 Single-phase system

For a single-phase load under sinusoidal condition, the instantaneous voltage and current are, respectively,

$$v(t) = \sqrt{2}V\sin(\omega t + \alpha) \tag{1}$$

$$i(t) = \sqrt{2}I\sin(\omega t + \beta) \tag{2}$$

Hence the apparent power, active power, and reactive power are, respectively,

$$S = VI \tag{3}$$

$$P = VI\cos\theta \tag{4}$$

where $\theta = \alpha - \beta$ is the phase angle difference between voltage and current.

$$Q = VI\sin\theta \tag{5}$$

$$PF = \frac{P}{S} = \frac{P}{\sqrt{P^2 + Q^2}} \tag{6}$$

When a single-phase system is under non-sinusoidal situation, the instantaneous voltage and current values can be

$$v(t) = V_0 + \sqrt{2}\sum_{h=1}^{\infty} V_h \sin(h\omega t + \alpha_h) \tag{7}$$

$$i(t) = I_0 + \sqrt{2}\sum_{h=1}^{\infty} I_h \sin(h\omega t + \beta_h) \tag{8}$$

where

V_0：average voltage
I_0：average current
$V_{h,}$：rms values of harmonic voltages
$I_{h,}$：rms values of harmonic currents
α_h：phase angles of harmonic voltages
β_h：phase angles harmonic currents

The root mean squared (rms) values are give by

$$V_{RMS} = \sqrt{\sum_{h=0}^{\infty} V_h^2} \tag{9}$$

$$I_{RMS} = \sqrt{\sum_{h=0}^{\infty} I_h^2} \tag{10}$$

The apparent power, active power, and reactive power are

$$S = V_{RMS} I_{RMS} \tag{11}$$

$$P = \sum_{h=0}^{\infty} V_h I_h \cos(\alpha_h - \beta_h) \tag{12}$$

$$Q_B = \sum_{h=1}^{\infty} V_h I_h \sin(\alpha_h - \beta_h) \tag{13}$$

Then the power factor is defined as

$$PF = \frac{P}{S} \neq \frac{P}{\sqrt{P^2 + Q_B^2}} \tag{14}$$

Because $S \neq \sqrt{P^2 + Q^2}$. There is a definition of the distortion power as

$$D_B = \sqrt{S^2 - P^2 - Q_B^2} \tag{15}$$

2.2 Three-phase system

Arithmetic apparent power and arithmetic power factor are, respectively

$$S_A = S_R + S_S + S_T = V_R I_R + V_S I_S + V_T I_T \tag{16}$$

$$PF_A = \frac{P}{S_A} \tag{17}$$

Effective apparent power and effective power factor are, respectively

$$S_e = 3V_e I_e \tag{18}$$

$$PF_e = \frac{P}{S_e} \tag{19}$$

In a three-phase four-wire system:
Effective current

$$I_e = \sqrt{\frac{I_R^2 + I_S^2 + I_T^2 + I_N^2}{3}} \tag{20}$$

Effective voltage

$$V_e = \sqrt{\frac{1}{18}\left[3\left(V_R^2 + V_S^2 + V_T^2\right) + \left(V_{RS}^2 + V_{ST}^2 + V_{TR}^2\right)\right]} \tag{21}$$

In a three-phase three-wire system:
Effective current

$$I_e = \sqrt{\frac{I_R^2 + I_S^2 + I_T^2}{3}} \tag{22}$$

Effective voltage

$$V_e = \sqrt{\frac{V_{RS}^2 + V_{ST}^2 + V_{TR}^2}{9}} \quad (23)$$

The fundamental apparent power and fundamental power factor are, respectively

$$S_{A1} = S_{R1} + S_{S1} + S_{T1} = V_{R1}I_{R1} + V_{S1}I_{S1} + V_{T1}I_{T1} \quad (24)$$

$$PF_{A1} = \frac{P}{S_{A1}} \quad (25)$$

In this paper, there are three definitions for the average power factor.

(a) average arithmetic power factor

$$PF_A = \frac{\int_T P(t)dt}{\int_T S_A(t)dt} \quad (26)$$

(b) average effective power factor

$$PF_e = \frac{\int_T P(t)dt}{\int_T S_e(t)dt} \quad (27)$$

(c) average fundamental power factor

$$PF_{A1} = \frac{\int_T P(t)dt}{\int_T S_{A1}(t)dt} \quad (28)$$

2.3 Evaluate of harmonic and unbalance load

The effective voltage and current of fundamental components of the three-phase four-wire system are given by

$$V_{e1} = \sqrt{\frac{1}{18}\left[3\left(V_{R1}^2 + V_{S1}^2 + V_{T1}^2\right) + \left(V_{RS1}^2 + V_{ST1}^2 + V_{TR1}^2\right)\right]} \quad (29)$$

$$I_{e1} = \sqrt{\frac{I_{R1}^2 + I_{S1}^2 + I_{T1}^2 + I_{N1}^2}{3}} \quad (30)$$

Those of the three-phase three-wire system are given by

$$V_{e1} = \sqrt{\frac{V_{RS1}^2 + V_{ST1}^2 + V_{TR1}^2}{9}} \quad (31)$$

$$I_{e1} = \sqrt{\frac{I_{R1}^2 + I_{S1}^2 + I_{T1}^2}{3}} \quad (32)$$

The fundamental effective apparent power is

$$S_{e1} = 3V_{e1}I_{e1} \quad (33)$$

Then, the nonfundamental effective apparent power is

$$S_{eN} = \sqrt{S_e^2 - S_{e1}^2} \quad (34)$$

The normalized nonfundamental effective apparent power is

$$\bar{S}_{eN} = \frac{S_{eN}}{S_{e1}} \quad (35)$$

When there is an unbalanced three-phase situation, the fundamental positive-sequence apparent power is

$$S_1^+ = 3V_1^+I_1^+ = \sqrt{\left(P_1^+\right)^2 + \left(Q_1^+\right)^2} \quad (36)$$

where

$$V_1^+ = \frac{1}{3}\left(V_{R1} + aV_{S1} + a^2V_{T1}\right)$$

$$I_1^+ = \frac{1}{3}\left(I_{R1} + aI_{S1} + a^2I_{T1}\right) \quad , a = 1\angle 120^0$$

The unbalanced fundamental apparent power is

$$S_{1U} = \sqrt{S_{e1}^2 - \left(S_1^+\right)^2} \quad (37)$$

The normalized fundamental unbalanced apparent power is

$$\bar{S}_{1U} = \frac{S_{1U}}{S_1^+} \quad (38)$$

3 Low-Pass Filter

In calculation of the fundamental frequency components, the low-pass filter is used to obtain the 60-Hz components and reject harmonic components. The impulse response of the filter is computed by Matlab.

Infinite-duration impulse response (IIR) digital filters have the input-output characteristics which are governed by linear constant-coefficient difference equations of a recursive nature. The transfer function of an IIR digital filter is a rational function in z^{-1}. Consequently, for a prescribed frequency response, the use of an IIR digital filter generally results in a shorter filter length. However, the improvement is achieved at the expense of phase distortion and a transient start-up interval.

Finite-duration impulse response (FIR) digital filters have the operation which is governed by liner constant-coefficient difference of nonrecursive nature. The transfer function of an FIR digital filter is a polynomial in z^{-1}. Consequently, the FIR digital filters exhibit three important properties:

(a) FIR filters can realize a desired magnitude response with an exactly liner phase response without phase distortion.

(b) FIR filters are always BIBO.

(c) FIR filters have finite memory, and transient star-up duration is limited.

This paper uses FIR filters to strain harmonic components and utilizes Kaiser window filter design method. The band characteristics of a low-pass filter are given in Fig. 1. The cutoff frequency of the ideal low-pass filter should let

TABLE I Kaiser Parameter

As	β	ω_P	ω_S	M
40dB	3.3953	0.031π	0.0938π	72

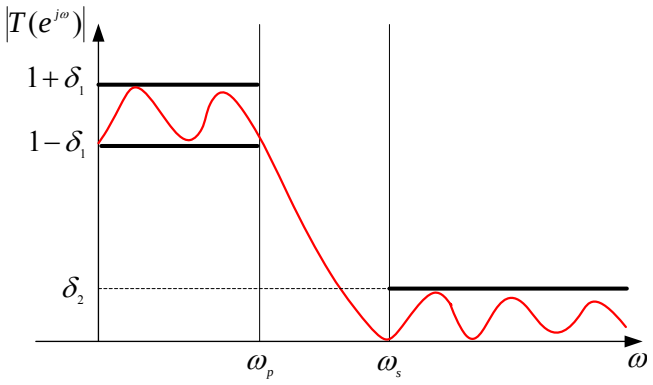

Fig.1. Band characteristics of a low-pass filter.

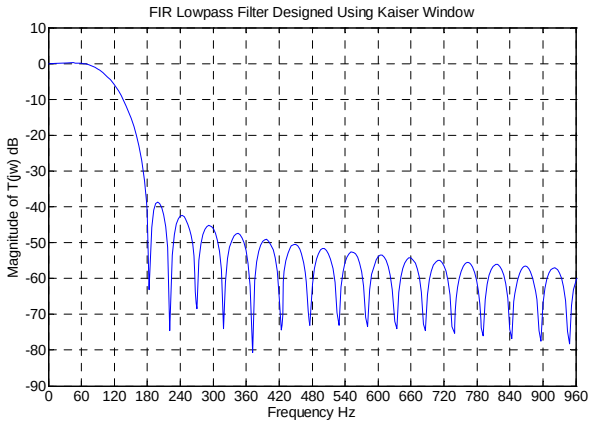

Fig.2. Low-pass filter designed by Kaiser window.

Fig.3. Single-phase circuit including harmonic current sources.

TABLE II Setting of fundamental frequency components

Voltage	f_1 (Hz)	P_1 (W)	Q_1 (VAR)	PF_1
220(V)	60	1200	1600	0.6

TABLE III harmonic current (A)

I_3	I_5	I_7	I_9	I_{11}
2.12	1.27	0.90	0.71	56

$$\omega_c = \frac{\omega_p + \omega_s}{2} \tag{39}$$

ω_s : the passband cutoff freuency

ω_p : the stopband cutoff freuency

It is determined empirically that the values of β need to achieve a specified value of A_s, and is give by

$$\beta = \begin{cases} 0.1102(As-8.7) & As > 50 \\ 0.5842(As-21)^{0.4} & \\ +0.07886(As-21) & 21 \le As \le 50 \\ 0 & As < 21 \end{cases} \tag{40}$$

A_s is the attenuation parameter of stop band.

$$M = \begin{cases} \dfrac{As-7.95}{14.36\times\Delta f}+1 & As > 21 \\ \dfrac{0.922}{\Delta f}+1 & As \le 21 \end{cases} \tag{41}$$

The Kaiser parameters used in this paper is given in TABLE I. The spectrum characteristics are given in Fig. 2. The FIR filter has the good ability to filter our the higher frequency components and the fundamental frequency components can be obtained.

4 Calculation of Fundamental Frequency Components

The simulation blocks were developed using the Simulink and Sim Power Systems, which work together with the MATLAB. The simulation model is shown in Fig.3. TABLE II reveals parameters of fundamental components. TABLE III gives the harmonic currents.

The use of FFT and FIR filters to obtain the fundamental frequency components are compared. The Xilinx ISE offers free library of IP that have been verified so that users can program directly. Introduction of model is as follows：

(1) Fast Fourier Transform

The FFT core computes an N-point forward DFT or inverse DFT (IDFT) where N can be 2^m. The input data are a vector of N complex values represented as bx-bit two's-complement numbers. The bx bits for each of the real and imaginary components of the data sample are bx=8~24. Similarly, the phase factors bw can be 8~24 bits wide. In this paper, the transfer function length is 64 and the input data width is 12 bit. The fundamental frequency components can be obtaind from the results of FFT. The FFT formulas are as follows：

TABLE IV Fundamental Power Factor of FIR

	V_1 (V)	I_1 (A)	S_1 (VA)	P_1 (W)	PF_1
Matlab	220	9.09	2000	1200	0.6
FPGA	219.6	9.08	1993.6	1197.9	0.601
Error(%)	0.200	0.110	0.320	0.179	-0.133

TABLE V Fundamental Power Factor of FFT

	V_1 (V)	I_1 (A)	S_1 (VA)	P_1 (W)	PF_1
Matlab	220	9.09	2000	1200	0.5998
FPGA	219.78	90.9	1997.80	1198.54	0.6001
Error(%)	0.100	0	0.110	0.122	-0.050

TABLE VI FPGA utilization summary of FIR

Logic Utilization	Used	Available	Utilization
Slice Flip Flops	12202	26624	45%
LUTs	8191	26624	30%
Slices	6701	13312	50%
IOBs	103	487	21%
MULT18×18	4	32	12%
Clk	1	8	12%
Global Timmig Constraints	Period		8.379(ns)
	Offset in		4.613(ns)
	Offset out		8.593(ns)

TABLE VII FPGA utilization summary of FFT

Logic Utilization	Used	Available	Utilization
Slice Flip Flops	11907	26624	44%
LUTs	11871	26624	44%
Slices	7735	13312	58%
IOBs	103	487	21%
MULT18×18	15	32	46%
Clk	1	8	12%
Global Timmig Constraints	Period		16.345(ns)
	Offset in		23.281(ns)
	Offset out		9.558(ns)

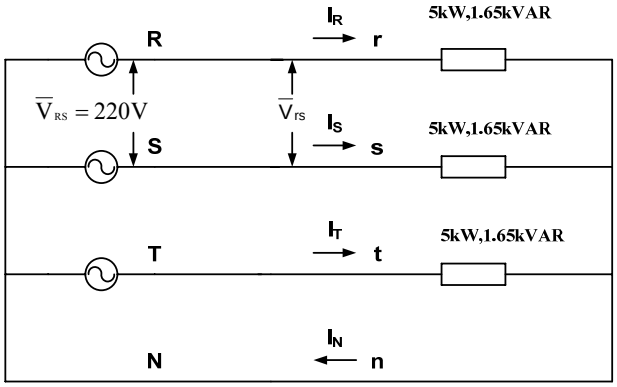

Fig. 4. Three-phase four-wire simulation system

TABLE VIII Load parameter of each phase

Voltage	f_1(Hz)	P_1(W)	Q_1(VAR)	Load	PF_1
220(V)	60	5000	1650	Inductive	0.9496

TABLE IX Three-phase load cases

Load category	Case 1	Case 2	Case 3	Case 4
$\overline{S}_{1U}$ (%)	0	0~100	0	0~100
$\overline{S}_{eN}$ (%)	0	0	0~100	100
Loading Conditions	balanced	unbalanced	balanced	unbalanced
	inductive	inductive	inductive	inductive
	without harmonics	without harmonics	with harmonics	with harmonics

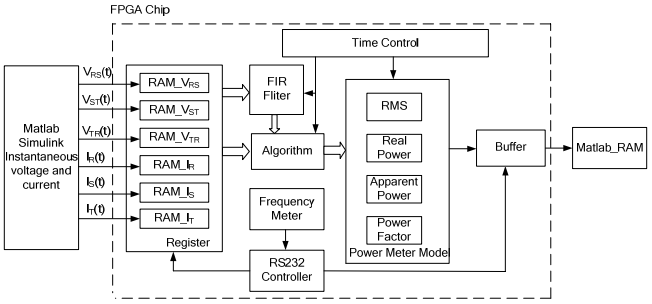

Fig. 5. Systematic structure diagram of calculation.

$$V_{rms}(n) = \frac{2}{N\sqrt{2}} * \sqrt{xk_{re}(n)^2 + xk_{im}(n)^2} \quad (42)$$

$$V_{\angle\theta}(n) = \tan^{-1}\frac{xk_{im}(n)}{xk_{re}(n)} \quad (43)$$

$V_{rms}(n)$: rms value of harmonic, n = 1,2...

$V_{\angle\theta}(n)$: angle of harmonic, n = 1,2..

$xk_{re}(n)$: real components of harmonic, n = 1,2..

$xk_{im}(n)$: imaginary components of harmonic, n = 1,2..

The detailed of FFT is given in Appendix.

(2) Distributed Arithmetic FIR Filter

The FIR core filters are used to strain harmonic components. The lengths and coefficients of FIR filters are calculated of Matlab. The filter coefficients are supplied to the filter compiler using a coefficient file with a coe extension.

An ASII text file with a single-line header that defines the radix of the number representation is used for the coefficient data, followed by the coefficient values themselves. For an N-tap filter, it is described as

radix=coefficient_radix;
coefdata=
a(0),
a(1),
a(2),
….
a(N-1);

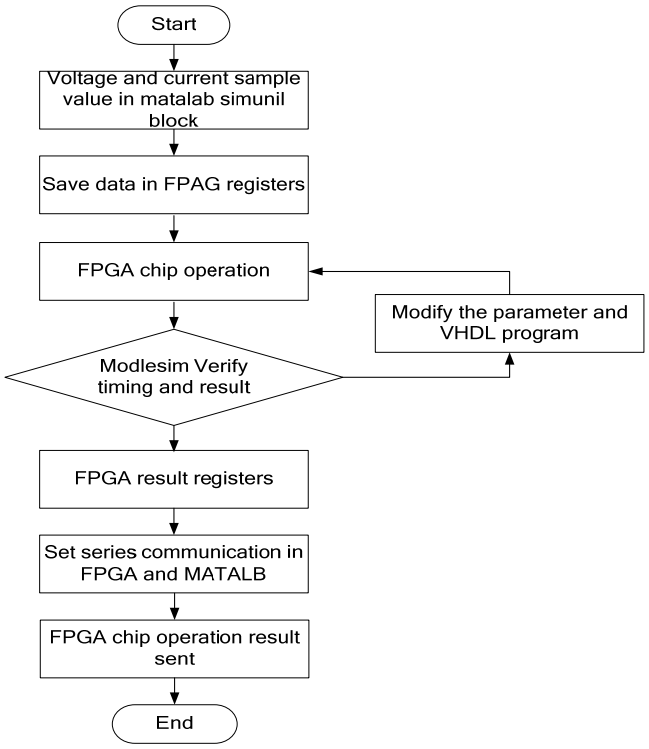

Fig. 6. The flowchart of FPGA design circuit.

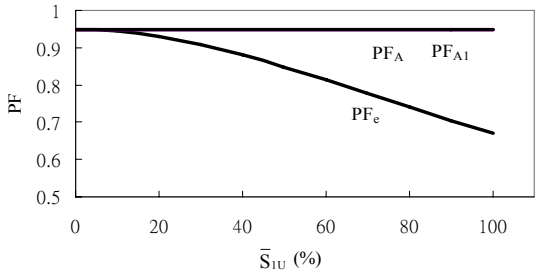

Fig. 7. PF vs $\bar{S}_{1U}$ (%) in Case 2

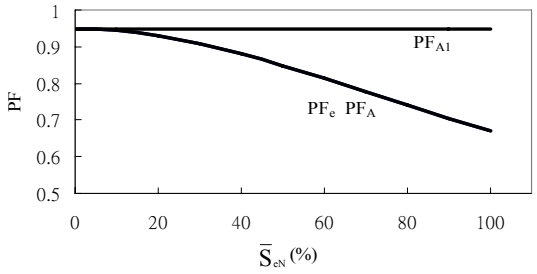

Fig. 8. PF vs $\bar{S}_{eN}$ (%) in Case 3.

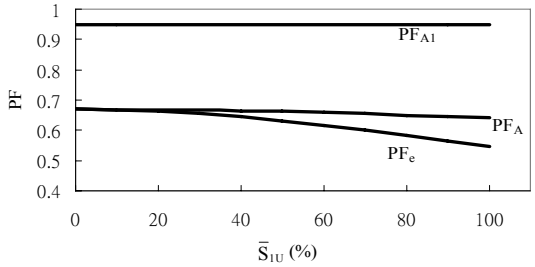

Fig. 9. PF vs $\bar{S}_{1U}$ (%) in Case 4.

(3) CORDIC core 3.0

The model features vector rotation (polar to rectangular), vector translation (rectangular to polar), trigonometric function, and square root calculation are used. Magnitude of FFT uses square root operation of CORDIC core 3.0 IP.

(4) Results

The computaton results are given in TABLE IV and V by using FIR filter and FFT, respectively. The method by using the FFT is more accurate. However, the errors by using the FIR filters are acceptable. The FPGA utilization conditions are given in TABLE VI and VII. It can be found that the approach by usin the FIR filters has a lower computation loading. The FIR filters are used for the following study in this paper.

5 Three-Phase System

The simulation block to generator the test data is developed by using the Simulink and Sim Power Systems, which work together with the MATLAB [20]. The simulation model is shown in Fig. 4. There are four given loading cases in investigating the power factor calculation, as shown in TABLE VIII and IX, based on the properties of fundamental powers and harmonic currents.

The systematic structure diagram of calculation using FPGA is given in Fig. 5. Fig. 6 reveals the flowchart of FPGA design circuit. The most important issue in designing the calculation IC is the choice of numerical data processing schemes. A floating-point arithmetic method has the advantage of a wide dynamic range, but its hardware realization is very complicated. A fixed-point arithmetic scheme is a more practical solution to most industrial applications with simple circuit realization. The proper numerical data scaling plays a significant role in synthesizing an integer controller. In this study, numerical variables and parameters must be transformed into approximate integers with finite word lengths.

TABLE X Utilization conditions of FPGA in calculating effective power factor

Logic Utilization	Used	Available	Utilization
Slice Flip Flops	3646	26624	13%
LUTs	3640	26624	13%
Slices	2771	13312	20%
IOBs	232	487	47%
MULT18×18	19	32	59%
Clk	1	8	12%
Global Timing Constraints	Period		13.421(ns)
	Offset in		4.899(ns)
	Offset out		8.896(ns)

TABLE XI Utilization conditions of FPGA in calculating arithmetic power factor

Logic Utilization	Used	Available	Utilization
Slice Flip Flops	2880	26624	10%
LUTs	2763	26624	10%
Slices	2143	13312	16%
IOBs	203	487	41%
MULT18×18	15	32	46%
Clk	1	8	12%
Global Timing Constraints	Period		9.873(ns)
	Offset in		4.899(ns)
	Offset out		7.241(ns)

TABLE XII Utilization conditions of FPGA in calculating fundamental power

Logic Utilization	Used	Available	Utilization
Slice Flip Flops	24902	26624	93%
LUTs	19371	26624	72%
Slices	13001	13312	97%
IOBs	203	487	41%
MULT18×18	18	32	56%
Clk	1	8	12%
Global Timing Constraints	Period		12.330(ns)
	Offset in		10.236(ns)
	Offset out		8.593(ns)

TABLE XIII Power factor values in Case 1

	PF_e	PF_A	PF_{A1}
Matlab	0.9496	0.9496	0.9496
FPGA	0.9504	0.9520	0.9498
Error(%)	-0.084	-0.253	-0.021

The test data are obtained as follows.

(1) The 220-V (line-to-line) symmetrical three-phase voltage source block is used.

(2) The three-phase loads are composed of series RLC load blocks and the harmonic current source blocks. The series RLC load blocks can be assigned the fundamental active and reactive powers. Then it is to use the Sim command to adjust unbalance level and harmonic level.

(3) The instantaneous line-to-line voltages and line currents of the three-phase cases can be obtained by the measurement blocks. The sampling rate is 3840 sample/second.

(4) Then the instantaneous voltages and current values are sent to calculate apparent powers and power factors. Because float-point calculations need large RAM capacity and long operation time, the instantaneous voltage and current values are mapped to integral values. The procedures are as follows:

(a) It is to normalize them to per-unit values. All instantaneous values are divided by the rms value. The rms value of the voltage is 220V and that of the fundamental current is 41.45A in case 1.

(b) Then all per-unit values are multiplied by 1000 to increase the effective bit number in FPGA.

(c) The calculation error by FPGA is defined as

$$\varepsilon(\%)=\frac{\text{given value(Matlab)-calculated value}(FPGA)}{\text{given value}(Matlab)}\times 100\% \tag{44}$$

6 Apparent Power and Power Factor Calculation Results

Figs. 7-9 show the trend of PF_e, PF_A, and PF_{A1} versus $\overline{S}_{1U}$ and $\overline{S}_{eN}$. The FPGA routing diagram is given in Fig. 10. Fig. 11. gives the timing simulation of the calculation IC. The utilization conditions of FPGA are given in TABLES X, XI, and XII. Some observations can be obtained.

(a) In Case 1, the three-phase system is balanced and without harmonic loads. The power factor values are given in TABLE XIII. So the values of three power factors are the same.

(b) In Case 2, the three-phase system is unbalanced but with harmonic loads. The distortion power is zero. Because PF_A and PF_{A1} do not drop with $\overline{S}_{1U}$, they do not reflect the unbalance degree. Only PF_e drops with of $\overline{S}_{1U}$, so that it can reflect the effect of unbalance degree. The analytical results reveal that $PF_e < PF_A = PF_{A1}$.

(c) Case 3 considers the effects of harmonic distortion. The analytical results reveal that since PF_{A1} only considers the fundamental components, the harmonic distortion is disregarded. Therefore, the values are equal to those in Case 1. The analytical results reveal that $PF_e=PF_A < PF_{A1}$. The higher the harmonic distortion is, the less PF_e and PF_A are.

(d) Case 4 simultaneously considers the effects of harmonic distortion and unbalance. Some power factor values are given in TABLE XIV. The analytical results reveal that $PF_e < PF_A < PF_{A1}$.

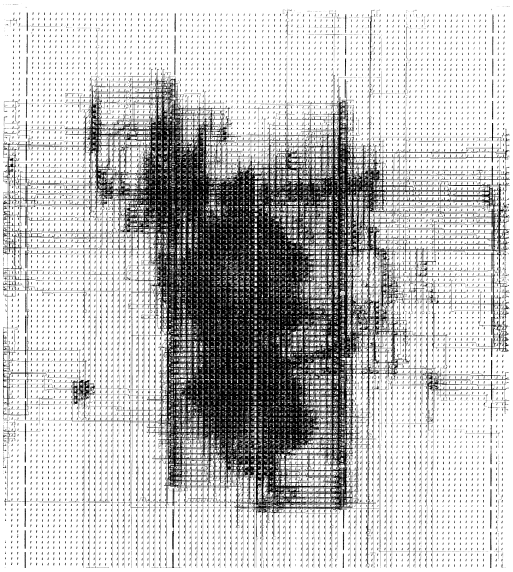

Fig. 10. FPGA routing diagram

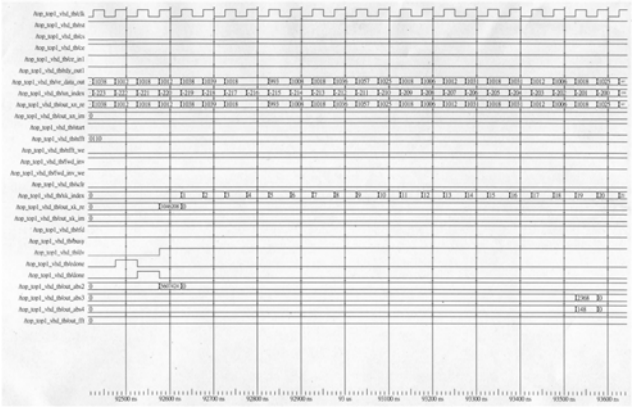

Fig. 11. Timing simulation of the calculation IC.

7 Conclusion

This study has presented an FPGA-based calculation IC for obtaining the apparent power and power factor values of three-phase power systems. The design scheme has advantages of concurrent operation, small hardware requirement, and easy and fast circuit modification. Adopting VHDL provides sufficient flexibility and speed to construct the design circuits by some IP cores. All modules were designed and integrated to others. The major benefit of the proposed approach is that it executes all logics continuously and simultaneously. The calculation of apparent powers and power factors are implemented in FPGA considering the effects of harmonic and unbalanced conditions. A lot of algorithms are written into IP on FPGA. The calculation results of power factors have the average error about 0.35%. In the FPGA chip utilization rates, the calculation procedures of fundamental power factor are the highest, and the calculation method of arithmetic the lowest. In calculating time of the procedures of the arithmetic factor is the fastest. The results reveal that the FPGA chip can be used to calculate the power factor values accurately.

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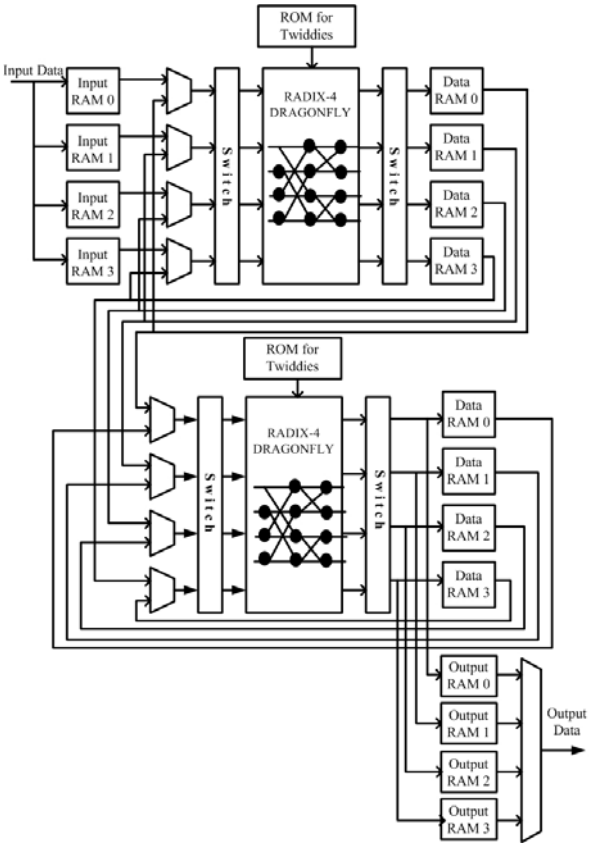

Fig. A1. Structure diagram of radix-4 FFT core.

Appendix: FFT core

The FFT core used in this paper is given in Fig. A1, where the radix-4 type is used. The Fast Fourier Transform (FFT) is a computationally efficient algorithm for deriving the Discrete Fourier Transform (DFT). The FFT core developed by Xilinx can compute an *N*-point forward DFT or inverse DFT (IDFT) where $N=2^m$, $m=4\sim14$. The FFT core applies the Cooley-Tukey decimation-in-time (DIT) algorithm to determine the DFT. It utilizes two radix-4 butterfly-processing engines, and offers continuous data processing using input memory, output memory, and intermediate memory banks. Figure 5 illustrates the structure of a radix-4 FFT. When using radix-4, the FFT consists of $\log_4(N)$ stages, with each stage including $N/4$ radix-4 butterflies. This core can simultaneously perform transform computations on the current data frame, load the input data for the next data frame, and unload the results of the previous frame of data. All memory is on-chip using either block RAM or distributed RAM. The radix-4 1024-point DIF method was adopted to process 2-channel data.

TABLE XIV Some power factor values in Case 4

$\overline{S}_{1U}$ (%)	$\overline{S}_{eN}$ (%)	PF_e			PF_A			PF_{A1}		
		Matlab	FPGA	ε(%)	Matlab	FPGA	ε(%)	Matlab	FPGA	ε(%)
0	100	0.6693	0.668	0.194	0.6693	0.6701	-0.120	0.9496	0.9498	-0.021
10	100	0.6676	0.667	0.090	0.6689	0.6694	-0.075	0.9496	0.9486	0.105
20	100	0.6626	0.662	0.091	0.6680	0.6696	-0.240	0.9496	0.9512	-0.168
30	100	0.6546	0.654	0.092	0.6664	0.6672	-0.120	0.9496	0.9502	-0.063
40	100	0.6439	0.643	0.140	0.6643	0.6657	-0.211	0.9496	0.9484	0.126
50	100	0.6308	0.630	0.127	0.6616	0.6626	-0.151	0.9496	0.9516	-0.211
60	100	0.6158	0.615	0.130	0.6584	0.6588	-0.061	0.9496	0.9499	-0.032
70	100	0.5995	0.599	0.083	0.6548	0.6561	-0.199	0.9496	0.9485	0.116
80	100	0.5821	0.581	0.189	0.6506	0.6516	-0.154	0.9496	0.9514	-0.190
90	100	0.5641	0.564	0.018	0.6460	0.6475	-0.232	0.9496	0.9500	-0.042
100	100	0.5459	0.545	0.165	0.6410	0.6411	-0.016	0.9496	0.9496	0.000
			Error(%)	0.120		Error(%)	-0.143		Error(%)	-0.098