

# High-SFDR and Multiplierless Direct Digital Frequency Synthesizer

**TZE-YUN SUNG**

Department of  
Microelectronics Engineering  
Chung Hua University  
Hsinchu City 300-12, Tawan  
bobsung@chu.edu.tw

**HSI-CHIN HSIN**

Department of Computer  
Science and Information  
Engineering  
National United University  
Miaoli 36003, Taiwan  
hsin@nuu.edu.tw

**LU-TING KO**

Department of Electrical  
Engineering  
Chung Hua University  
Hsinchu City 300-12, Tawan  
m09601049@chu.edu.tw

*Abstract:* - This paper presents a hybrid COordinate Rotation DIgital Computer (CORDIC) algorithm for designs and implementations of the direct digital frequency synthesizer (DDFS). The proposed multiplier-less architecture with small ROM ( $16 \times 4$ -bit) and pipelined data path provides a spurious free dynamic range (SFDR) of more than 84.4 dBc. A SoC (System on Chip) has been designed by  $0.18\mu\text{m}$  1P6M CMOS, and then emulated on the Xilinx FPGA. It is shown that the hybrid CORDIC-based architecture is suitable for VLSI implementations of the DDFS in terms of hardware cost, power consumption, and SFDR.

*Key-Words:* - DDFS, hybrid CORDIC, SoC, FPGA, SFDR.

## 1 Introduction

The direct digital frequency synthesizer (DDFS) plays a key role in many digital communication systems. Fig. 1 depicts the conventional DDFS, which consists mainly of phase accumulator, sine/cosine generator, digital-to-analog converter, and low-pass filter. The sine/cosine generator as the core of DDFS is usually implemented by using a ROM lookup table; with high spurious free dynamic ranges (SFDR) comes a large ROM lookup table [1]. In order to reduce the size of the lookup table, many techniques were proposed [1]-[4]. The quadrant compression technique can reduce the ROM size by 75% [2]. The Sunderland architecture is to split the ROM into two smaller ones [3], and its improved version known as the Nicholas architecture results in a higher ROM-compression ratio (32:1) [4]. In [5], the polynomial hyperfolding technique with high order polynomial approximation was used to design DDFS. In [6]-[10], the angle rotation algorithm was used to design quadrature direct digital frequency synthesizer/complex mixer (QDDSM).

COordinate Rotation DIgital Computer (CORDIC) is a well known arithmetic algorithm, which evaluates various elementary functions including sine and cosine functions by using simple adders and shifters only. Thus, CORDIC is suitable for the design of high-performance chips with VLSI

technologies. Recently, the CORDIC algorithm has received a lot of attention to the design of high-performance DDFS [11]-[14], especially for the modern digital communication systems.

In this paper, we propose a hybrid CORDIC algorithm for the VLSI implementation of DDFS. The remainder of this paper proceeds as follows. In section 2, the proposed hybrid CORDIC algorithm is presented. In section 3, the hardware implementation of DDFS is described. The performance analysis is given in section 4. Conclusion can be found in section 5

## 2 The Hybrid CORDIC Algorithm

In this section, the hybrid CORDIC algorithm is proposed, and based on which, a low-power and high-SFDR DDFS can be developed.

### 2.1 The modified scaling-free CORDIC algorithm

In order to reduce the number of CORDIC iterations, the input angle can be divided into encoded angles by using the modified Booth encoding (MBE) method [15]. Specifically, let  $\psi$  denote the input angle represented by

$$\psi = f(0)2^{-p} + f(1)2^{-(p+1)} + \dots + f(w-1)2^{-(w-1)} \quad (1)$$

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where  $f(i) \in \{0,1\}$ ,  $w$  is the word length of operands, and  $\left\lceil \frac{(w-2.585)}{3} \right\rceil = p \leq i \leq w-1$ . The MBE decomposition of  $\psi$  is as follows.

$$\psi = \sum_{i=p/2}^{(w-1)/2} \beta(i) \quad (2)$$

where the encoded angle:  $\beta(i) = \rho(i)2^{-i}$  with  $\rho(i) \in \{-2,-1,0,1,2\}$ . As  $\sin \beta(i)$  and  $\cos \beta(i)$  can be approximated by

$$\sin \beta(i) \cong \beta(i) = \rho(i)2^{-i} \quad (3)$$

$$\cos \beta(i) \cong 1 - \frac{\beta^2(i)}{2} = 1 - \rho^2(i)2^{-(2i+1)} \quad (4)$$

we have

$$\begin{bmatrix} x(i+1) \\ y(i+1) \end{bmatrix} = \begin{bmatrix} 1 - \rho^2(i)2^{-(2i+1)} & \rho(i)2^{-i} \\ -\rho(i)2^{-i} & 1 - \rho^2(i)2^{-(2i+1)} \end{bmatrix} \begin{bmatrix} x(i) \\ y(i) \end{bmatrix} \quad (5)$$

$$z(i+1) = z(i) - \rho(i)2^{-i} \quad (6)$$

Fig. 2 shows the proposed architecture for the modified scaling-free CORDIC arithmetic, in which, eight shifters, two CSAs, two CLAs, two latches, and four MUXs are used; the shifters and MUXs are to determine  $\rho(i)$ .

### 2.2 The modified scaling-free radix-8 CORDIC Algorithm

By using the modified angle recoding method [15]-[16], the input angle  $\psi$  can be divided as follows.

$$\psi = \sum_{i=p}^{w-1} \phi(i) \tan^{-1} 2^{-i} \quad (7)$$

where  $\phi(i) \in \{0,1\}$ , and  $w$  is the word length. The CORDIC iteration is therefore represented as

$$\begin{bmatrix} x(i+1) \\ y(i+1) \end{bmatrix} = \begin{bmatrix} 1 & \phi(i)2^{-i} \\ -\phi(i)2^{-i} & 1 \end{bmatrix} \begin{bmatrix} x(i) \\ y(i) \end{bmatrix} \quad (8)$$

$$z(i+1) = z(i) - \phi(i) \tan^{-1} 2^{-i} \quad (9)$$

Let  $i = 3n - c$ ;  $c \in \{0,1,2\}$ . By using the Taylor series expansion, the absolute difference between  $\tan^{-1}(2^{-(3n-c)})$  and  $2^c \tan^{-1}(2^{-3n})$  is given by

$$\zeta = \left| \tan^{-1} 2^{-(3n-c)} - 2^c \tan^{-1} 2^{-3n} \right| = \left| \frac{1}{3} \cdot 2^{-3(3n-c)} + \Lambda \right| \quad (10)$$

where  $\Lambda$  is the remaining terms of the difference between  $\tan^{-1}(2^{-(3n-c)})$  and  $2^c \tan^{-1}(2^{-3n})$ . Thus, we have

$$\zeta \cong \frac{2^{-3(3n-c)}}{3} = \frac{2^{-3i}}{3} \quad (11)$$

For  $w$ -bit operands,  $\zeta$  can be ignored in the following sense

$$\zeta \leq 2^{-w} \quad (12)$$

Based on equations (11) and (12), we have

$$\frac{2^{-3i}}{3} \leq 2^{-w} \quad (13)$$

$$3i + \log_2 3 \geq w \quad (14)$$

$$i \geq \frac{w - \log_2 3}{3} = \left\lceil \frac{w - \log_2 3}{3} \right\rceil \cong \frac{w}{3} \quad (15)$$

As a result, when  $i > \frac{w}{3}$ , three consecutive terms of equation (7) can be integrated into a single term as follows:

$$\begin{aligned} & \phi(3n-2) \tan^{-1}(2^{-(3n-2)}) + \phi(3n-1) \tan^{-1}(2^{-(3n-1)}) \\ & + \phi(3n) \tan^{-1}(2^{-(3n)}) \\ & = (\phi(3n-2) \cdot 2^2 + \phi(3n-1) \cdot 2^1 + \phi(3n) \cdot 2^0) \tan^{-1}(2^{-3n}) \\ & = \varphi(n) \tan^{-1}(2^{-3n}) \end{aligned} \quad (16)$$

where  $\phi(\cdot) \in \{0,1\}$ , and therefore  $\varphi(n) \in \{0,1,2,\dots,7\}$ . It follows that the resulting radix-8 CORDIC algorithm is represented as

$$\begin{bmatrix} x(i+1) \\ y(i+1) \end{bmatrix} = K_8(i) \begin{bmatrix} 1 & -\varphi(i) \cdot 2^{-3i} \\ \varphi(i) \cdot 2^{-3i} & 1 \end{bmatrix} \begin{bmatrix} x(i) \\ y(i) \end{bmatrix} \quad (17)$$

$$z(i+1) = z(i) - \varphi(i) \tan^{-1} 2^{-3i} \quad (18)$$

$$K_8(i) = (1 + \varphi^2(i)2^{-6i})^{1/2} \quad (19)$$

The scaling factor  $K_8$  is given by

$$K_8 = \prod_{i=p}^{i=\lceil w/3 \rceil - 1} K_8(i) \quad (20)$$

It can be shown that the scaling factor turns out to be equal to 1 when the input angle is less than  $2^{-w/2}$ , and moreover, if the input angle is less than  $2^{-w/3}$ , equation (18) can be rewritten as [19]

$$z(i+1) = z(i) - \varphi(i)2^{-3i} \quad (21)$$

Fig. 3 depicts the proposed architecture for the modified scaling-free radix-8 CORDIC arithmetic. In which, six shifters, two CSAs, two CLAs, and two latches are used; the shifters and switches are to determine the radices for computations. Note that the number of processors is reduced, and system throughput is increased at the cost of hardware complexity.

### 2.3 The proposed hybrid CORDIC Algorithm

The input angle  $\Omega$  can be decomposed into a higher-angle  $\Omega_H$  and a lower-angle  $\Omega_L$  represented as

$$\Omega = \Omega_H + \Omega_L = \sum_{i=0}^{\lceil u/2 \rceil - 1} \rho(i) 2^{-2i} + \sum_{i=\lceil u/2 \rceil}^{\lceil u/2 \rceil + \lceil (w-u)/3 \rceil - 1} \varphi(i) 2^{u-1+3(i-\lceil w/4 \rceil)} \quad (22)$$

where  $w$  is the word length with the first  $u$  bits being the most significant bits;  $\Omega_H$  and  $\Omega_L$  are computed by using the modified scaling-free CORDIC algorithm and the modified scaling-free radix-8 CORDIC algorithm, respectively. For computation efficiency, the determination of  $u$  is as follows: 1)  $u$  must be an odd number to satisfy the MBE method, and 2)  $u \geq \frac{w}{2}$  under the scaling-free constraint. Thus, we have

$$u = \begin{cases} 2n+1, & \text{if } w = 4n+0 \\ 2n+1, & \text{if } w = 4n+1 \\ 2n+1, & \text{if } w = 4n+2 \\ 2n+3, & \text{if } w = 4n+3 \end{cases} \quad (23)$$

Based on the above equation, the minimum iteration number of the proposed hybrid CORDIC algorithm can be obtained as shown in Fig. 4. The computations of  $x(i)$  and  $y(i)$  are therefore as follows.

For  $\frac{p}{2} \leq i < \left\lceil \frac{u}{2} \right\rceil$ ,

$$x(i+1) = x(i) - \rho^2(i) 2^{-(4i+1)} x(i) - \rho(i) 2^{-2i} y(i) \quad (24)$$

$$y(i+1) = y(i) - \rho^2(i) 2^{-(4i+1)} x(i) + \rho(i) 2^{-2i} y(i) \quad (25)$$

For  $\left\lceil \frac{u}{2} \right\rceil \leq i < \left\lceil \frac{w}{4} \right\rceil + \left\lceil \frac{w-u}{3} \right\rceil$ ,

$$x(i+1) = x(i) - \varphi(i) 2^{u-1+3(i-\lceil w/4 \rceil+1)} y(i) \quad (26)$$

$$y(i+1) = y(i) + \varphi(i) 2^{u-1+3(i-\lceil w/4 \rceil+1)} x(i) \quad (27)$$

### 3 Hardware Implementation of the Proposed DDFS

In this section, the DDFS implemented by using the hybrid CORDIC algorithm is presented. Fig. 5 shows the 16-bit DDFS architecture consisting mainly of phase accumulator, phase calculator, and sine/cosine generator, which is different from the conventional architecture. It is noted that the accumulated error in the sine/cosine generator is to be corrected by using the  $4 \times 16$ -bit correction table. Take into account DAC technology, hardware cost and practical applications, the word length of the propose DDFS is set to 16-bit.

The hybrid CORDIC-based sine/cosine generator with recursively accumulated angle  $\mathcal{G}_m$  is given by

$$\begin{bmatrix} x(i+1) \\ y(i+1) \end{bmatrix} = \begin{bmatrix} \cos \mathcal{G}_m & -\sin \mathcal{G}_m \\ \sin \mathcal{G}_m & \cos \mathcal{G}_m \end{bmatrix} \begin{bmatrix} x(i) \\ y(i) \end{bmatrix} \quad (28)$$

where  $\mathcal{G}_m = \Delta_{acc} \frac{2\pi}{2^{16}}$ , and  $\Delta_{acc}$  is an integer number. (29)

For convergence, the input angle of the scaling-free CORDIC algorithm is restricted as follows:

$$\mathcal{G}_m < \sum_{i=4}^{w-1} 2^{-i} \cong \frac{1}{8} \quad (30)$$

From the above two equations, we have

$$\Delta_{acc} = \frac{2^{16}}{2\pi} \cdot \mathcal{G}_m < 1304 \quad (31)$$

The architecture for the sine/cosine generator is shown in Fig. 5. In which three modified scaling-free CORDIC arithmetic units (MCORDIC-Type A) and two modified scaling-free radix-8 CORDIC arithmetic units (MCORDIC-Type B) are used.

The chip is synthesized by the TSMC 0.18  $\mu\text{m}$  1P6M CMOS cell libraries [17]. The layout view of the proposed DDFS is shown in Fig. 6. The core size obtained by the Synopsys<sup>®</sup> design analyzer is  $612 \times 612 \mu\text{m}^2$ . The power consumption obtained by the PrimePower<sup>®</sup> is 6.05 mW with a clock rate of 100MHz at 1.8V. The tuning latency is 8 clock cycles. All the control signals are internally generated on-chip. The chip provides both high throughput and low gate count.

### 4 Performance Analysis of the Proposed DDFS

The number of correcting points versus the SFDRs with different  $(F_s / F_o)$ 's in the proposed DDFS is shown in Fig. 7. Due to trade-off between hardware cost and system performance, the correcting circuit with 16 points is implemented in the proposed DDFS. In case of 16-bit word length, as shown in Fig. 8, the high-frequency SFDR is 169.7 dBc, respectively. The mid-frequency SFDR of sine and cosine is 122 dBc, as shown in Fig. 9, respectively. The low-frequency SFDR of sine and cosine is 85.06 dBc, as shown in Fig. 10, respectively. As a result, the SFDR is above 85 dBc. Table 1 shows various comparisons of the proposed DDFS with other methods in [11] and [13]. As one can see, the proposed DDFS is superior in terms of SFDR, hardware cost, and power consumption.

### 5 Conclusion

The hybrid CORDIC-based multiplier-less DDFS architecture with small ROM and pipelined data path has been implemented. A SoC designed by 1P6M CMOS has been emulated on Xilinx

XC2V6000 FPGA. For 16-bit DDFS, the SFDR of sine and cosine using the proposed architecture are more than 85.06 dBc. Simulation results show that the hybrid CORDIC-based approach is superior to the traditional approach to the design and implementation of DDFS, in terms of SFDR, power consumption, and hardware cost. The 16-bit DDFS is a reusable IP, which can be implemented in various processes with efficient uses of hardware resources for trade-offs of performance, area, and power consumption.

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Table I Comparison with previous works

CORDIC Based DDFS	Madiseti [11] 1999		Swartzlander [13] 2006		This work [Sung, Hsin & Ko]
Process ( $\mu m$ )	1.0		0.13		0.18
Core Area ( $mm^2$ )	0.306	0.176	0.35	0.15	0.375
Maximum Sampling Rate (MHz)	80.4	85.7	1018	1052	100
Power Consumption (mw)	40.602	20.8251	350	143	6.056
Power Consumption (mw/MHz)	0.505	0.243	0.343	0.134	0.06
SFDR ( $dB_c$ )	81	62.1	90	60	85.06
Output Resolution (bits)	16	16	16	11	16
Tuning Latency (clock cycles)	16	16	--	--	8

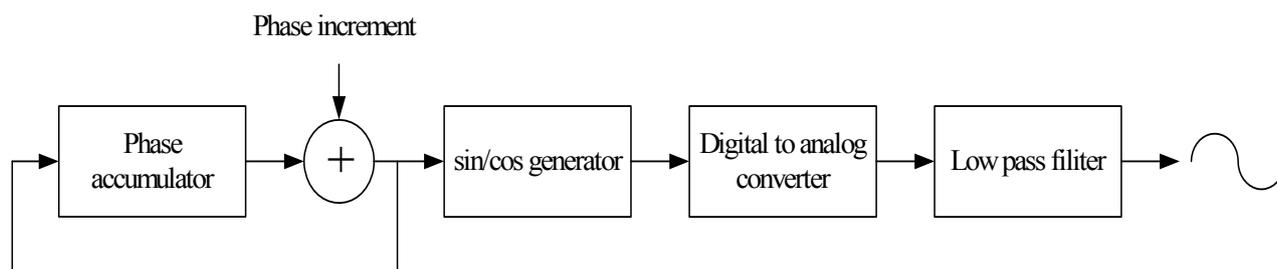


Fig. 1 The conventional DDFS architecture

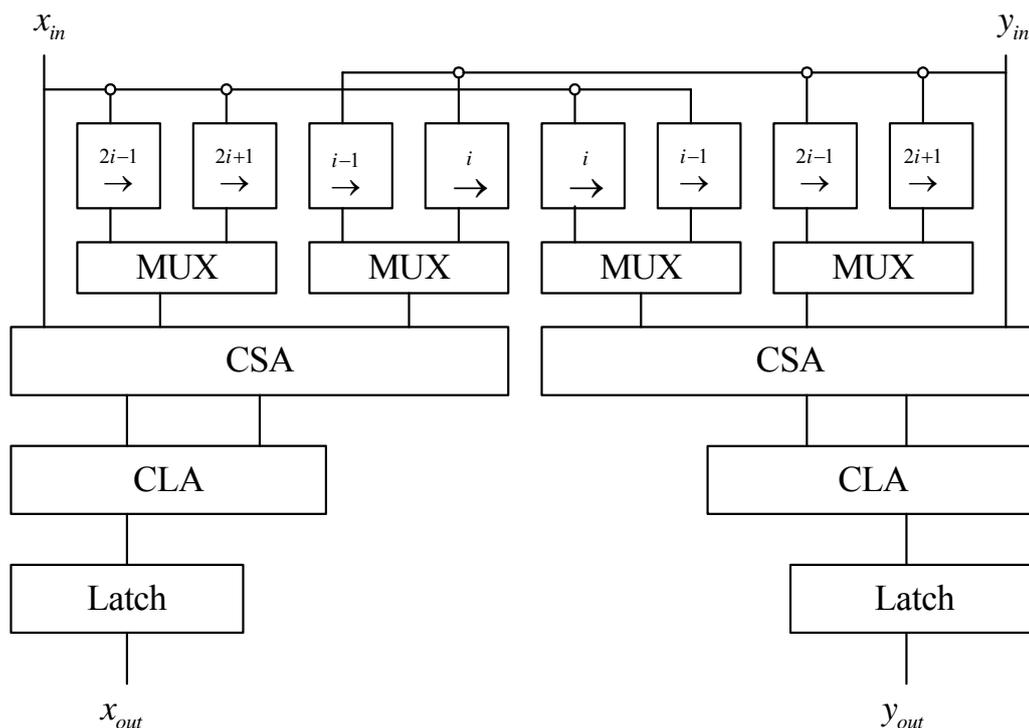


Fig. 2 The proposed architecture of modified scaling-free CORDIC arithmetic for computing  $\theta_H$  (MCORDIC-Type A)

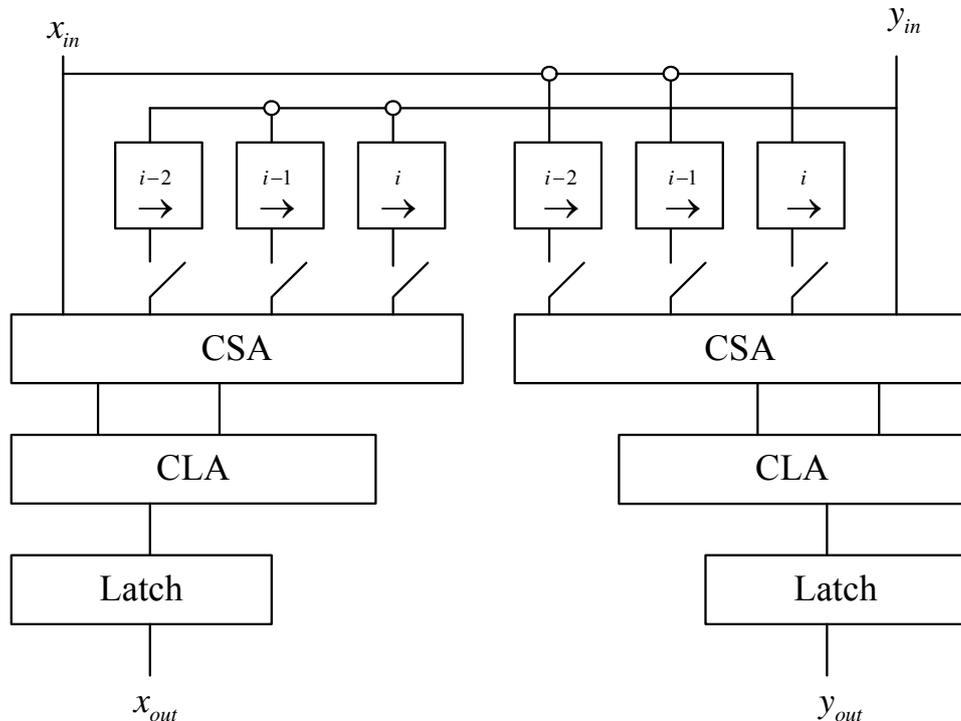


Fig. 3 The architecture of modified scaling-free radix-8 CORDIC arithmetic for computing  $\theta_L$  (MCORDIC-Type B)



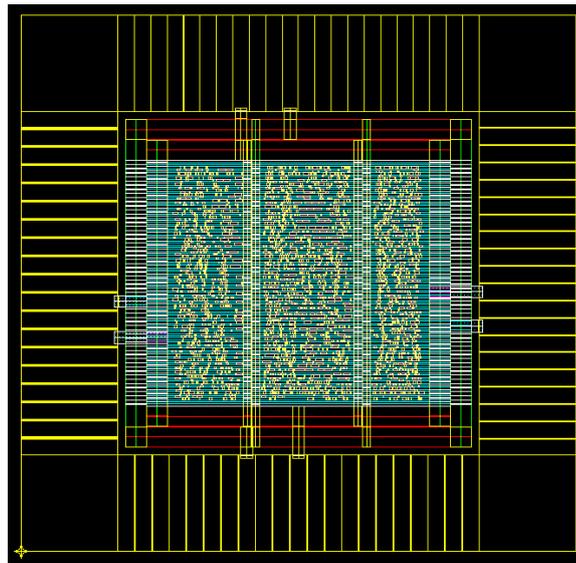


Fig. 6 The layout view of the proposed DDFS

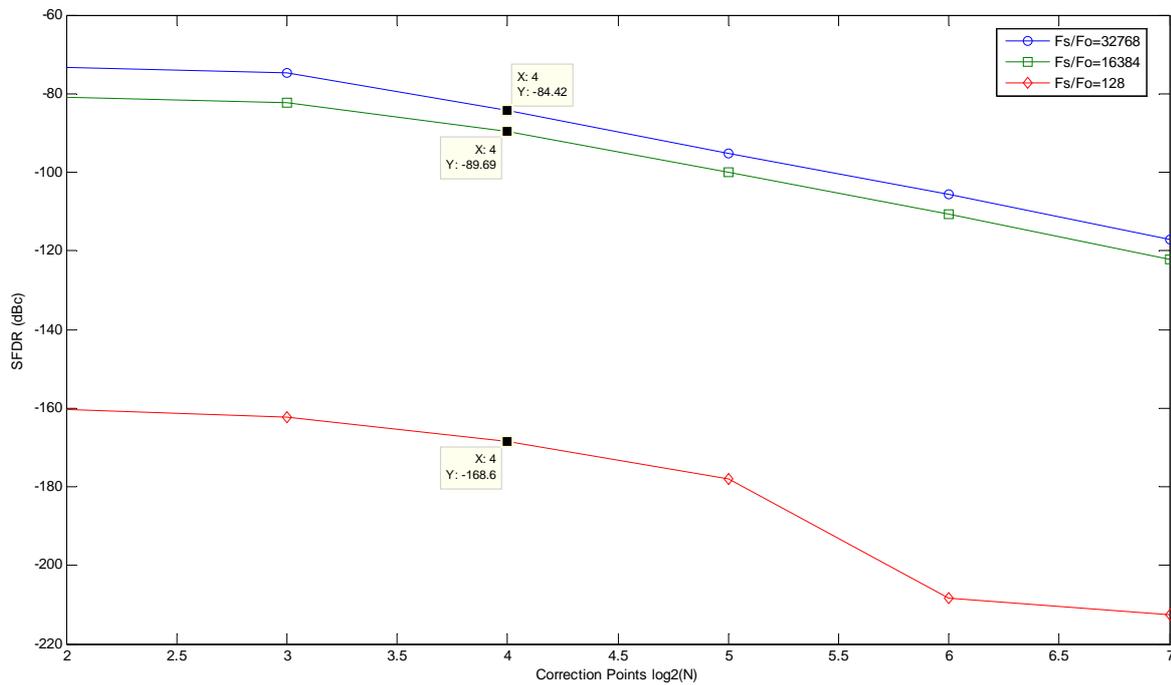


Fig. 7 Plot of the number of correcting points versus SFDRs with different  $(F_s / F_o)$ 's

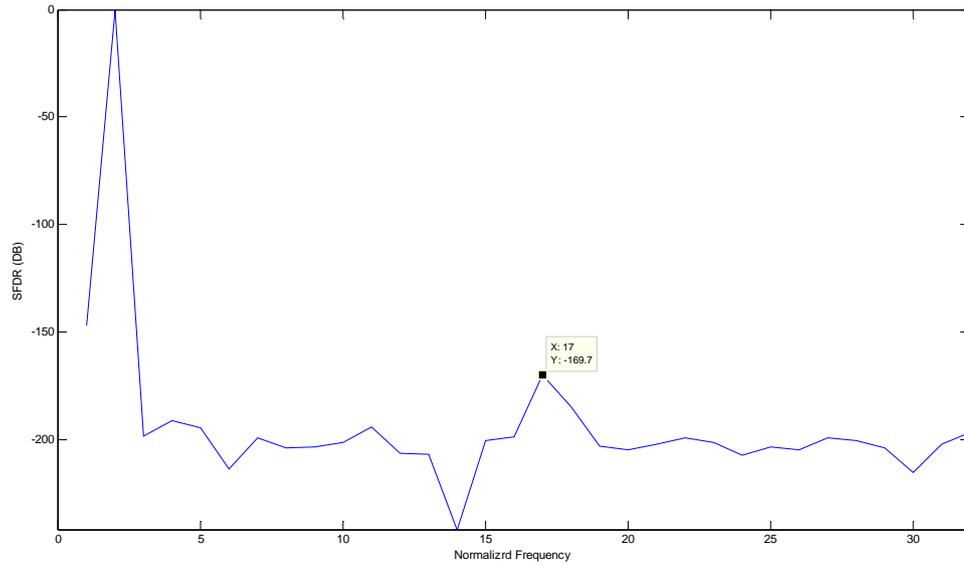


Fig.8 High-frequency SFDR using the proposed 16-bit DDFS (169.7 dBc)

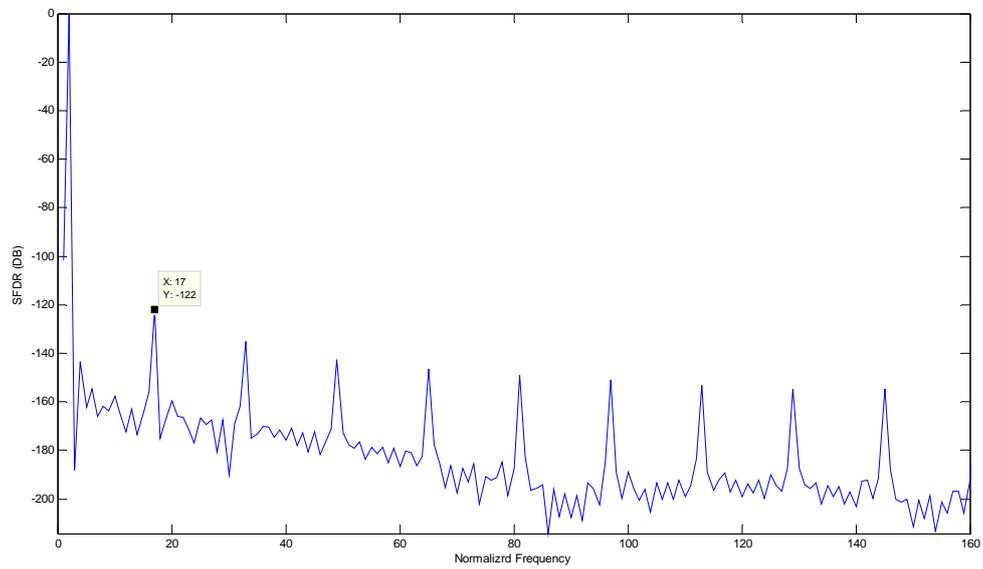


Fig.9 Mid-frequency SFDR using the proposed 16-bit DDFS (122 dBc)

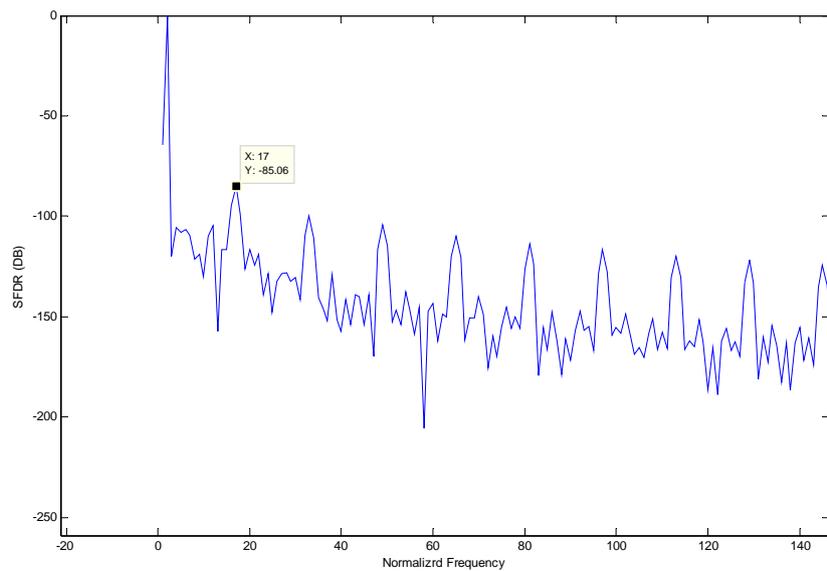


Fig.10 Low-frequency SFDR using the proposed 16-bit DDS (85.06 dBc)