Improved Design of Three-Level NPC Inverters in Comparison to Two-Level Inverters

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Abstract : -As voltage source 3-level NPC inverters are suitable for AC drives in average voltage and FACT applications in distribution systems, this report introduces optimized design of 3-level NPC inverter by decreasing inverter losses and costs. At first optimization parameters and application functions of losses are introduced[1], then by using MATLAM6.5 program and IGBT, diodes, switching frequency and load current typical input parameters [1] are considered then by SPWM switching algorithm in program, optimized RG_{on} , RG_{off} and gate voltage for 3-level NPC inverters are calculated for minimizing switching and conduction losses of inverter among all amounts of calculated RG_{on} , RG_{off} and gate voltage in comparison to optimized design of 2-level inverters[1]. Then results of NPC optimization are applied for simulation of improved NPC, using SVM switching algorithm as the best method of switching and results are presented.

Key words: -Design, IGBT inverter, NPC, SPWM, SVM, loss model, optimization

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1 Introduction

Inverters change DC voltage to AC voltage and using them in power systems, improves power system stability, power quality, transmission power quality, decreasing load of network, reactive power control, decreasing oscillations of network in SVC lights and harmonic filtering. Also inverter is used as supply of AC drives.

It's beneficial in many power electronic applications to increase the switching frequency in order to minimize the size of passive devices but it declines the switching and total efficiency; however inverter switching losses are functions of current and voltage slopes during switch on and off of IGBTs and diodes and (di/dt ,dv/dt) are functions of RG_{ON} and RG_{OFF} in gate circuit that can be optimized.

In many design methods gate voltage is considered constant but it can be selected in a range and it can be used as another design parameter. Therefore optimization design of a 3-phase NPC inverter can present parameters of RG_{ON} and RG_{OFF} and gate voltage for a constant load current and switching frequency.

An optimized design for decreasing switching and conduction losses of 2-level inverters has been already performed by SABER simulator in [1].

In this report finding optimized parameters is performed by MATLAB among all calculated amounts of RG_{ON} and RG_{OFF} and gate voltage by using step size 1 between them and supposing load current as a defined input parameter for a 3-level NPC inverter that has a discrete modulation function or duty cycle function [2] as a new idea. Then the comparison is presented in tables for 2-level and 3-level inverters.

In this report by using parameters of a typical IGBT, diodes, switching frequency and domain of load current as inputs and SPWM method as switching method, RG_{ON} and RG_{OFF} and gate voltage parameters for 3-level NPC inverters are

presented so that inverter switching and conduction losses are minimized and complete model of 3-level NPC inverter without snubber circuit which includes modulation function, switching losses, and conduction losses is improved and used for calculating optimized snubber parameters. Then results are applied for simulation of 3-level NPC inverter, using SVM switching as the best switching method for fast switching and high efficiency but SVM is not subject of this report[7].

2 On and off times of IGBT and Diodes

One of the most important parts of loss calculation is determining on and off time of IGBT.s and diodes that are directly related to switching frequency and modulation function used for inverter (SPWM). Benefit of sine modulation method is that has not third and lower harmonics but switching frequency in this method is increased [1].
Modulation functions of 3-level NPC and 2-level inverters are defined as equations (1) [2] and (2) [1].

$$\begin{aligned}
&\delta_{a1} = m\cos(\omega t) && \omega t \in \left[0,\frac{\pi}{2}\right],\left[\frac{3\pi}{2},2\pi\right] \\
&\delta_{a1} = 0 && \omega t \in \left[\frac{\pi}{2},\frac{3\pi}{2}\right] \\
&\delta_{a2} = 1 + m\cos(\omega t) && \omega t \in \left[\frac{\pi}{2},\frac{3\pi}{2}\right] \\
&\delta_{a2} = 1 && \omega t \in \left[0,\frac{\pi}{2}\right],\left[\frac{3\pi}{2},2\pi\right]
\end{aligned}$$

$a1, a2$ *are indices related to a* half *leg*.

(1)

$$\delta = \frac{1}{2} + \frac{1}{\sqrt{3}} m\left(\sin(\omega t) + \frac{1}{6}\sin(\beta\omega t)\right) \quad (2)$$

Where

m=modulation index
ω = angular frequency of fundumental

3 Switching Losses in an Inverter

The most important part in optimized design of an inverter is inverter losses modeling. Power losses in inverter are divided to 1- conduction losses 2- switching losses that are discussed below.

4 Conduction Losses

Conduction loss (p_{con}) in IGBT or diode is in equation (3) [1].

$$Pcon, x = \frac{1}{T}\int_0^T V_{on}(t) * i_L(t) dt \quad (3)$$

$V_{on}(t)$ is voltage drop on IGBT and can be modeled by a dynamic resistance *ro* with constant voltage drop[1].

$$Von(t) = V_0 + ro * i_L(t)^{Bcon} \quad (4)$$

Dynamic resistance *ro* for transistor is function of gate voltage source ($V_G{}^+$). Bias voltage V_0 is nearly constant. Resistance $r_{o,T}$ is defined as (5) [1].

$$r_{o,T}(V_G{}^+) = \frac{1}{1 + \alpha(V_G{}^+ - V_{G0})} * R_{OT} \quad (5)$$

ro for diode is constant.
Then equation (3) for transistor and diode is:

$$P_{conT} = \frac{1}{T}\int_0^T [V_{0,T} + \frac{R_{OT}}{1+\alpha(V_G^+ - V_{G0})} * i_L(t)^{BconT}] \cdot i_L(t) \cdot dt \quad (6)$$

$$P_{con,D} = \frac{1}{T}\int_0^T [V_{0,D} + r_{o,D} * i_L(t)^{Bcon,D}] \cdot i_L(t) \cdot dt \quad (7)$$

5 Switching Losses in an Inverter

The total switching losses $E_{sw,total}$ for an inverter are given by (8) [1]:

$$E_{sw,total} = E_{T,sw(on)} + E_{T,sw(off)} + E_{D,sw(off)} \quad (8)$$

$E_{T,SW(on)}$ = turn-on switching losses
$E_{T.SW(off)}$ = turn-off switching losses
$E_{D,SW(off)}$ = turn-off diode losses

6 Turn-on IGBT Switching Losses

The turn-on losses can be expressed as (9) [1]:

$$E_{T,sw}(on) = \frac{1}{2} \cdot (V_{dc} - 2 \cdot L_{st} (\frac{di}{dt})_{on}) \cdot \frac{I_P^{\,2}}{(\frac{di}{dt})_{on}} - \frac{1}{2} \cdot I_L \cdot \frac{V_{dc}^{\,2}}{(\frac{dv}{dt})_{on}} \quad (9)$$

L_{st}= stray-inductances in the inverter
I_L= Load current
I_P= allowed peak current
$(\frac{di}{dt})_{on}$ = *current gradient during turn on*
$(\frac{dv}{dt})_{on}$ = *voltage gradient during turn on*

The relationship between the turn-on gate resistor RG_{on} and $(\frac{di}{dt})_{on}$ is (10) [1]:

$$(\frac{di}{dt})_{on} = g_m \cdot \frac{V_G^{\,+} - \frac{1}{2} \cdot \frac{I_P}{g_m} - V_{GE}(th)}{C_{ies1} \cdot RG_{on}} \quad (10)$$

R_{Gon}= turn-on gate-resistor
g_m= transcunductance of IGBT
C_{ies1} = the input capacitance at high $V_{CE\text{-value}}$
$V_{GE(th)}$ = threshold voltage of IGBT
V_{G+} = the positive gate-drive supply

$$(\frac{dv}{dt})_{on} = -\frac{V_G^{\,+} - V_{GE}(th) - \frac{I_L}{g_m}}{C_{GC1} \cdot RG_{on}} \quad (11)$$

C_{GC1}= the gate-collector capacitor at high $V_{CE\text{-value}}$ [1]

7 Turn-off IGBT Switching Losses

The turn-off losses in the IGBT can be expressed as (12) [1]:

$$E_{T,sw}(off) = \frac{1}{2} \cdot \frac{V_{dc}^{\,2}}{(\frac{dv}{dt})_{off}} \cdot I_L - \frac{1}{2} \cdot (V_{dc} - 2 \cdot L_{st} \cdot (\frac{di}{dt})_{off}) \cdot \frac{I_L^{\,2}}{(\frac{di}{dt})_{off}} + \frac{1}{2} \cdot k_t \cdot V_{dc} \cdot I_L \cdot t_{i,tail} \quad (12)$$

$(\frac{dv}{dt})_{off}$ = voltage gradient during turn-off
$(\frac{di}{dt})_{off}$ = current gradient during turn-off
K_t = tail current factor in IGBT
$t_{i,tail}$ = duration of tail current for IGBT

and current gradient during turn-off is as (13) [1]:

$$\left(\frac{di}{dt}\right)_{off} = -\frac{V_p - V_{DC}}{2 \bullet L_{st}} \quad (13)$$

V_P= allowable peak voltage during turn-off

The turn-off gate resistor $R_{G,off}$ is calculated by (14) [1]:

$$R_{Goff} = g_m \frac{V_{G-} - V_{GE(th)} - \frac{1}{2} \bullet \frac{I_L}{g_m}}{C_{ies1} \bullet \left(\frac{di}{dt}\right)_{off}} \quad (14)$$

R_{Goff}= turn-off gate resistor
V_{G-}= the negative supply for the gate-drive

The voltage gradient $(\frac{dv}{dt})_{off}$ can be calculated by (15) [1]:

$$\left(\frac{dv}{dt}\right)_{off} = \frac{V_{GE\ (th)} + \frac{I_L}{g_m} - V_{G-}}{C_{GC\ 1} \bullet R_{Goff}} \quad (15)$$

8 Turn-off Diode Switching Losses

During turn-on of the IGBT, the free-wheeling diode also has turn-off losses, and they can be calculated as (16) [1]:

$$E_{D,SW(off)} = \frac{1}{2} \bullet \left[V_{DC} + 2 \bullet L_{st} \bullet \left(\frac{di}{dt}\right)_{diode} \right] \bullet \frac{I_{RM}^2}{\left(\frac{di}{dt}\right)_{diode}} \quad (16)$$

$\left(\frac{di}{dt}\right)_{diode}$ = current gradient during turn-off controlled by the diode

I_{RM} = reverse recovery peak current and is calculated as (17) [1]:

$$I_{RM} = \left(\frac{di}{dt}\right)_{on} (\tau - \tau_{rr}) \left[1 - e^{\frac{-T_1}{\tau}} \right] \quad (17)$$

τ_{rr} = reverse recovery time constant

τ = charge carrier life time

T_1= time to turn-off the diode and is calculated as (18) [1]:

$$T_1 = \frac{I_L + I_{RM}}{\left(\frac{di}{dt}\right)_{on}} \quad (18)$$

9 Switching Losses Calculation

In ac machines as loads, the current will be lagging the modulated voltage. This will also make influence on the calculation ratio between the diode and IGBT transistor [1].

The conduction losses are as (19) [1]:

$$P_{con,x} = \frac{1}{T_f} \int_0^{T_f} V_{on}(t).i_L(t)dt \quad (19)$$

x=T for transistor and D for diode

$T_f = \frac{1}{fs}$

f_s =fundamental frequency

V_{on} (t) =on-state voltage drop

That (19) can be rewritten approximately as (20) [1]:

$$P_{con,x} = \frac{1}{T_f} \int_0^{T_f} (V_{0,x} + r_{0,x}(t).i_L(t)^{Bcon,x}).i_L(t).dt \quad (20)$$

Where

$V_{0,x}$=bias voltage for device x

$B_{con,x}$=curve fitted constant for device x

$r_{0,x}$ =dynamic resistance for device x that for diode is constant and can be calculated as (21) for transistor [1]:

$$r_{0,T}(V_{G+}) = \frac{1}{1 + \alpha(V_{G+} - V_{G0})} \times R_{0T} \quad (21)$$

Where

V_{G0} =minimum gate voltage from which (21) is valid (>3V)

R_{0T}=base resistor at minimum gate voltage

α = degrading coefficient of R_{0T}

The total loss for 2-level inverter can be expressed six times the losses in one leg as (22) [1]:

$$P_{totinv} = 6 \times f_{sw} \sum_{t=n.T_{sw}}^{n.T_{sw}+\frac{f_{sw}}{2f_s}.T_{sw}-T_{sw}} (E_{T,sw}(on).i_L(t) + E_{T,sw}(off).i_L(t) + E_{D,sw}(off).i_L(t) + PconT\ (\delta_n T_{sw}) + PconD\ (T_{sw} - \delta_n T_{sw}))$$

(22)

Where

$$P_{conT}(\delta_n T_{sw}) = \int_{\alpha_n - \frac{\delta_n}{2fsw}}^{\alpha_n + \frac{\delta_n}{2fsw}} \left(V_{0,T} + r_{0,T} \times i_L(t)^{B_{ConT}}\right) i_L(t) dt$$

$$P_{conD}(T_{sw} - \delta_n T_{sw}) = \int_{\alpha_n - \frac{\delta_n}{2fsw}}^{\alpha_{n+1} + \frac{\delta_{n+1}}{2fsw}} \left(V_{0,T} + r_{0,T} \times i_L(t)^{B_{ConD}}\right) i_L(t) dt$$

and

δ_n =duty cycle or conduction time at pulse n

α_n =time to the center of pulse n

n= number of pulse corresponding to the phase angle Φ

f_{sw}= switching frequency

$\frac{f_{sw}}{f_s}$ = number of switching in a fundamental

The total loss for 3-level NPC inverter can be presented twelve times the losses in half leg including two transistors a1, a2 and two diodes a1, a2 and one clamping diode as (23):

$$P_{totinv} = 12 \times f_{sw} \sum_{t=n.T_{sw}}^{n.T_{sw}+\frac{f_{sw}}{2f_s}.T_{sw}-T_{sw}} (E_{T,sw}(on).i_L(t) + E_{T,sw}(off).i_L(t) + E_{D,sw}(off).i_L(t) + PconT(\delta_{a1} T_{sw}) + PconD(T_{sw} - \delta_{a2} T_{sw}) + PconT(\delta_{a2} T_{sw}) + 2 \times PconD(T_{sw} - \delta_{a1} T_{sw}) + PconD(\delta_{a2} T_{sw}))$$

(23)

10 Switching Losses Calculation Algorithm

In this paper load current peak is assumed constant (29A) when circuit is in ordinary situation. At first, total switching loss is calculated for different RG_{on} and VG^+ parameters then a point with minimum switching loss is available between them. At last by using RG_{on} and VG^+ of this point, RG_{off} is calculated by MATLAB program.

Switching Loss Calculation Algorithm is according to fig.1.

In this algorithm by using continuous modulation function for 2-level inverter and discrete modulation function for 3-level, inverter Switching Losses Calculation is performed.

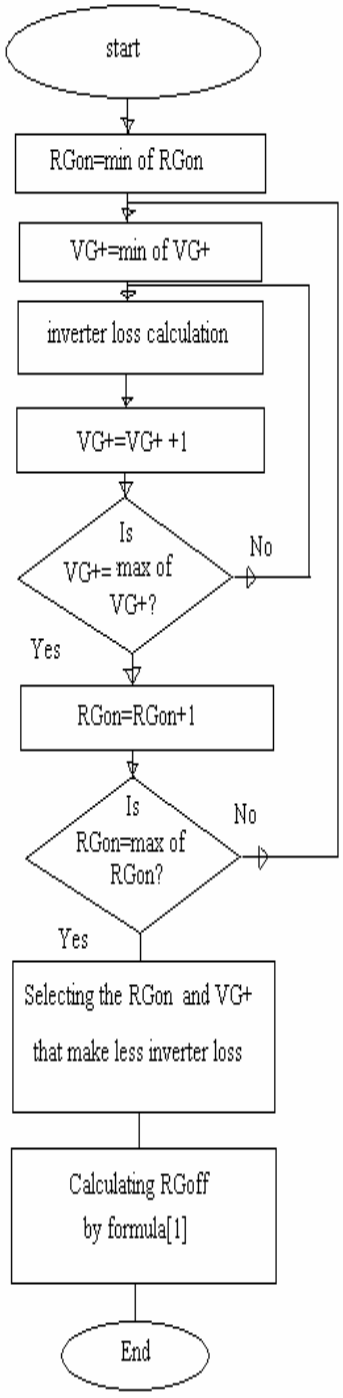

Fig.1-Algorithm of calculating optimized parameters

Input parameters are according to table-1 [1] and results of gate circuit optimized parameters calculation are in table-2 for 2-level and table-3 for 3-level NPC inverter and fig.s2 -7.

Table 1- Parameters for optimized design of three-phase inverter [1]

Circuit	Device	Designer
L_{st}=120nH V_{DC}=600V	g_m=22 C_{GC1}=75pF τ=325ns τ_{rr}=51ns $V_{GE(th)}$=5.5V C_{ies1}=7.8nF $\left(\frac{di}{dt}\right)diode = 200\ A/\mu s$ K_t=.25 $t_{i,tail}$=300ns $V_{0,D}$=.82V $V_{0,T}$=1.54V $r_{0,D}$=.084Ω $B_{con,T}$=1 $B_{con,D}$=.66 α=.137V^{-1} V_{G0}=8 R_{0T}=36.4mΩ R_{thD}=1K/W R_{thT}=.31K/W	Ip=70A Vp=800V V_{G+}=18V V_{G-}= -7V $I_{L,max}$=50A f_{sw}=5kHz f_s=50Hz Φ=38° m=1 $V_{G,min}$=8V $V_{G,max}$=20V

Table 2- optimized parameters for 2-evel inverter

Limit	P_{totmin}	V_{G+}	$R_{G\,on\,min}$	R_{Goff}
Rg=1:10:40 Vg+=18:1:20	209.7950	18	31	42.2921
Rg=1:5:40 Vg+=18:1:20	206.6530	19	36	45.6767
Rg=1:1:40 Vg+=18:1:20	204.4587	20	40	49.0613
Rg=1:1:40 Vg+=8:1:20	204.4587	20	40	49.0613
Rg=1:1:100 Vg+=8:1:20	200.1758	20	61	49.0613

Table 3-optimized parameters for 3-level NPC inverter

Limit	P_{totmin}	V_{G+}	$R_{G\,on\,min}$	R_{Goff}
R_{Gon}=1:10:40 V_{G+}=18:1:20	559.8781	18	31	42.2921
R_{Gon}=1:5:40 V_{G+}=18:1:20	553.8348	18	36	42.2921
R_{Gon}=1:1:40 V_{G+}=18:1:20	550.6067	19	40	45.6767
R_{Gon}=1:1:40 V_{G+}=8:1:20	550.6067	19	40	45.6767
R_{Gon}=1:1:100 V_{G+}=8:1:20	542.3623	20	61	49.0613

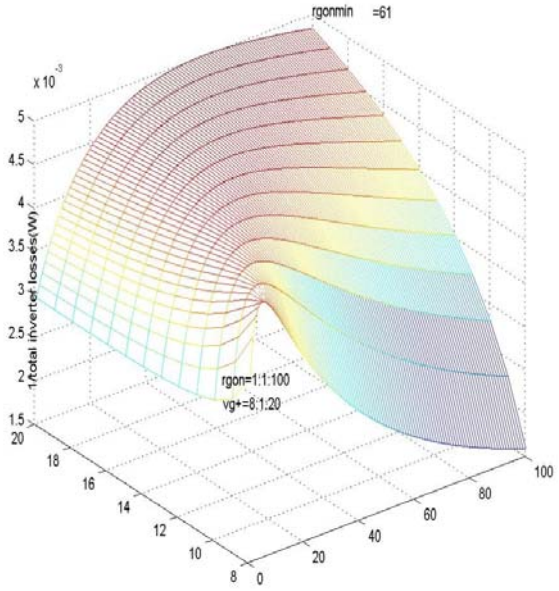

Fig. 2-Depict of minimum total loss parameters when $1<R_{gon}<100$ and $8<V_{G+}<20$ are varied for 2-level inverter.

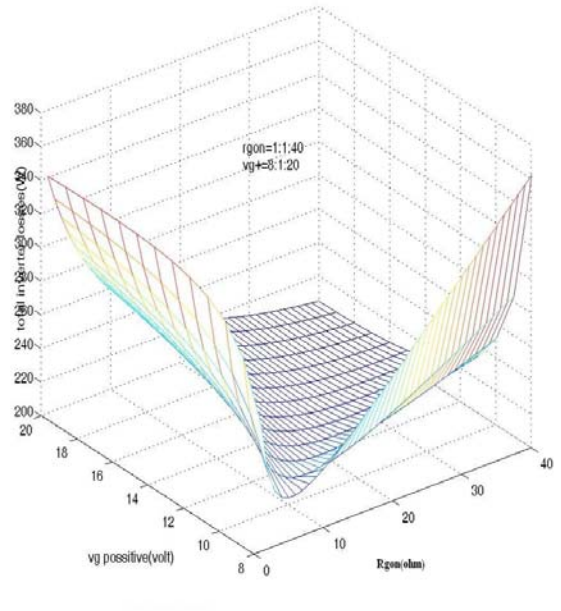

Fig. 4-Depict of total loss parameters when $1<R_{gon}<40$ and $8<V_{G+}<20$ are varied for 2-level inverter.

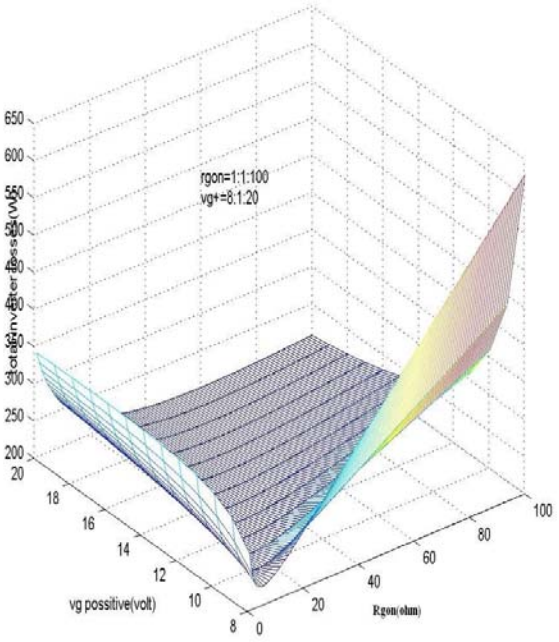

Fig. 3-Depict of total loss parameters when $1<R_{gon}<100$ and $8<V_{G+}<20$ are varied for 2-level inverter.

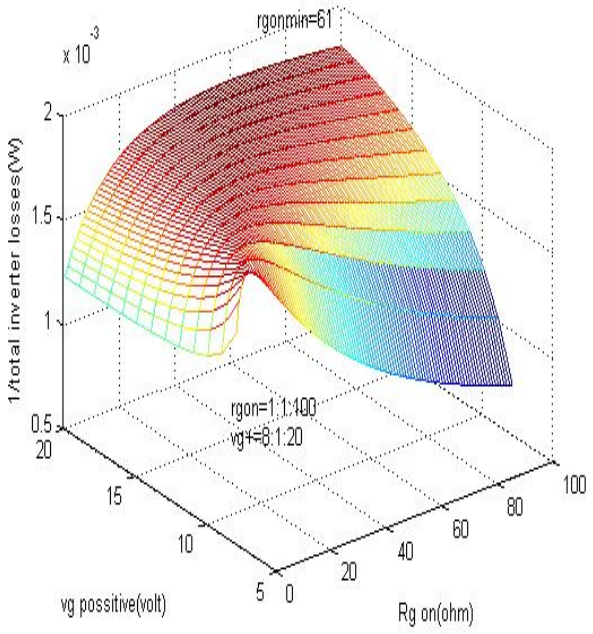

Fig. 5-Depict of minimum total loss parameters when $1<R_{gon}<100$ and $8<V_{G+}<20$ are varied for 3-level NPC inverter.

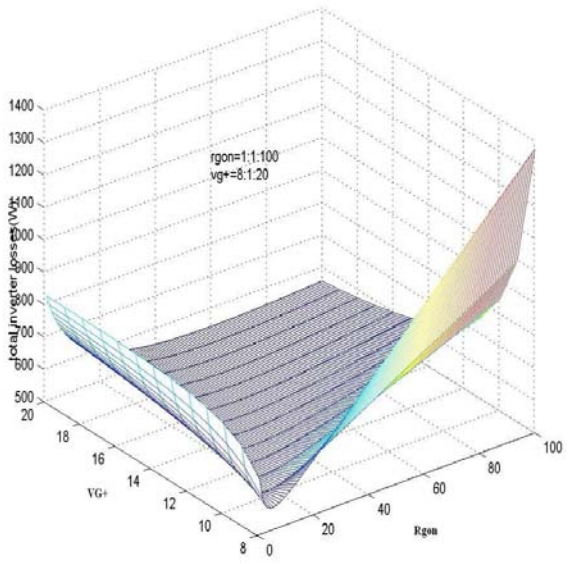

Fig. 6-Depict of total loss parameters when $1<R_{gon}<100$ and $8<V_{G+}<20$ are varied for 3-level NPC inverter.

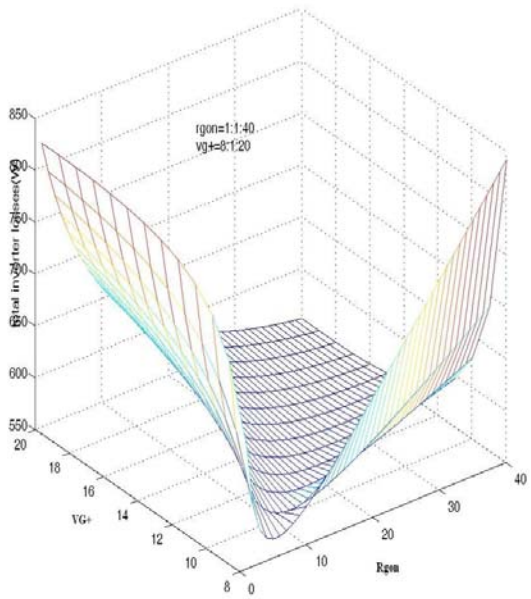

Fig. 7-Depict of total loss parameters when $1<R_{gon}<40$ and $8<V_{G+}<20$ are varied for 3-level NPC inverter.

By using optimized parameters in table 3 snubber parameters are calculated by:

$$C_s=I_L/(dV/dt) \quad (18)$$

$$L_s=V_s/(di/dt) \quad (19)$$

$$R_s=\sqrt{\frac{Ls}{Cs}} \quad (20)$$

The results are:

C_s=9.159n; L_s=1.0052μ; R_s=7.24

That are applied for 3-level inverter simulation with SVM switching method in SIMULINK and percent of inverter losses over input power is according to table 4.

Table 4- optimized parameters for 3-level inverter for V_i=600v

Simulation	V_i	$\frac{Ploss_{inv}}{P_i}\%$
optimized	600	0.26
ordinary	600	1.87

10 Results

The most important limitations for increasing of inverter switching frequency, are switching losses, problem of cooling and efficiency decreasing. If parameters of gate circuit are optimized, efficiency in high switching frequency is suitably increased. In this report by calculating total loss power of 3 level NPC for different parameters of gate and selecting optimized parameters for minimum inverter losses, maximum efficiency in a particular load current is achieved.

As a future work, this program can be performed for no sinusoidal loads. Also it is suggested to compare the results when other switching methods are applied.

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