Current Conveyor-Based Versatile Precision Rectifier

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Abstract: - A versatile precision rectifier based on a current conveyor and current mirrors is presented. The proposed circuit performs positive half-wave, negative half-wave, positive full-wave, and negative full-wave rectification into a single circuit. The current-mode technique has been employed to provide the high-precision capability of the circuit. The circuit configuration is very suitable for integrated circuit implementation both in bipolar and CMOS technologies and it exhibits a precise rectifier and good temperature stability. Simulation results using the PSPICE program based on 0.5μm CMOS parameter through MIETEC demonstrate the performance of the proposed rectifier. Experimental results are provided to confirm the theory.

Key-Words: - Precision rectifier, current conveyor, current-mode, half-wave, full-wave

1 Introduction

Rectifiers are an important circuit. It is used extensively in many applications, such as AC measurements, RF demodulators, function fitting, triangular-wave frequency doubling, error measurements, RMS to DC conversions and peak detectors to floor detectors in ultrasonic. In general, rectifier circuits are typically realized using diodes but this device cannot rectify signals whose amplitudes are less than the threshold voltage (approximately 0.7V for the silicon diode and 0.3V for the germanium diode). As a result diode-only rectifiers are used in only those applications in which the precision in the range of threshold voltage is insignificant, such as RF demodulators and DC voltage supply rectifiers. For applications requiring accuracy, the diode-only rectifiers cannot be used. It can be overcome by using integrated circuit rectifiers instead. The precision rectifiers based on operational amplifier (op-amp), diodes, and resistors are presented [1]-[4]. However, the classical problem with conventional precision rectifiers based on op-amps and diodes is that during the non-conduction/ conduction transition of the diodes, the op-amps must recover with a finite small-signal, dv/dt, (slew-rate) resulting in significant distortion during the zero crossing of the input signal. The use of the high slew-rate op-amps does not solve this problem because it is a small signal transient problem [5]. The gain-bandwidth is a parameter of op-amp that limits the high frequency performance of this scheme. Moreover, since these structures use the op-amp and the resistors; therefore these circuits are not suitable for IC fabrication. This limitation is improved by designing the rectifiers using the current-mode technique. Various current-mode precision rectifiers based on different active devices have been proposed, e.g. current conveyors (CCIIs) [5]-[9], voltage gain amplifier [10], operational transconductance amplifier (OTA) [11]-[12], realizing rectifier rectifying either as full-wave rectifier or half-wave rectifier.

In this paper, we propose a precision current-mode rectifier circuit that performs both dual output full-wave rectifier and dual output half-wave rectifier. The proposed rectifier is composed of a CCII, seven current mirrors, two diodes and five grounded resistors that yields the following advantage over other rectifiers.

(1) When the input single-phase signal is applied to the circuit, the outputs can be the function of a positive half-wave, a negative half-wave, a positive full-wave and a negative full-wave rectification without changing the circuit configuration, which no a rectifier circuit performs in this way publish in literatures. In view of these properties, we are called "the versatile rectifier circuit".
(2) The proposed configuration is very suitable for integrated circuit implementation both in bipolar and CMOS technologies.
(3) The proposed rectifier employs a CCII, seven current mirrors and five grounded resistors. The use of grounded resistors is

beneficial for IC implementation. In addition, a fully integrable rectifier circuit is also obtained by replacing the resistors with MOS/bipolar resistors in [13]-[14]. The circuit with all solid-state structure is very suitable to IC fabrication [15].

(4) The proposed rectifier provides good temperature stability.

2 Circuit Realization

The proposed versatile rectifier is shown in Fig. 1. It consists of three main components: a *V-I* converter, a current rectifier, and an *I-V* converter. The *V-I* converter is composed of a CCII and a resistor R_{in}, the current rectifier is composed of diodes and current mirrors and the *I-V* converter composed of resistors R_{oi} (i=1, 2, 3, and 4). From Fig. 1(b), the port characteristics of the CCII are given by [15]

$$\left.\begin{aligned} V_X &= V_Y \\ I_Z &= I_X \\ I_Y &= 0 \end{aligned}\right\} \tag{1}$$

When an input voltage is applied to node V_{in} of the circuit, using (1) the output current of CCII (i_Z) can be written as

$$i_z = \frac{V_{in}}{R_{in}} \tag{2}$$

where R_{in} is conversion resistance. This current is fed into the input of the current-mode rectifier. In the proposed rectifier, the current-mode versatile rectifier consists of seven current mirrors CM1-CM7 (M1-M17); two diodes; and six constant current sources (I_o, I_1-I_4). The constant current sources I_o mean that the transistors in CM1 to CM7 are turn-on all the time, reducing the problem during the non-conduction/conduction transition of these transistors whereby both currents create the offset currents (I_o and $2I_o$) through R_{oi} (i=1, 2, 3, and 4). To eliminate this offset current at R_{oi}, we exploit I_1=I_2=I_o and I_3=I_4=$2I_o$ at the output of the proposed versatile rectifier.

The operation of the proposed rectifier is as follows. When i_Z>0, it is fed through D1 and then is reflected by CM1 to the drain of M2 as -i_Z, this -i_Z is again mirrored by CM3 to the drain of M6 as I_{o1} (+i_Z). In addition, when i_Z<0, it is fed through D2 and then is reflected by CM2 to the drain of M4 as -i_Z, this -i_Z is again reflected by CM4 to the drain of M9 as I_{o2} (+i_Z). The relations between the input current i_Z and the current I_{o1}, the current I_{o2} can be expressed as

$$i_Z > 0\,;\; I_{o1} = +i_Z + I_o \tag{3}$$

$$i_Z < 0\,;\; I_{o2} = +i_Z + I_o \tag{4}$$

Sine the constant current sources I_1 and I_2 compensate the offset I_o in (3) and (4), the currents I_{o1} and I_{o2} can be rewritten as

$$i_Z > 0\,;\; I_{o1} = +i_Z \tag{5}$$

$$i_Z < 0\,;\; I_{o2} = +i_Z \tag{6}$$

Using (2) and R_{o1}=R_{o2}=R_{in}, we can write get the relations between V_{in} and V_{H+} as

$$V_{in} > 0\,;\; V_{H+} = V_{in} \tag{7}$$

$$V_{in} < 0\,;\; V_{H+} = 0 \tag{8}$$

and the relations between V_{in} and V_{H-} as

$$V_{in} > 0\,;\; V_{H-} = 0 \tag{9}$$

$$V_{in} < 0\,;\; V_{H-} = V_{in} \tag{10}$$

This means that V_{H+} and V_{H-} are the positive and negative half-wave voltage, respectively.

For the case of the full-wave rectifiers, it can be explained as follows. By using the multiple outputs current mirror, the operation of the full-wave rectifier can be continuously explained from the half-wave rectifier. When i_Z>0, the current I_{R1} that equal of the current I_{o1} is reflected by CM5 to the drain of M12 as -I_{R1} (-i_Z), this -I_{R1} is reflected again by CM6 to the drain of M14 as I_{o3} (+i_Z). In addition, when i_Z<0, the current I_{R2} that equal of the current I_{o2} is reflected by CM6 to the drain of M14 as I_{o3} (+i_Z). From the operation of the full-wave rectifier explained, the relations between the input current i_Z and the output current I_{o3} can be expressed as

$$\left.\begin{aligned} i_Z > 0\,;\; I_{o3} &= +i_Z + 2I_o \\ i_Z < 0\,;\; I_{o3} &= -i_Z + 2I_o \end{aligned}\right\} \tag{11}$$

The offset, $2I_o$, in (11) is compensated using I_3. Thus it can write the relation between i_Z and I_{o3} as

$$\left.\begin{aligned} i_Z > 0\,;\; I_{o3} &= +i_Z \\ i_Z < 0\,;\; I_{o3} &= -i_Z \end{aligned}\right\} \tag{12}$$

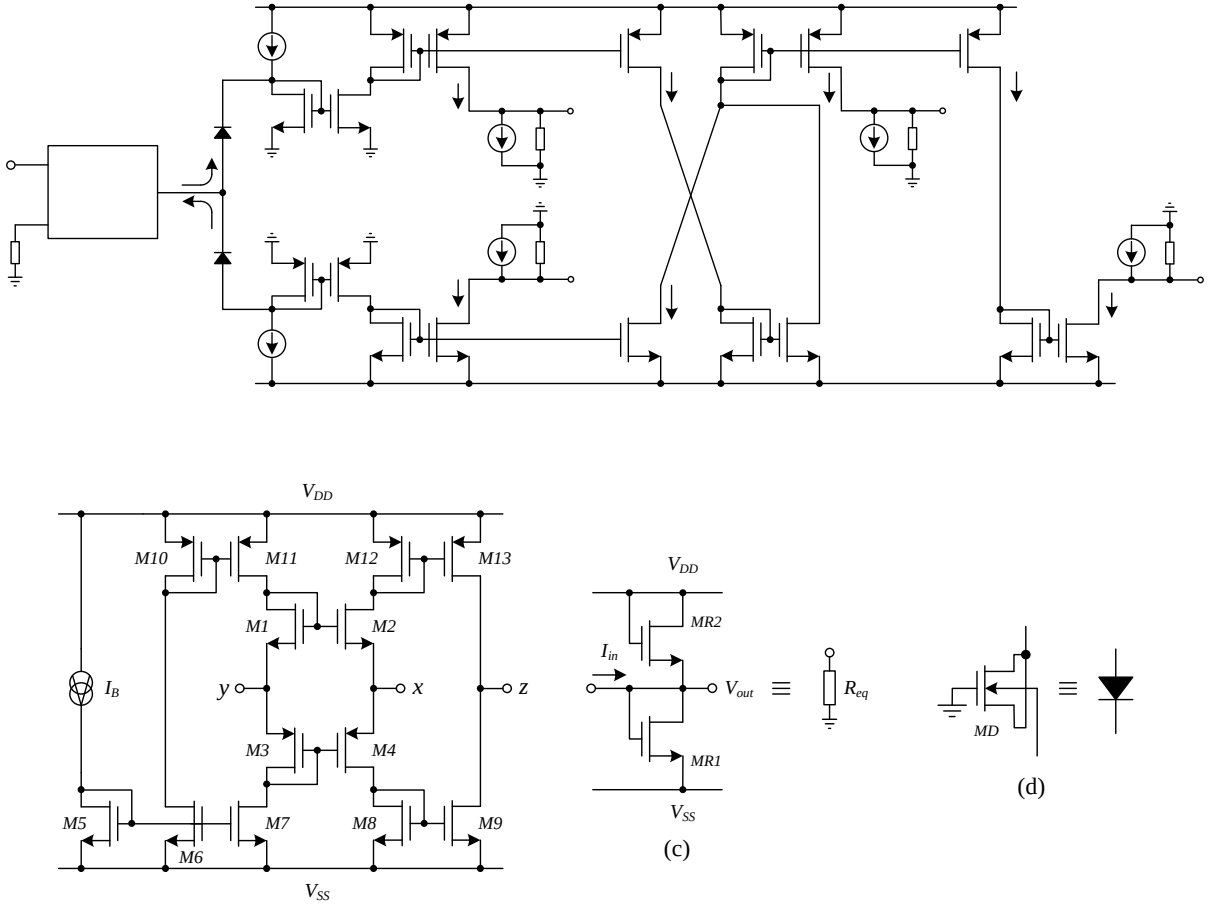

Fig. 1. The proposed rectifier: (a) CMOS implementation of the proposed versatile rectifier; (b) CMOS implementation of the CCII; (c) MOS transistor implementation for resistor [13] and (d) MOS transistor implementation for diode.

Using (2) and setting $R_{o3}=R_{in}$, it get the relation between V_{in} and V_{F+} as

$$\left.\begin{array}{l} V_{in} > 0 \;;\quad V_{F+} = +V_{in} \\ V_{in} < 0 \;;\quad V_{F+} = -V_{in} \end{array}\right\} \tag{13}$$

It is evident in (13) that V_{F+} is the positive full-wave rectifier.

The negative full-wave rectifier uses the current mirror CM7, which operate as follows. By using multiple outputs current mirror, $I_{o3}=I_{R3}$ as well as $R_{o4}=R_{in}$, the current I_{R3} is reflected by CM7 to the drain of M17 as I_{o4}. The relation between the V_{in} and V_{F-} can be expressed as

$$\left.\begin{array}{l} V_{in} > 0 \;;\quad V_{F-} = -V_{in} \\ V_{in} < 0 \;;\quad V_{F-} = +V_{in} \end{array}\right\} \tag{14}$$

where the offset, $2I_o$, is compensated by using I_4. This means that the proposed rectifier can be operated as the negative full-wave rectifier. It is evident in equations (7)-(10) and (13)-(14) that the proposed rectifier provides a positive half-wave rectifier, a negative half-wave rectifier, a positive full-wave rectifier, and a negative full-wave rectifier into a single circuit hence the name "versatile precision rectifier".

The resistors R_{in}, R_{o1}, R_{o2}, R_{o3} and R_{o4} in Fig. 1(a) can be implemented by MOS transistors. MOS resistor by using two MOS transistor is shown in Fig. 1(c) by Wang [13]. Assume MR1 and MR2 have the same characteristics and operating in the saturation regions, the resistance value can be expressed as

$$R_{eq} = \frac{1}{2K(V_{DD} - V_{TH})} \tag{15}$$

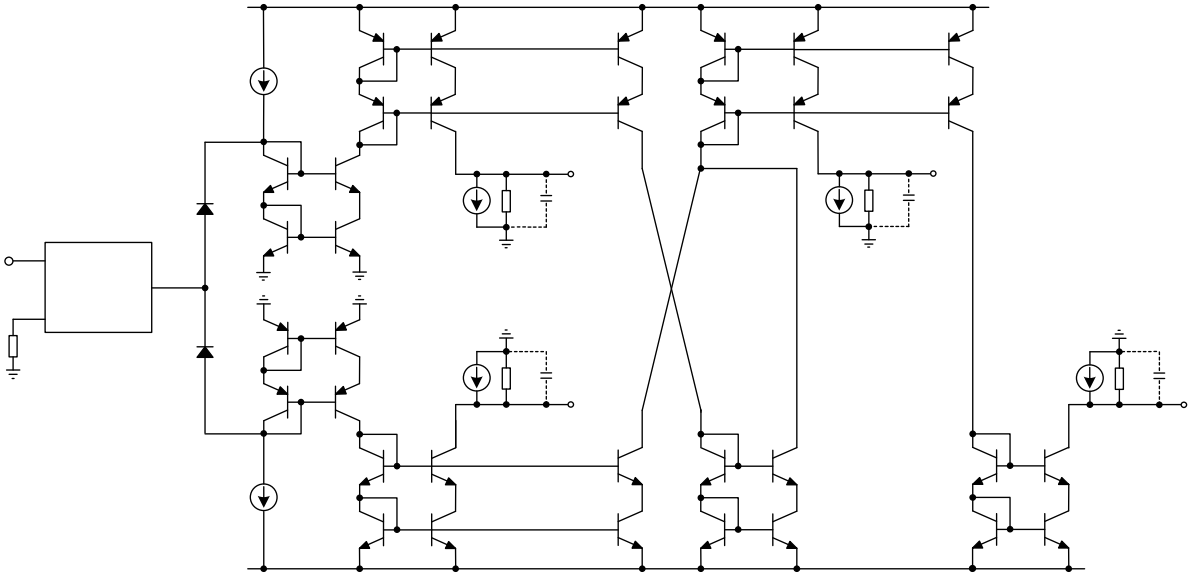

Fig. 2. The bipolar implementation of the proposed versatile rectifier.

where $K=\mu_O C_{OX}(W/L)$, V_{TH} is the threshold voltage, $V_{DD}=|-V_{SS}|$ is the supply voltage, μ_O is the carrier mobility, C_{OX} is the gate capacitance per unit area, and W and L are the channel width and length, respectively. The diodes D1 and D2 can be implemented by MOS transistor. Fig. 1(b) shows the MOS diode. It can be implemented by drain-source-connected and gate-attached to ground [7].

Fig. 2 shows the proposed versatile rectifier using bipolar technology. The simple current mirrors in Fig. 1 are replaced by cascode current mirrors. For all solid-state structure, bipolar diodes (base-collector connected) [8] must substitute two diodes and bipolar resistors [14] must substitute five resistors in Fig. 2. From schematics in Figs. 1 and 2, it has been confirmed that the proposed structure can be implemented both in CMOS and bipolar technologies.

3 Error Analysis

In practical realization, the deviation from ideal performance of the circuit is due to the non-ideal characteristics of the CCII and the current mirrors being used. If ε_V and ε_i ($|\varepsilon_V|\ll 1$ and $|\varepsilon_i|\ll 1$) represent the voltage and current tracking errors, respectively, of the CCII, the port characteristics of CCII can be rewritten as

$$\left.\begin{aligned} V_X &= \beta V_Y \\ I_Z &= \alpha I_X \\ I_Y &= 0 \end{aligned}\right\} \tag{16}$$

where $\beta=1-\varepsilon_V$ and $\alpha=1-\varepsilon_i$. By using (14), current i_Z can be rewritten as

$$i_z = \frac{\alpha\beta V_{in}}{R_{in}+r_X} \tag{17}$$

when r_X is the parasitic resistance looking into the port X of the CCII.

For the non-ideal of current mirror, we first consider the proposed structure in Fig. 1(a). The error of the simple current mirrors, i.e. the input and output currents of simple current mirror is given by [17]:

$$I_{out} = I_{in}\left(1-\varepsilon_M\right) \tag{18}$$

and

$$\varepsilon_M = \lambda\left(\frac{1}{g_m}-\frac{1}{g_d}\right) \tag{19}$$

where λ, is the channel-length modulation factor of MOS transistor, g_m is the transconductance gain and g_d is the drain conductance of MOS transistor. Taking the non-ideals of the CCII and the current mirror into the account, equations (7) and (10) can be rewritten as

$$V_{in}>0\,;\; V_{H+}=\frac{\alpha\beta V_{in}R_{o1}}{R_{in}+r_X}-2\varepsilon_M R_{o1} \tag{20}$$

$$V_{in}<0\,;\; V_{H-}=\frac{\alpha\beta V_{in}R_{o2}}{R_{in}+r_X}-2\varepsilon_M R_{o2}\,. \tag{21}$$

and equations (13) and (14) can be rewritten as

$$\left.\begin{array}{l} V_{in} > 0 \;;\quad V_{F+} = +\dfrac{\alpha\beta V_{in} R_{o3}}{R_{in} + r_X} - 4\varepsilon_M R_{o3} \\ V_{in} < 0 \;;\quad V_{F+} = -\dfrac{\alpha\beta V_{in} R_{o3}}{R_{in} + r_X} - 3\varepsilon_M R_{o3} \end{array}\right\} \quad (22)$$

$$\left.\begin{array}{l} V_{in} > 0 \;;\quad V_{F-} = -\dfrac{\alpha\beta V_{in} R_{o4}}{R_{in} + r_X} - 5\varepsilon_M R_{o4} \\ V_{in} < 0 \;;\quad V_{F-} = +\dfrac{\alpha\beta V_{in} R_{o4}}{R_{in} + r_X} - 4\varepsilon_M R_{o4} \end{array}\right\} \quad (23)$$

From the circuit in Fig. 1, when i_Z>0 the current $+i_Z$ is mirrored to R_{o1} by current mirrors CM1 and CM3, whereas when i_Z<0 the current $-i_Z$ is mirrored to R_{o2} by current mirrors CM2 and CM4. This means that the output voltages V_{H+} and V_{H-} are roughly equal of amplitude. It can be confirmed by (20) and (21).

For the case of full-wave rectifier, when i_Z>0 the current $+i_Z$ is mirrored to R_{o3} by four current mirrors CM1, CM3, CM5 and CM6 whereas when i_Z<0 the current $-i_Z$ is mirrored by three current mirrors CM2, CM4 and CM6. This makes the amplitude of the output voltage V_{F+} when i_Z>0 is smaller than when i_Z<0. It can be confirmed by (22) while Eq. (23) expressed the error of output V_{F-}. The amplitude error of the output voltage can be corrected by increasing the value of R_{oi} (i=1, 2, 3, 4).

From Fig. 1, the rectifier circuit bases simple current mirrors. The major factor to be effect is the finite drain resistance of the transistor. If the output resistance of the current mirror is not high, this problem can be solved by using cascode current mirrors or the Wilson current mirrors. However, the supply voltage of the rectifier circuit will be increased. Moreover, it will be also increased of transistor.

For the proposed structure in Fig. 2, the error of the cascode current mirrors, i.e. the input and output currents of cascode current mirror is given by [17]:

$$I_{out} = I_{in}(1 - \varepsilon_B) \quad (24)$$

and

$$\varepsilon_B = \frac{4\beta + 2}{\beta^2 + 4\beta + 2} \quad (25)$$

where β is the current gain of all bipolar transistors of cascode current mirrors. Taking the non-ideals of the CCII and the current mirrors into the account, the relation between V_{in} and V_{H+}, V_{H-}, V_{F+}, V_{F-} can be written as same equations (20)-(23) but it must replace ε_M with ε_B.

4 Results

4.1 Simulation Results

In order to test the ideal designed, the schematic in Fig. 1 has been simulated by using the PSPICE simulation program and the schematic in Fig. 2 has been constructed on printed circuit. The parameters used in simulation are 0.5μm CMOS model obtained through MIETEC [7] as listed in Table 1. The aspect ratio (W/L) of MOS transistors used are as follows: 20μm/0.6μm for all NMOS transistors; 60μm/0.6μm for all PMOS transistors, while 40μm/0.6μm for MR1-MR2, and 1μm/0.6μm for MDs. The supply voltage used is ±1.5V. The current source values used were I_1=I_2=I_o=25μA. I_3 and I_4 were therefore set to I_3=I_4=2I_o=50μA. R_{o1} to R_{o4} and R_{in} are replaced with MOS resistors as shown in Fig. 1(c). The DC transfer characteristics of the proposed rectifier are shown in Fig. 3, which shows the operating voltage ranging from –200mV to 200mV of the input voltage.

Table 1. CMOS model used in the simulation.

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.MODEL NMOS LEVEL=3 UO=460.5 TOX=1.0E-8
+TPG=1 VTO=+0.62 JS=1.08E-6 XJ=0.15U RS=417
+RSH=2.73 LD=0.04U VMAX=130E3 NSUB=1.71E17
+PB=0.761 ETA=0.00 THETA=0.129 PHI=0.905
+GAMMA=0.69 KAPPA=0.10 CJ=76.4E-5 MJ=0.357
+CJSW=5.68E-10 MJSW=0.302 CGSO=1.38E-10
+CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28
+AF=1 WD=+0.11U DELTA=+0.42 NFS=1.2E11
+DELL=0U LIS=2 ISTMP=10 TT=0.1E-9

.MODEL PMOS LEVEL=3 UO=100 TOX=1.0E-8
+TPG=1 VTO=-0.58 JS=0.38E-6 XJ=0.10U RS=886
+RSH=1.81 LD=0.03U VMAX=113E3 NSUB=2.08E17
+PB=0.911 ETA=00 THETA=0.120 PHI=0.905
+GAMMA=0.76 KAPPA=2 CJ=85E-5 MJ=0.429
+CJSW=4.67E-10 MJSW=0.631 CGSO=1.38E-10
+CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29
+AF=1 WD=+0.14U DELTA=0.81 NFS=0.52E11
+DELL=0U LIS=2 ISTMP=10 TT=0.1E-9
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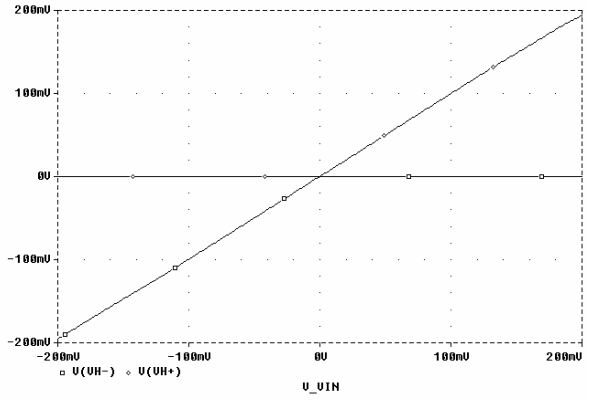
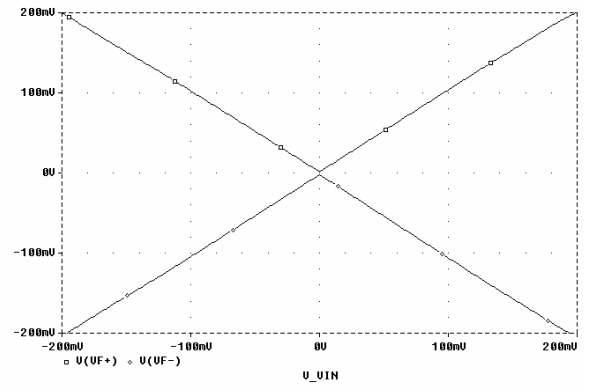
Applying the 100mV$_{peak}$ sine wave at the input of the proposed rectifier, the input and output signals at frequencies of 100kHz, 1MHz, and 10MHz are shown in Figs 4-6, respectively, where (a) the input and positive half-wave output V_{H+}, (b) the input and negative half-wave output V_{H-}, (c) the input and positive full-wave output V_{F+}, (d) the input and negative full-wave output, V_{F-}. From these results,

they show that the proposed rectifier is a versatile rectifier circuit. In addition, undistorted half-wave and full-wave rectified signals are produced at all three frequencies. At the frequency of 100kHz, we again simulate the proposed rectifier in Fig. 1 by changing temperatures from 50°C to 100°C. Fig. 7 shows the output waveform of the proposed rectifier at temperatures of 50°C, 75°C and 100°C. From the simulation results in Fig. 7, it is evident that the proposed rectifier circuit provides excellent temperature stability.

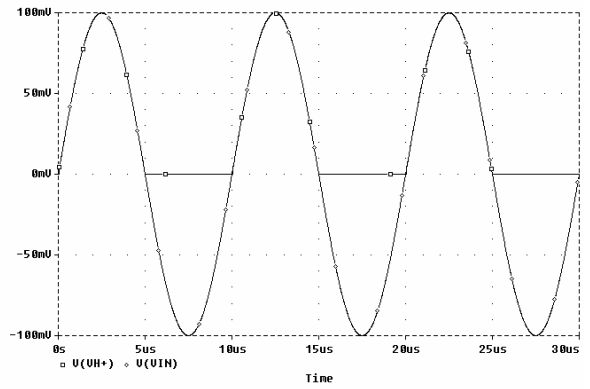


(a)

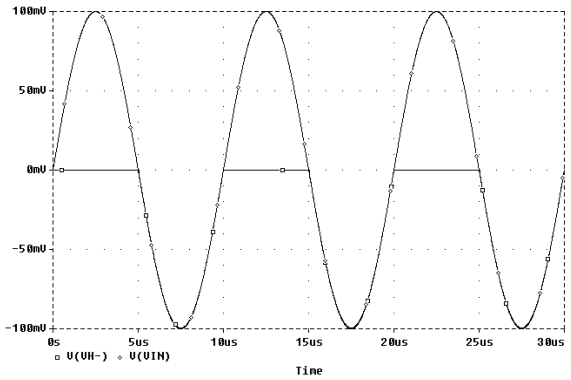


(b)

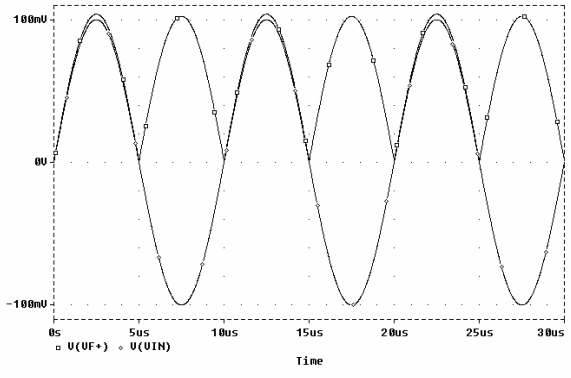
Fig. 3. DC transfer characteristics: (a) half-wave rectifier; (b) full-wave rectifier.



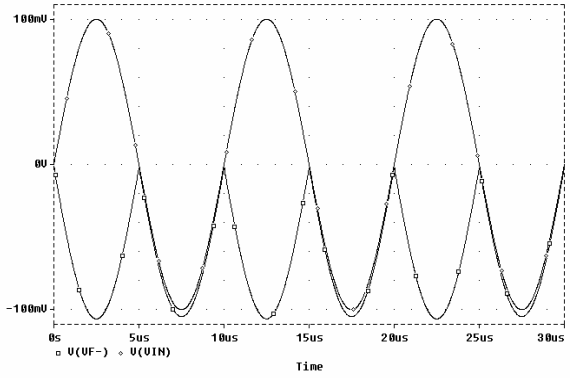
(a)



(b)

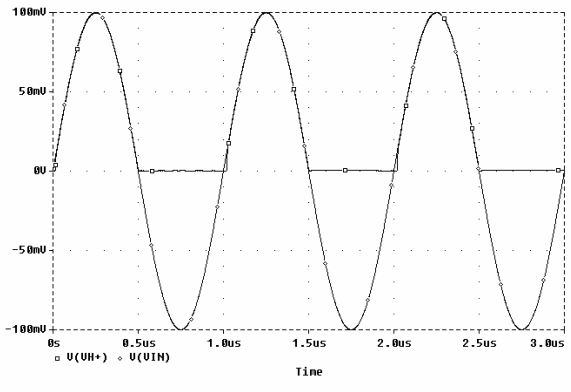


(c)

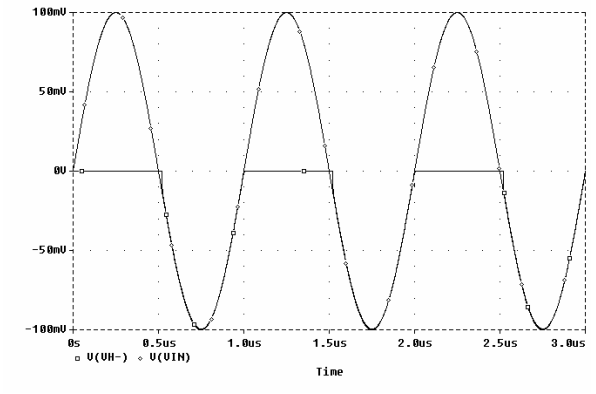


(d)

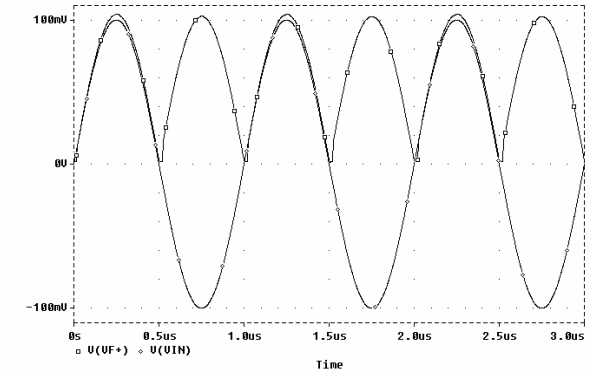
Fig. 4. Operation of rectifier in Fig. 3 at the input signal frequency 100kHz: (a) V_{in}, V_{H+}; (b) V_{in}, V_{H-}; (c) V_{in}, V_{F+} and (d) V_{in}, V_{F-}.



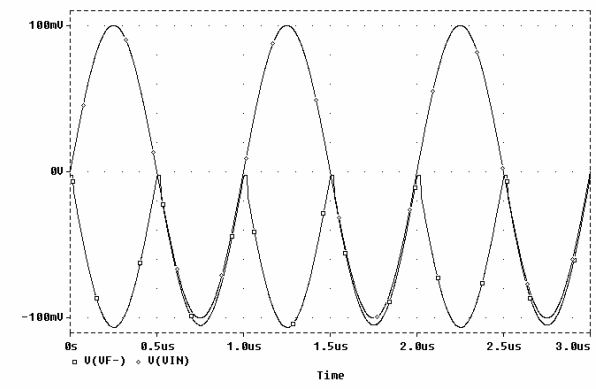
(a)



(b)



(c)



(d)

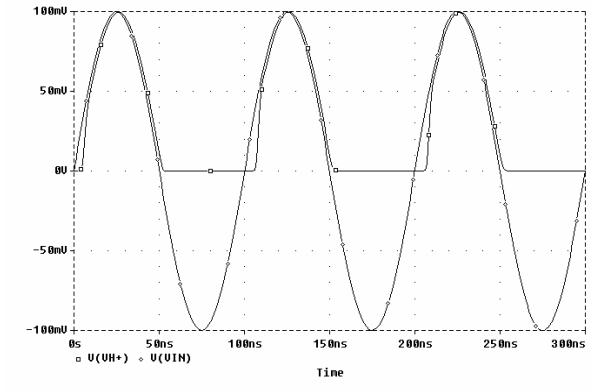
Fig. 5. Operation of rectifier in Fig. 3 at the input signal frequency 1MHz: (a) V_{in}, V_{H+}; (b) V_{in}, V_{H-}; (c) V_{in}, V_{F+} and (d) V_{in}, V_{F-}.

(b)

(c)

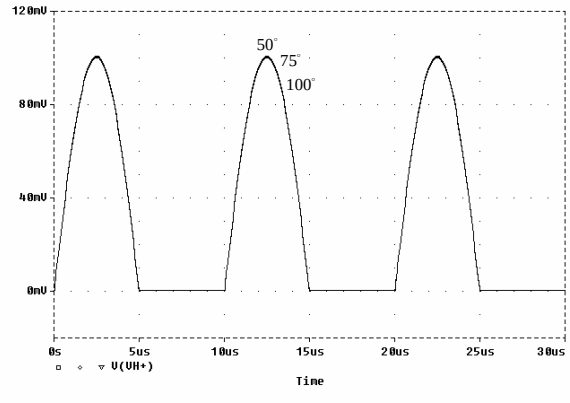
(d)

Fig. 6. Operation of rectifier in Fig. 3 at the input signal frequency 10MHz: (a) V_{in}, V_{H+}; (b) V_{in}, V_{H-}; (c) V_{in}, V_{F+} and (d) V_{in}, V_{F-}.

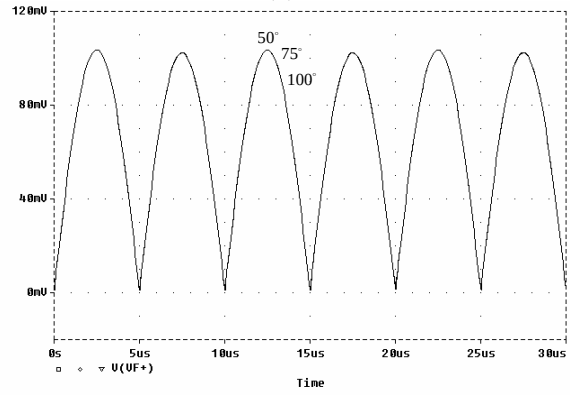


(a)

Again, applying the 100kHz sine wave of amplitude $10mV_{peak}$ at the input of the circuit in Fig. 1, the input and output signals are shown in Fig. 8. From these results, it is apparent that the circuit exhibits undistorted of the output signal for an input signal of peak amplitude as low as 10mV. This shows that the proposed rectifier has high input signal sensitivity. This is as a direct result of the action of the current-mode rectifier which is operated in class B and the fast action of the CCII. The accuracy of the system is verified as (7), (8), (11), and (12) is confirmed to a good approximation.

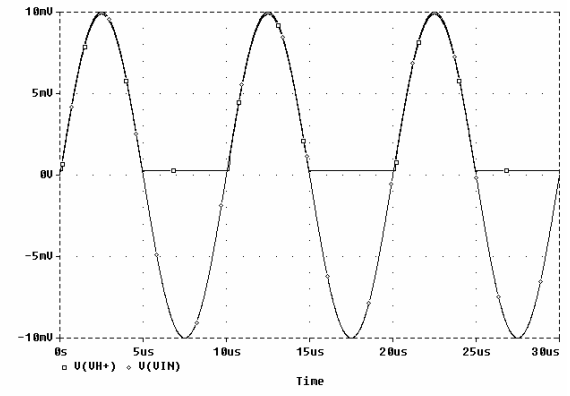


(a)

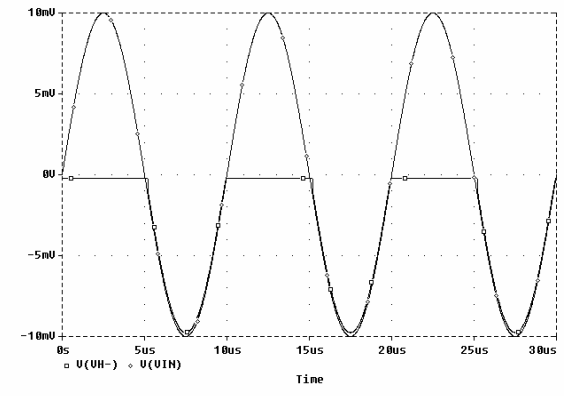


(b)

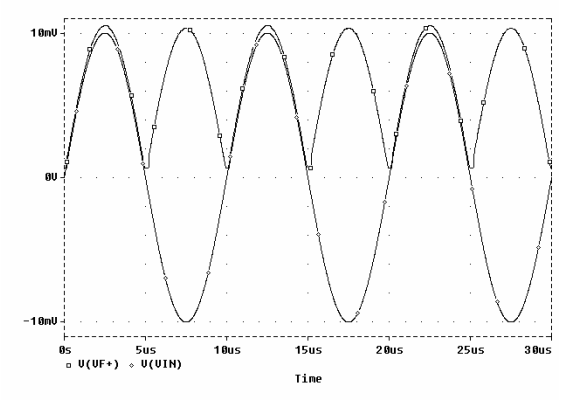
Fig. 7. Outputs waveforms at different temperature: (a) V_{H+} and (b) V_{F+}.



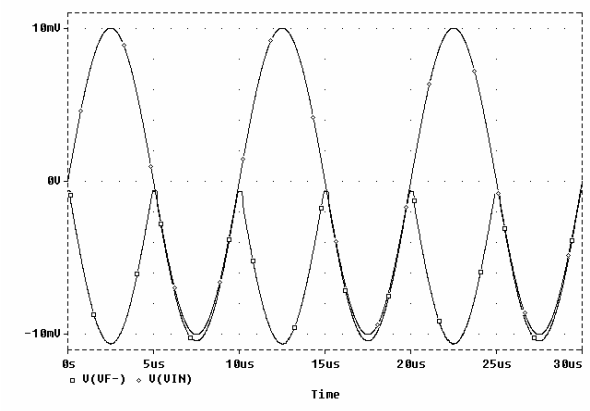
(a)



(b)



(c)



(d)

Fig. 8. Outputs waveforms at the input signal frequency 100kHz for 10mV$_{peak}$: (a) V_{in}, V_{H+}, (b) V_{in}, V_{H-}, (c) V_{in}, V_{F+}, (d) V_{in}, V_{F-}.

4.2. Experimental results

For experimental purpose, the circuit in Fig. 2 has been constructed on printed circuit as shown in Fig. 9. The AD844AN was used along with 2N3904 npn and 2N3906 pnp transistors. 1N914 diode was used. R_{in} was set to 200Ω while R_{o1} to R_{o4} and C_L were set to 300Ω and 1nF, respectively. The supply voltages used was ±10V. The currents source values used were I_1=I_2=100μA. I_3 and I_4 was therefore set to I_3=I_4=200μA.

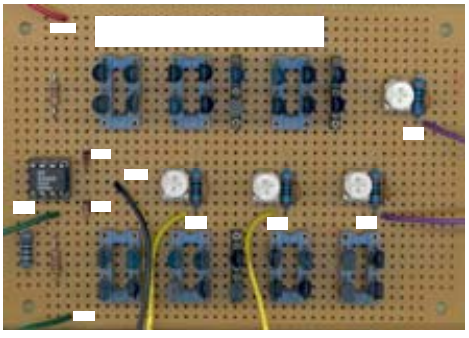
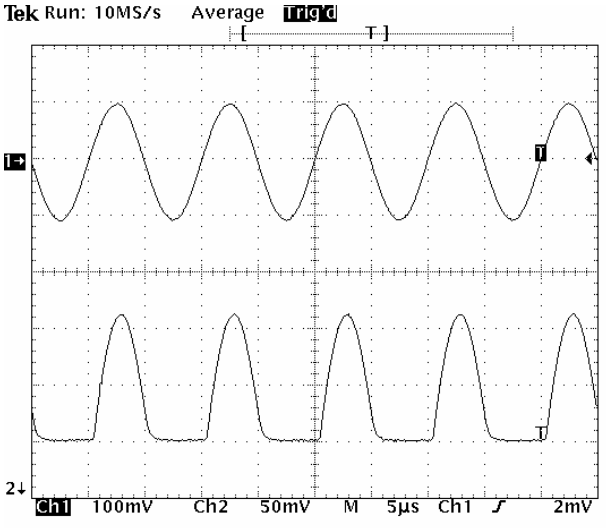
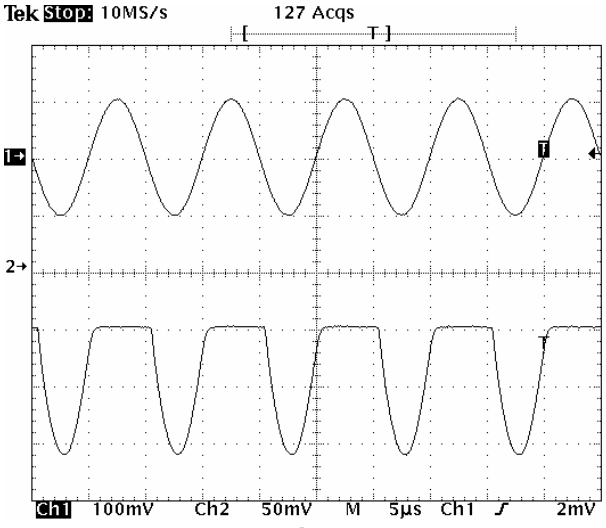


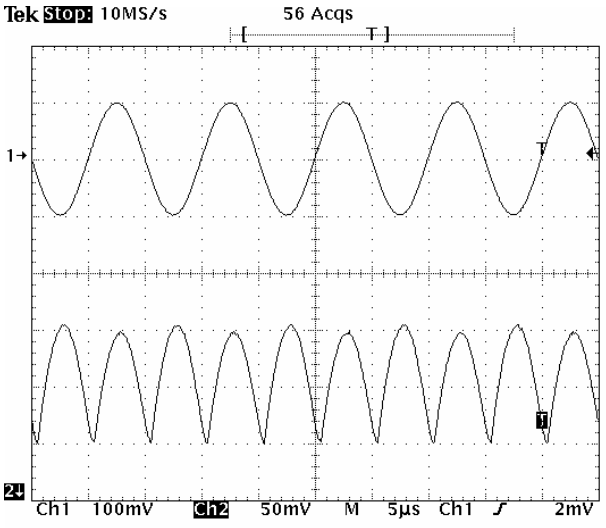
Fig. 9. Versatile precision rectifier prototype.



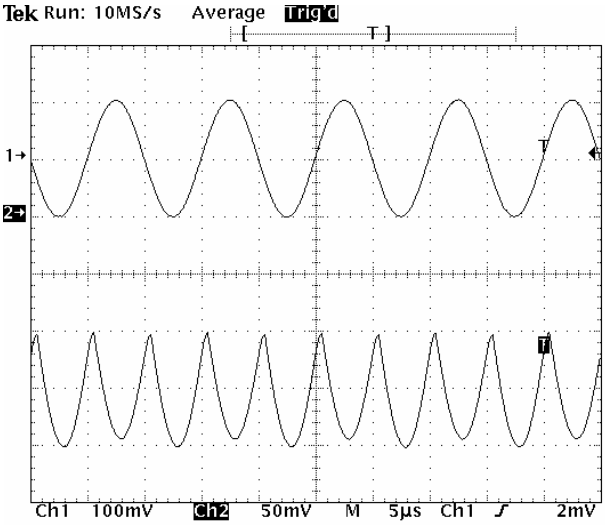
(a)



(b)



(c)



(d)

Fig. 10. Experimental for rectifier circuit in Fig. 2 at the input signal frequency 100kHz: (a) V_{in} and V_{H+}, (b) V_{in} and V_{H-}, (c) V_{in} and V_{F+}, (d) V_{in} and V_{F-}; upper track: $200mV_{P-P}$ sine signal of 100kHz (100mV/div), lower track: output wave form (50mV/div), horizontal scale is 5µs/div.

Fig. 10 shows the transient response of the circuit in Fig. 2 for input signal frequency 100kHz of amplitude $100mV_{peak}$. In this test, it is evaluated that the circuit in Fig. 2 can operate at a few 100kHz frequencies with undistorted rectified signals. The conduction/non-conduction of diodes is a cause the high frequency limitation. It can see that at an input signal frequency of 100kHz the output waveform of proposed rectifier has a better shape than that the output waveform of the rectifier circuit in [8].

5 Conclusions

A versatile precision rectifier circuit was presented in this paper. The proposed circuit have distinguish in used of a CCII and current mirrors, and its combine a positive half-wave rectifier, a negative half-wave rectifier, a positive full-wave rectifier, and a negative full-wave rectifier into a single circuit. The configuration described is very suitable for integrated circuit implementation both in bipolar and CMOS technologies. The use of grounded resistors is beneficial to IC implementation. For CMOS implementation, the proposed rectifier uses a ±1.5V supply voltage and produces an input operating ranging from -200mV to +200mV. The proposed versatile rectifier uses the MOS transistor for convert the output current to output voltage which is suitable for a high impedance load. If the

proposed rectifier is loaded by a low impedance load, the load may be connected directly instead of the output resistors (R_{o1}, R_{o2}, R_{o3} and R_{o4}), it needs the linear input resistor (R_{in}). The diodes can be implemented by using MOS transistors. For bipolar implementation, the operating frequency is up to 100kHz. The experimental results are included to confirm theory.

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