# High-PSR-Bandwidth Capacitor-Free LDO Regulator with 50μA Minimized Load Current Requirement for Achieving High Efficiency at Light Loads

Huan-ChienYang, Ming-Hsin Huang, and Ke-Horng Chen

Electrical and Control Engineering National Chiao Tung University, Hsinchu, Taiwan

*Abstract:* - A capacitor-free LDO regulator with the minimized-Q (MQ) and adaptive zero compensation (AZC) techniques is proposed in this paper. With the MQ technique, light load efficiency is greatly improved since only 50μA minimized load current is required. Furthermore, due to noise cancellation from power supply, the LDO regulator with the MQ technique has higher PSR bandwidth with compatible compensation capacitors compared to the Q-reduction technique [1]. Besides, fast transient response time is also achieved because phase margin equals to 60 degree is always maintained by the MQ and AZC techniques. The capacitor-free LDO regulator with the MQ and AZC techniques was fabricated in TSMC 0.35μm 2P4M CMOS process with small compensation capacitors 5pF and 1.5pF. Experimental results demonstrate that the minimum load can be reduced to about 50μA and transient response time can be reduced by the MQ and AZC techniques to be smaller than 4μs. The measured load and line regulation are 20μV/mA and 3.3mV/V respectively.

*Key-Words:* - Capacitor-free LDO regulator, minimum load, frequency compensation, PSR bandwidth, fast transient response

## 1 Introduction

With the increasing demanding of portable devices, how to use the battery energy efficiently is the most concerned problem. Therefore, power management system is indispensable for modern consumer products. For power management system, low-dropout liner regulator is the most common block due to the characteristics, such as simplicity, small board space, low noise and cost.

Conventional low-dropout liner regulator is compensated by the equivalent series resistor (ESR). However, this kind compensation is hardly to maintain because gain and poles locations are varied with load conditions [2]-[4]. In recent years, the demanding for high performance liner regulator such as high load regulation and high power supply rejection is getting growing. In the meanwhile, owing to the development of SoC system, a capacitor-free LDO shown in Fig. 1 is preferred to reduce the footprint area and cost greatly. For modern consumer products, high precision and high PSR performance are required. Capacitor-free LDOs with characteristics of high DC gain can achieve these requirements. For example, capacitor-free LDOs can be used in DSPs or other precision-concerned devices that require high load regulation and in RF or other noise-sensitive circuits which need high power supply rejection. Since capacitor-free LDOs do not need an off-chip capacitor be compensated, it is requisite for SoC applications and cost is greatly reduced [5]-[7].

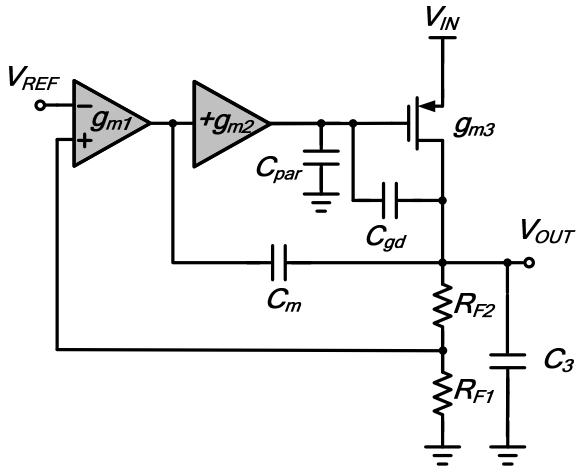


Fig. 1. Conventional three-stage capacitor-free LDO regulator.

For nowadays, the multi-stage LDO regulators can achieve high low-frequency gain for getting better load and line regulation and capacitor-free characteristic for minimizing the external footprint area. Three-stage LDO design inherently needs to be compensated by a nested Miller compensation (NMC) topology that is composed of a miller capacitor and the large gate-to-drain capacitor of power MOSFET. However, this topology suffers minimum load restriction for three-stage LDO regulators [8]-[12]. In other words, it suffers from oscillation problems at very light load condition. Therefore, capacitor-free LDOs with Miller compensation have the problem of minimum load restriction [9, 10]. Besides, in [1, 5], the system bandwidth is limited by the complex pair, which is generated by the output pole and the pole at gate of power MOSFET at light load condition. That is the system phase margin has to be designed at 90 degree [1, 5]. Therefore, the response time is slowed down due to inappropriate phase margin and narrow bandwidth.

The methodologies of reducing the minimum load limitation are classified into two techniques. Moving the pole at the output or the pole at the gate of the power MOSFET to a higher frequency is an important technique to make sure the stability at light load condition. The damping factor control (DFC) technique [5, 12] provides a method to control the damping factor to achieve reduction of quality (Q) factor. Owing to the short path generated by the Miller capacitor, the other DFC capacitor shorts the DFC amplifier to get a small resistance for generating a smaller time constant than that without DFC capacitor. However, its minimum load current is not carefully considered because the effect of capacitance $C_{gd}$ of the power MOSFET is ignored in the analysis. The existence of the large capacitance $C_{gd}$ makes the complex poles appear at a higher load current condition. This technique still has the high-Q problem when load current decreases. The load current range is about 100μA to 10mA with a DFC compensation capacitor, which has the same value as the miller capacitor. It means that the high Q problem may cause the system unstable.

Therefore, Q-reduction technique [1] uses the other technique to move the pole at the gate of the power MOSFET to a higher frequency to reduce minimum load limitation. It decreases the minimum load to about 100μA by using a compensation capacitor $C_{cf}$ 1pF. However, the additional compensation capacitor $C_{cf}$ provides a ground path to the gate of p-type power MOSFET, the noise from the supply voltage will be feed through to the output directly. It means the Q-reduction method solves the minimum load current problem but it deteriorates the PSR performance seriously [13]-[15]. Both minimum load current and maximum PSR bandwidth cannot be demanded at the same time by the Q-reduction technique.

In this paper, minimized Q and adaptive zero compensation techniques for three-stage LDO regulator are proposed, which can be operated in ultra light load operation and with high power supply rejection. Besides, the adaptively adjusting the phase margin achieves fast transient response. Therefore, MQ and AZC techniques are proposed for capacitor-free LDO regulator to reduce the minimum load restriction to about 50μA and maintain appropriate phase margin about 60 degrees to achieve faster transient response. The architecture of the proposed LDO regulator is shown in Section 2. Section 3 describes circuit implementation of the LDO with MQ and AZC techniques. Experimental results are shown in Section 4. Finally, a conclusion is made in Section 5.

## 2 Architecture of the Proposed LDO Regulator

The minimized Q (MQ) and adaptive zero compensation (AZC) techniques are proposed to reduce the minimized load restriction without sacrificing PSR performance. The frequency response of the proposed LDO with MQ and AZC techniques is shown in Fig. 2. The role of the MQ capacitor $C_q$ and the nulling resistor $R_{AZC}$ is to generate a pole-zero pair. Thus, the load-dependent output pole can be moved to a higher frequency because the capacitor $C_q$ and the compensation capacitor $C_m$ are short for getting a low equivalent resistance to ground at high frequency. Beside, the MQ pole that is generated by capacitor $C_q$ and located at frequency near UGF has the ability to ensure that the magnitude rolls off at a rate of -40dB/decade and then the phase margin is about 60 degree. When the frequency approaches the frequency of the complex poles, the magnitude of the loop gain is attenuated to a lower value and the system can tolerate a higher $Q$ value compared to the previous design [1]. Therefore, MQ technique can effectively reduce the minimum load restriction without the need of large compensation capacitor.

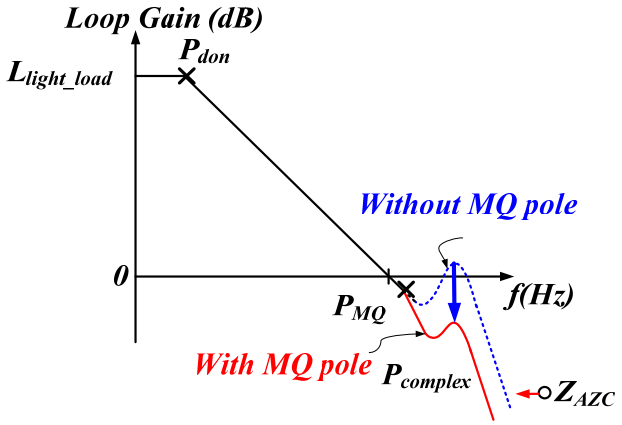


Fig. 2. The proposed capacitor-free LDO regulator with the MQ and AZC techniques.

Fig. 3(a) shows the structure of the proposed capacitor-free LDO with MQ and AZC techniques. The MQ capacitor $C_q$ connects the ground reference $V_f$ to $V_1$ when the Miller capacitor $C_m$ has a short effect at higher frequency. It means that the compensation capacitor $C_m$ provides a ground path to the output so that the PSR bandwidth can be maintained by the proposed MQ technique. However, the pole generated by the MQ capacitor $C_q$ is moved toward the origin at a load current step about mini-amp, which deteriorates the phase margin about ten degrees. Thus, an adaptive zero generated by an adaptive resistance $R_{AZC}$ is needed to compensate the phase deterioration caused by the MQ pole at heavy load condition. In other words, the adaptive zero $z_{AZC}$ is moved toward the origin owing to the increase of the load current for compensating the phase loss due to the MQ pole at heavy loads.

For the proposed capacitor-free LDO regulator, the small signal model is shown in Fig. 3(b). The $g_{m1}$~$g_{m3}$ are the equivalent transconductances of each stage. The $g_1$~$g_3$ are the equivalent output reactance of each stage and the $C_1$~$C_3$ are the lumped parasitic capacitors of each stage. The $C_p$ is the lumped capacitor of current mirror of first stage and can be neglected compared to the MQ capacitor. The huge gate-to-drain capacitor of power p-type MOSFET is represented as $C_{gd}$. The capacitors $C_m$ and $C_q$ are the Miller compensation and MQ capacitors, respectively.

The transfer function from input to output can be expressed in (1). The system consists of four poles and three zeros. The dominant pole is decided by Miller compensation capacitor $C_m$ associated with the output resistance $1/g_1$. The first non-dominant pole named as MQ pole is located near and above the UGF at light loads not only to decrease the magnitude of loop gain before the occurrence of the complex poles but also to maintain the phase margin about 60 degrees for achieving fast transient response. In (1), the numerator contains one low-frequency LHP zero generated by $1/R_{AZC}C_q$ that is named as the adaptive compensation zero $z_{AZC}$. Besides, the other two high-frequency zeros are neglected in the analysis of stability.

The stability analyses at different loads are discussed as follows:

$$Loop\ gain = -L_o \frac{\left(sC_qR_{AZC}+1\right)\left(s^2\frac{C_mC_2}{g_{m2}g_{m3}}+s\frac{g_{m2}C_{gd}}{g_{m2}g_{m3}}-1\right)}{\left(1+\frac{s}{p_{don}}\right)\left(1+\frac{s}{p_{MQ}}\right)\left(s^2\frac{C_2C_3}{g_{m2}g_{m3}}+s\frac{\left(\frac{1}{g_{mcf}}+R_{AZC}\right)\left(g_{m3}-g_{m2}\right)C_{gd}C_qC_m+MQ\_factor}{\left(\frac{1}{g_{mcf}}+R_{AZC}\right)g_{m2}g_{m3}C_qC_m}+1\right)} \quad (1)$$

where $L_o=\frac{g_{m1}g_{m2}g_{m3}}{g_1g_2g_3}$, $p_{don}=\frac{g_1g_2g_3}{C_mg_{m2}g_{m3}}$, and $MQ\_factor=\left(C_m+2C_q\right)C_2C_3$

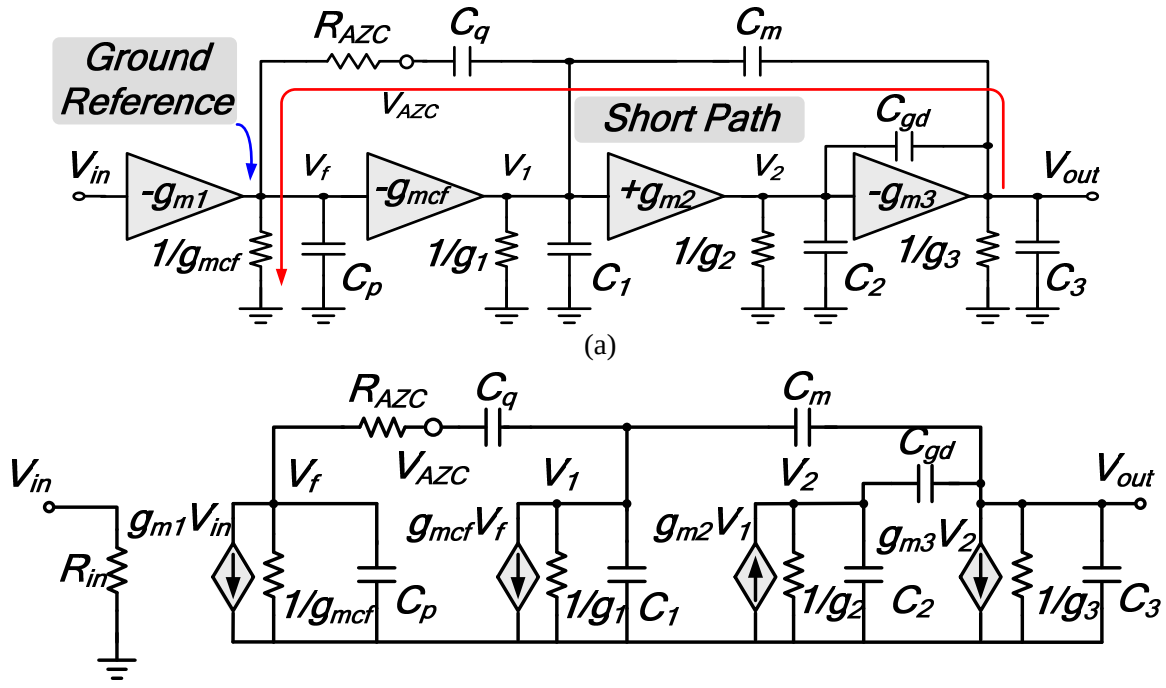


Fig. 3. Topology of capacitor-free LDO regulator with MQ and AZC technique. (a) Structure of the proposed circuit. (b) Small-signal of the proposed circuit.

*2.1 Ultra Light Load Current (i.e. the transconductance of the last stage is smaller than that of the second stage):*

Owing to the transconductance of the last stage is smaller than that of the second stage, the complex poles may locate at right half plane (RHP). Thus, the insertion of the MQ capacitor $C_q$ let the value of Q is become positive and greatly reduced due to the MQ_factor in (1). At higher frequency, the output node has low impedance to ground owing to the short path formed by Miller capacitor $C_m$. In other words, the output node has a short path to the adaptive resistance $R_{AZC}$. Thus, the adaptive resistance $R_{AZC}$ must be set to a small value at ultra light loads. It means that the series resistance composed of $R_{AZC}$ and $1/g_{mcf}$ is still small enough to form a low-impedance to ground. At this time, the output pole moves toward to the origin to form a complex at a lower load current than that of conventional capacitor-free design. The proposed LDO can achieve a minimized load current about 50μA. The frequency response with and without MQ and AZC techniques are shown in Fig. 4(a). The pole locations with small resistance $R_{AZC}$ at ultra light loads are shown in (2)-(3):

$$p_{don} = \frac{g_1 g_2 g_3}{C_m g_{m2} g_{m3}},$$
$$p_{MQ} = \frac{g_{mcf}}{C_q} \tag{2}$$
$$\omega_o = \sqrt{\frac{g_{m2} g_{m3}}{C_2 C_3}},$$
$$Q = \sqrt{\frac{C_2 C_3}{g_{m2} g_{m3}}} \frac{\frac{1}{g_{mcf}} g_{m2} g_{m3} C_m}{\left(\frac{C_m + 2C_q}{C_q}\right) C_2 C_3} \tag{3}$$

To maintain the phase margin about 60 degrees, the MQ pole must be placed above the UGF by a factor of two with low $Q$ approximately equal to 5. To avoid the complex poles causing unstable, the MQ pole must be set at half the nature frequency at least to effectively reduce the loop gain. Since the magnitude rolls off at a rate of -20dB/dec after the dominant pole $P_{don}$ and at an increased rate of -40dB/dec after the MQ pole, there is at least 18dB margin for the complex poles with the same Q value compared to the previous designs. In other words, the requirement of the minimized load current can be reduced to about 50μA. The compensation capacitors $C_m$ and $C_q$ can be obtained as expressed

in (4). The MQ pole and the complex pair contribute about 30 degree phase shift to the system and AZC zero is far away which can be neglected. Thus, the overall phase margin can be determined by (5).

$$C_m = 4g_{m1}\sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}},$$
$$C_q = 2g_{mcf}\sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}} \quad (4)$$

$$PM = 90^\circ - \tan^{-1}\left(\frac{UGF}{p_{MQ}}\right) - \tan^{-1}\left(\frac{\frac{UGF}{\omega_o}}{Q\left[1-\left(\frac{UGF}{\omega_o}\right)^2\right]}\right) \quad (5)$$
$$\approx 60^\circ$$

*2.2 Light to Medium Load Current (i.e. the transconductance of the last stage is little larger than that of the second stage):*

As load current is increased from light to medium, the MQ pole will slightly be moved toward the origin due to the slight increase of resistance $R_{AZC}$ by adaptive zero compensation technique. The complex poles are further moved to higher frequency and contribute no phase shift to the system. The frequency response of the loop gain at medium loads is shown in Fig. 4(b). The poles locations are shown in (6). Thus, the overall phase margin can be determined by (7) and approximately equal to 60 degrees.

$$p_{MQ} = \frac{1}{\left(\frac{1}{g_{mcf}} + R_{AZC}\right)C_q},$$
$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}}{C_2C_3}}, \quad Q = \sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}}\frac{g_{m2}}{C_{gd}} \quad (6)$$

$$PM = 90^\circ - \tan^{-1}\left(\frac{UGF}{p_{MQ}}\right) \approx 60^\circ \quad (7)$$

*2.3 Medium to Heavy Load Current (i.e. the transconductance of the last stage is much larger than that of the second stage):*

As load current is further increased to approach heavy load current, the MQ pole as shown in (8) will be moved before the UGF due to the increased output reactance $g_3$ and the increased resistance $R_{AZC}$. The adaptive compensation zero $z_{AZC}$ in (8) will be moved closely toward the UGF to compensate the phase loss owing to the low-frequency MQ pole. Fig. 4(c) shows the positions of the MQ pole and the AZC zero. Thus, the phase margin can be maintained to a value of 60 degrees and expressed by (9):

$$p_{MQ} = \frac{g_{m2}g_{m3}C_m}{\left(\frac{1}{g_{mcf}} + R_{AZC}\right)g_{m2}g_{m3}C_qC_m + g_3C_2\left(C_m + 2C_q\right)},$$

$$z_{AZC} = \frac{1}{R_{AZC}C_q} \quad (8)$$

$$PM = 90^\circ - \tan^{-1}\left(\frac{UGF}{p_{MQ}}\right) + \tan^{-1}\left(\frac{UGF}{z_{AZC}}\right) \quad (9)$$
$$\approx 60^\circ$$

MQ pole acts two important roles in capacitor-free LDO. One is to slow down the movement of the output pole toward the origin at light loads due to the short path generated by the MQ pole. It is different to the Q-reduction technique in [1]. Besides, this pole also reduces the magnitude of loop gain when the complex pair occurs. Thus, the new LDO can tolerate a larger Q than that of the previous designs. Furthermore, the other characteristic of this MQ pole is to ensure the overall phase margin is maintained around 60 degrees to achieve faster response time over a wide load range.

# 3 Circuit Implementation of the LDO with the MQ and AZC techniques

In the schematic shown in Fig. 5, the basic structure of this LDO regulator consists of three gain stages. The first high gain stage is composed of transistors $M_1$~$M_6$ that convert a differential signal to a single-ended output. Transistors $M_7$~$M_{12}$ and resistor $R_B$ forms the second gain stage to achieve high PSR performance [13]. The diode-connected $M_{sw}$ is used to increase biasing current at heavy loads to achieve faster response owing to a higher second non-dominant at the gate of power p-type MOSFET. The third gain stage is common source power p-type MOSFET stage. The feedback resistors $R_{F1}$ and $R_{F2}$ form a shunt feedback to regulate the output voltage.

The MQ and AZC network, $C_q$ and $R_{AZC}$, is shown within dotted line in Fig. 5. The MQ capacitor $C_q$ is connected to a ground reference to maintain high PSR performance. The adaptive resistor $R_{AZC}$ acts an adaptive zero compensation formed by a PMOS operated in triode region controlled by the sensing network, $M_{SEN}$ and $R_{SEN}$.

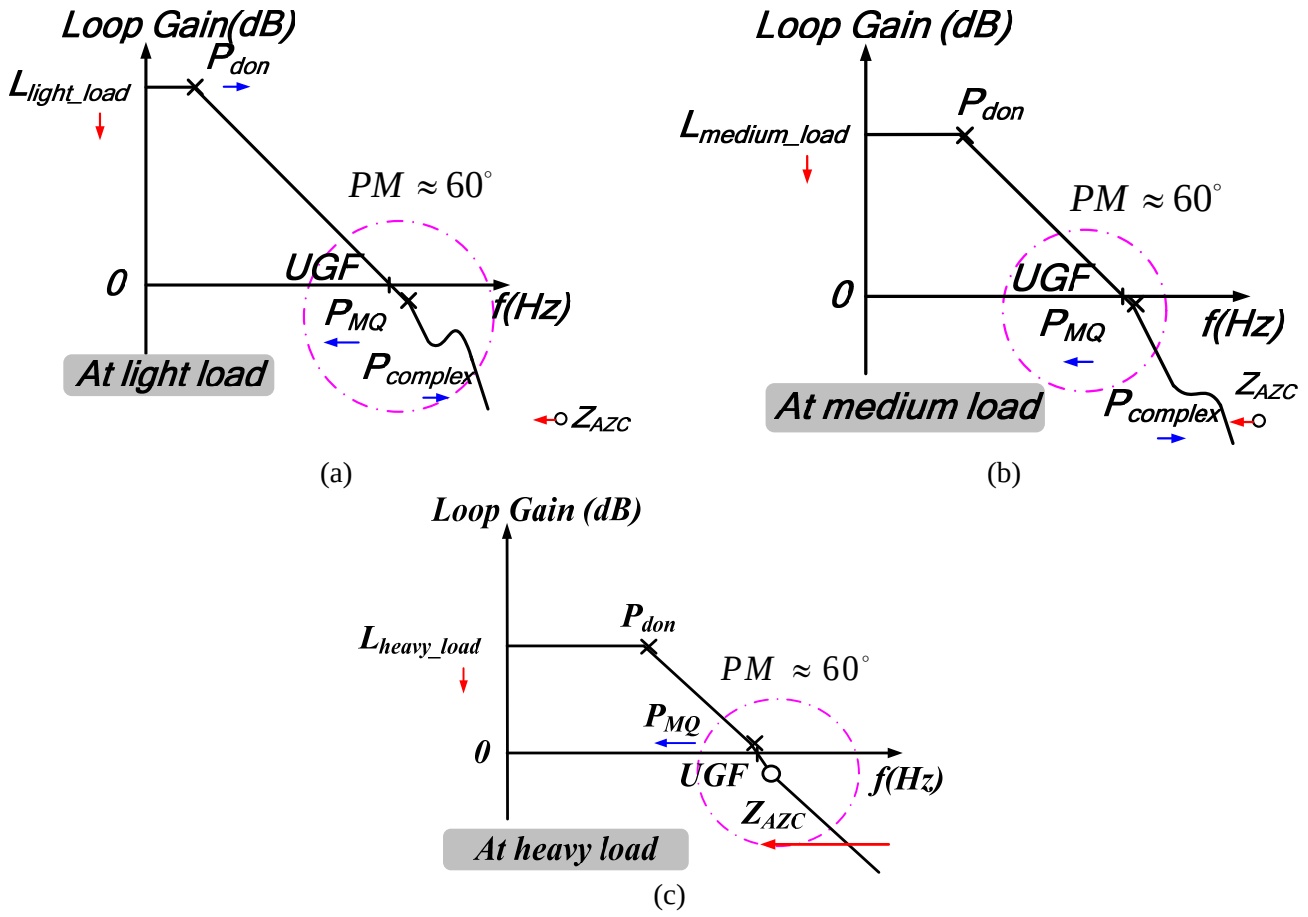


Fig. 4. The locations of poles and zero at different loads. (a) Poles and zero at ultra light loads. (b) Poles and zero at medium loads. (c) Poles and zero at heavy loads.

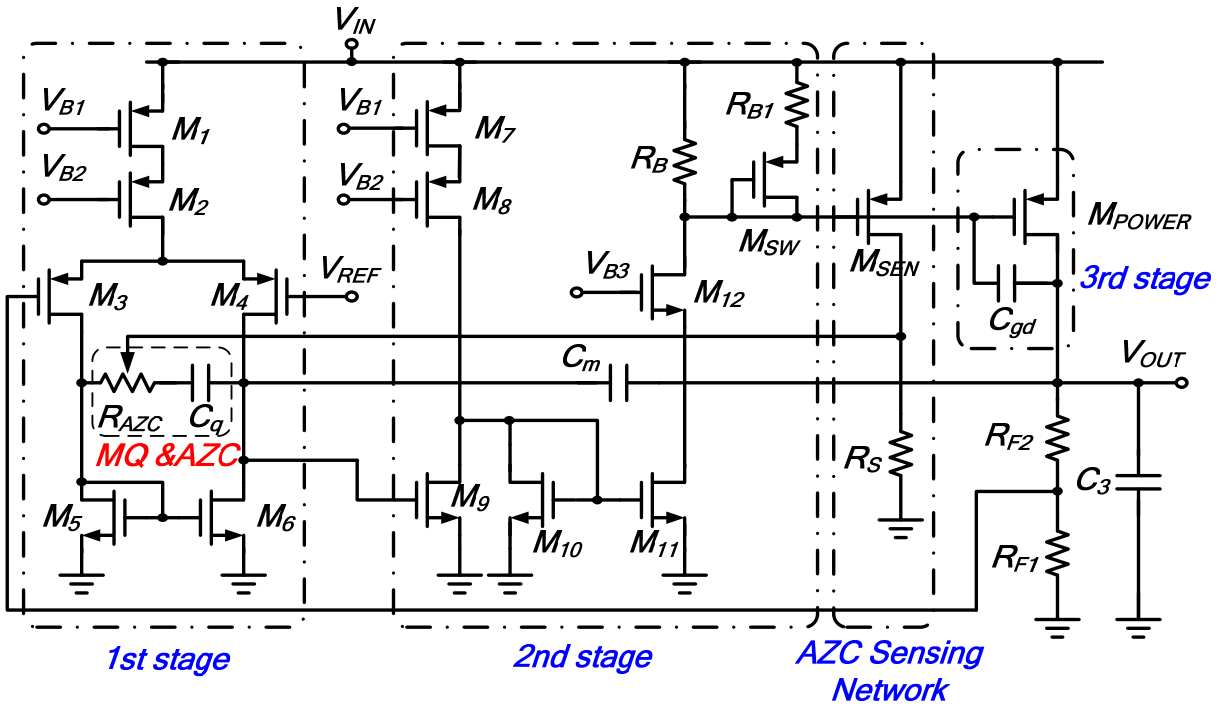


Fig. 5. The schematic of capacitor-free LDO regulator with the MQ and AZC techniques.

The frequency response of loop gain at different loads is shown in Fig. 6. The magnitude rolls off at a rate of -20dB/dec after the dominant pole $P_{don}$ and at a rate of -40dB/dec above the MQ pole. The UGF and PM always can be kept around 850 kHz and 60 degrees, respectively.

The frequency response of loop gain loop at different light loads is shown in Fig. 7. Without MQ technique, the minimum load current is about 1mA since the quality factor Q is relatively large at load current equal to 500μA. Besides, the complex poles are moved to right-half-plane at load current smaller than 100μA. With MQ technique, the minimum load limitation is greatly decreased to 50μA. Since there is minimum load restriction without MQ technique, the compensation capacitor $C_m$ must be large enough and the tranconductance $g_{m2}$ must be set small enough to ensure the stability. In this design, $C_m$ is 20 pF and $g_{m2}$ is 0.8mS without MQ technique. However, for the proposed LDO regulator with MQ technique, $C_m$ and $C_a$ are 5pF and 1.5pF, respectively. At this time, the requirement of the transconductance $g_{m2}$ of the second stage is 1.175mS.

The capacitor-free LDO regulator with MQ and AZC techniques was fabricated by TSMC 0.35μm 2P4M process. The input voltage range is from 3V to 5V and the output voltage is regulated to 2.8V. The load current range is from 50μA to 100mA. The specification of the proposed LDO with MQ and AZC technique is listed in Table I. The load parameter testing is under the condition with supply voltage 3V and load current ranged from 50μA to 100mA. The measured load regulation is about 20μV/mA. The load transient response from 50μA to 100mA is shown in Fig. 8(a). The output voltage variation is about 60mV with recovery time 2.5μs. The load transient response from 100mA to 50μA is shown in Fig. 8(b). The output voltage variation is about 80mV with recovery time about 4μs. The line parameter testing is under the condition with supply voltage ranged from 3V to 5V at load current equal to 100mA. The measured line regulation is about 3.3mV/V. The line transient response from 3V to 5V within 5μs is shown in Fig. 9(a). The output voltage variation is about 90mV. The line transient response from 5V to 3V within 5μs is shown in Fig. 9(b). The output voltage variation is about 110mV.

## 4 Experimental results

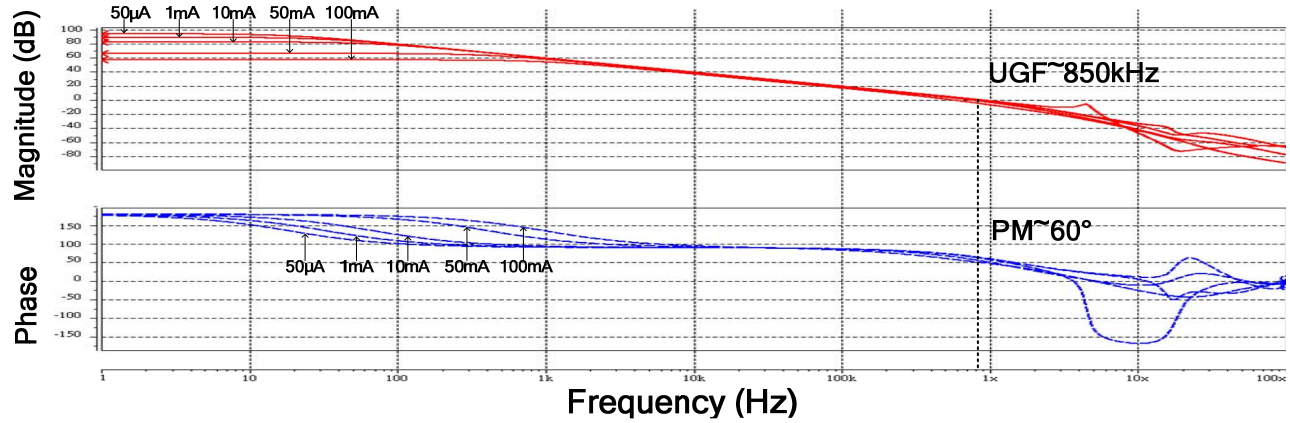


Fig. 6. Frequency response of loop gain at different loads.

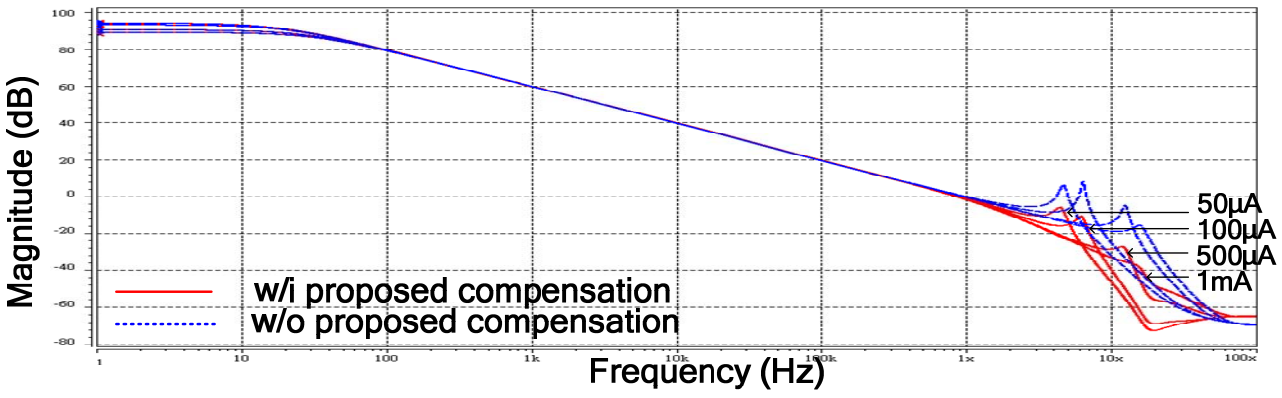


Fig. 7. The frequency peaking with and without the MQ compensation at different light loads.

Table I: Experimental results of the proposed LDO with the MQ and AZC techniques.

| | |
|---|---|
| Technology | TSMC 0.35μm 2P4M |
| Supply voltage $V_{in}$ | 3V~5V |
| Output voltage $V_{out}$ | 2.8V |
| Load range $I_{Load}$ | 50μA -100mA |
| Load Regulation | 20 $\mu V/mA$ @ $I_o$= 0.05-100mA |
| Line Regulation | *3.3 mV/V* @ $V_{in}$= 3~5V, $I_o$= 100mA |
| Load transient settling time | 2.5 $\mu s$ @ $I_o$= 50μA-100mA<br>4 $\mu s$ @ $I_o$= 100mA-50μA |
| Load transient output voltage variation | 60 *mV* @ $I_o$= 50μA-100mA<br>80 *mV* @ $I_o$= 100mA-50μA |
| Power Consumption | 170$\mu A$ @ $V_{in}$ =3V |
| Active Area | 570 × 600$\mu m^2$ |

From Table II, it is obvious the phase margin is maintained around 60 degree. According to the comparison listed in Table III, with the similar compensation capacitor size the proposed LDO has reduced requirement of minimum load current about 50μA and nearly constant phase margin equal to 60 degrees. Furthermore, a higher PSR bandwidth is achieved by our proposed LDO compared to the Q-reduction technique [1] in Fig. 10. The PSR bandwidth is improved from 60Hz to 5kHz.

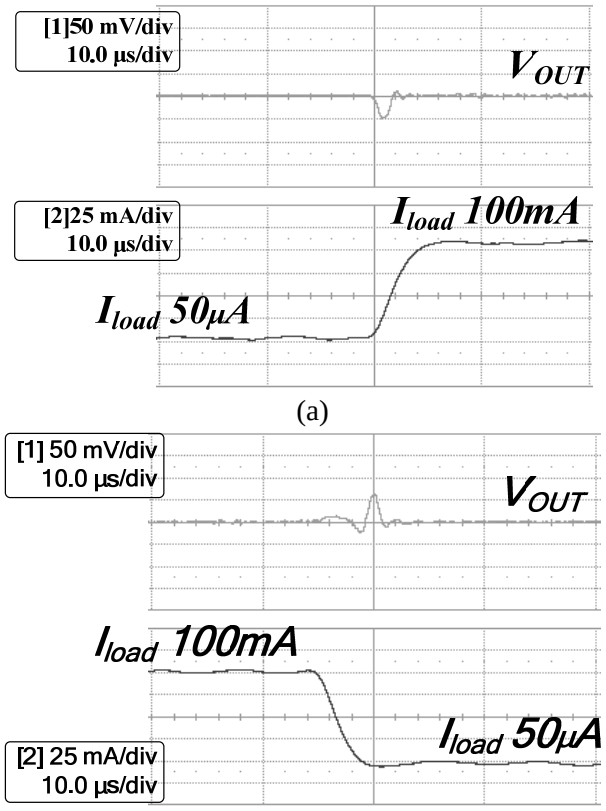


Fig. 8. Load transient response: Load current $I_{load}$ changes (a) from 50μA to 100mA (b) from 100mA to 50μA.

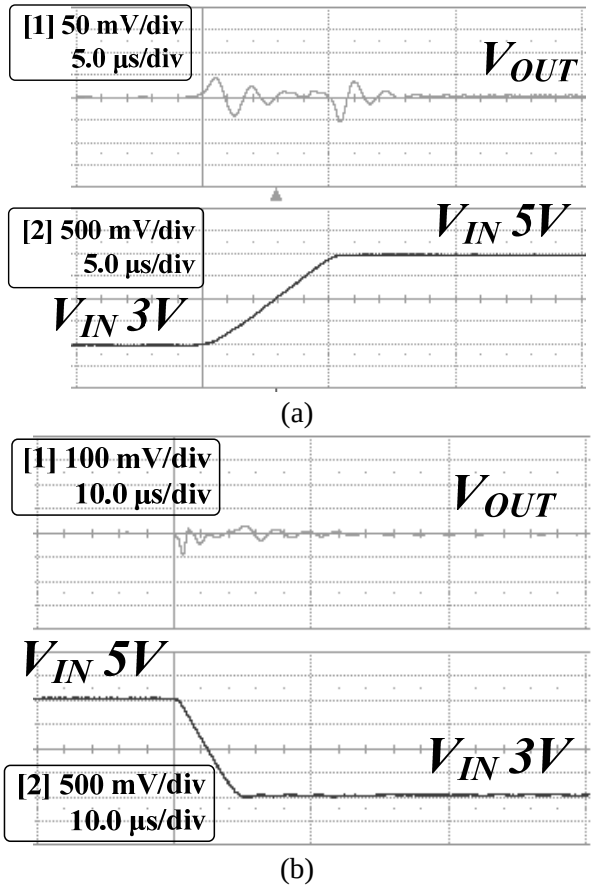


Fig. 9. Line transient response: Input voltage $V_{IN}$ changes (a) from 3V to 5V (b) from 5V to 3V.

## 5 Conclusion

A capacitor-free LDO regulator with the MQ and AZC techniques is proposed in this paper. Light load efficiency and fast transient response time are improved since only 50μA minimized load current is needed and 60 degrees is always maintained in the proposed LDO regulator. Furthermore, the

proposed LDO regulator has higher PSR bandwidth compared to the Q-reduction technique [1]. The capacitor-free LDO regulator with the MQ and AZC techniques was fabricated in TSMC 0.35μm 2P4M CMOS process and shown in Fig. 11 with small compensation capacitors 5pF and 1.5pF. Experimental results demonstrate that the minimum load is 50μA and transient response time is smaller than 4μs.

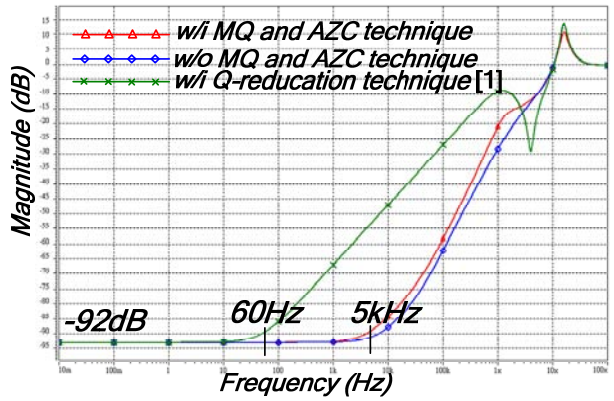


Fig. 10. PSR performance for different compensation techniques at load current $I_{load}$=1mA.

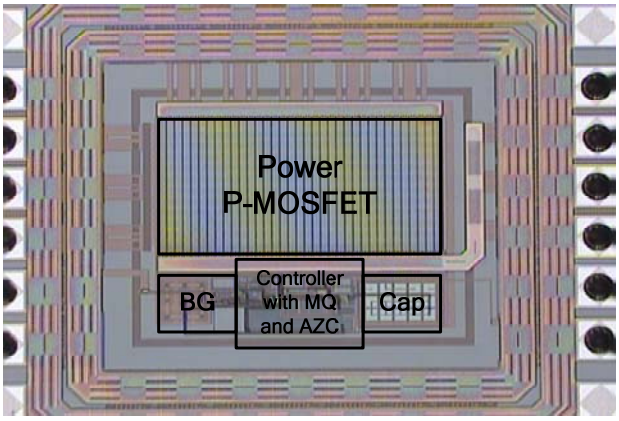


Fig. 11. Chip micrograph.

*Acknowledgment*

The authors wish to thank to Chunghwa Picture Tubes, LTD for their help. This research is also supported by the National Science Council, Taiwan, R.O.C. under Grant NSC 96-2221-E-009-240.

Table II: Poles and zero locations and phase margin at different loads.

| *Load* | $P_{don}$ | $P_{MQ}$ | $Z_{AZC}$ | *PM* |
|---|---|---|---|---|
| **50 μA** | 19 Hz | 1.8 MHz | 11.4 MHz | **61.3°** |
| 1 mA | 34 Hz | 1.7 MHz | 11.3 MHz | **63.7°** |
| 10 mA | 70 Hz | 1.6 MHz | 11.1 MHz | **63.6°** |
| 50 mA | 422 Hz | 1.3 MHz | 9.1 MHz | **58.6°** |
| 100 mA | 1 kHz | 560 kHz | 1.1 MHz | **58.5°** |
| | ↗ | ↘ | ↘ | × |

Table III: Comparison of four different capacitor-free LDO regulators.

| | DFCFC [5] | Q-Reduction [1] | This work w/o MQ and AZC | This work |
|---|---|---|---|---|
| Compensation Capacitor | $C_{m1}$+ $C_{m2}$=5pF | $C_{m1}$+ $C_{cf}$=6pF | $C_m$ =5pF | $C_m$+ $C_q$=6.5pF |
| Minimum load | 100 μA -10mA | 100 μA | 1 mA | 50 μA |
| UGF | ~ 500 kHz | 660 kHz | 850 kHz | 850 kHz |
| Phase Margin | 90° | 90° | 85°-63° | **60°** |

*References:*

[1] S. K. Lau, P. K. T Mok, K. N. Leung, "A low-dropout regulator for SoC with Q-reduction", *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 658-664, Mar. 2007.

[2] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, pp. 36-44, Jan. 1998.

[3] G. A. Rincon-Mora and P. E. Allen, "Optimized frequency-shaping circuit topologies for LDOs," *IEEE Trans. Circuit and Systems II*, vol. 45, pp. 703-708, June 1998.

[4] C. K. Chava and J. Silva-Martinez, "A frequency compensation scheme for LDO voltage regulators," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 6, pp. 1041-1050, Jun. 2004.

[5] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691-1702, Oct. 2003.
[6] G. A. Rincon-Mora, "Active capacitor multiplier in miller-compensated circuits," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 26-32, Jan. 2000.
[7] R. J. Milliken, J. Silva-Martínez, E. Sánchez-Sinencio, "Full on-chip CMOS low-dropout voltage regulator," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 9, pp. 1879-1890, Sep. 2007.
[8] K. N. Leung and P. K. T. Mok, "Analysis of multi-stage amplifier—frequency compensation," *IEEE Trans. Circuits Syst. I*, vol. 48, no. 9, pp. 1041-1056, Sep. 2001.
[9] K. N. Leung and P. K. T. Mok, "Nested Miller compensation in low power CMOS design," *IEEE Trans. Circuits Syst. II*, vol. 48, no. 4, pp. 388-394, Apr. 2001.
[10] G. Palumbo and S. Pennisi, "Design methodology and advances in nested-Miller compensation," *IEEE Trans. Circuits Syst. I*, vol. 49, no. 7, pp. 893-903, Jul. 2002.
[11] X. Fan, C. Misgra and E. Sanchez-Sinencio, "Single Miller capacitor frequency compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, March 2005.
[12] K. N. Leung, P. K. T. Mok, W. H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, pp. 221-230, Feb. 2000.
[13] K. Wong and D. Evans, "A 150mA low noise, high PSRR low-dropout linear regulator in 0.13µm technology for RF SoC applications", *IEEE European Solid-State Circuits Conference*, Sep. 2006, pp. 532-535.
[14] V. Gupta, and G. A. Rincón-Mora, "A low dropout, CMOS regulator with high PSR over wideband frequencies" *IEEE International Symposium on Circuits and Systems*, May 2005, vol. 5, pp. 4245-4248.
[15] S. K. Hoon, S. Chen, F. Maloberti, J. Chen, and B. Aravind, "A low noise, high power supply rejection low dropout regulator for wireless system-on-chip applications", *IEEE Custom Integrated Circuits Conference,* Sept. 2005, pp. 759-762.