A 2.4-GHz ISM Band Delta-Sigma Fractional-N Frequency Synthesizer with Automatic Calibration Technique

Shiwei Cheng, Ke Zhang, Shengguo Cao, Xiaofang Zhou*, Dian Zhou
State Key Laboratory of ASIC & System
Fudan University
CHINA
chengshiwei@fudan.edu.cn, kezhang@fudan.edu.cn, shengguocao@fudan.edu.cn
xiaofangzhou@fudan.edu.cn, zhoud@fudan.edu.cn

Abstract: - In the paper, a programmable phase-locked loop (PLL) based ISM band fractional-N frequency synthesizer, commonly used in wireless communication system, is presented. The third order error-feedback Delta-Sigma modulator and high linearity offset phase frequency detector (PFD)/ Charge Pump (CP) are adopted to reduce close-in phase noise due to $\Delta\Sigma$ quantization noise folding. Automatic calibration technique is also introduced to select the optimal frequency sub-band of voltage controlled oscillator (VCO) automatically through process, voltage and temperature (PVT) variation. The Synthesizer is designed in UMC .18um RF process and has a die size of 1.5mm*2.3mm. The measured phase noise is -112 dBc/Hz at 1 MHz offset.

Key-Words: - Fractional –N Frequency Synthesizer, Delta-Sigma Modulation, Quantization noise folding, Automatic Calibration Technique

1 Introduction

The recent boom in the wireless telecommunication systems has resulted in great demand in high performance, low power, and low cost, single chip RF transceivers [1] [2]. In the wireless RF transceiver, frequency synthesizer (FS) affords a stable RF frequency to up convert modulated base-band signals to RF frequency in the transmitter or down convert the received RF signal to base band signal in the receiver. Nowdays software radio (SDR) design requires most circuit blocks to be configurable to realize multiple communication standards [3]. Frequency synthesizer needs to cover multiple frequency bands and switch fast to satisfy different carrier frequency and channel width, modulation mode and phase noise performance of multiple communication standards. Except from high frequency resolution, phase noise and spurious tone deteriorate performance of transceiver. So design low cost, high phase noise performance frequency synthesizer is one important aspect of wireless transceiver circuit design [4] [5].

Frequency synthesizer is phase-locked loop (PLL) circuit that locks the frequency from voltage controlled oscillator (VCO) with the reference frequency. The frequency synthesizer can be either integer-N or fractional-N PLL [6] [7]. The integer-N frequency synthesizer can only generate frequency integer times of reference frequency: $f_{out} = N * f_{ref}$. In order to generate fine frequency steps, low reference frequency must be adopted. However, the adoption deteriorates the loop dynamic performance. The loop bandwidth is normally set to be less than 1/10 of reference frequency for stability consideration, while most communication standards always need not only high frequency resolution but also fast frequency switching, especially in frequency hopping systems. And the low reference frequency will make reference spur locate in the in neighbor channels to low the receiving sensitivity and increase bit error ratio (BER) in receiver. The integer-N frequency synthesizers suffer from trade off between fast dynamics, high frequency resolution and phase noise performance.

Fractional-N frequency synthesizer circumvents this problem by allowing fractional divide ratio [8] [9] [10]. The output frequency steps can be much smaller than the reference frequency: $f_{out} = N.F * f_{ref}$. In a fractional-N frequency synthesizer, the multiple mode frequency divider averages many integer divider cycles over time to get an effective fractional divider ratio. A simple accumulator with an overflow can be used as a fractional modulator to get any fractional number between 0 and 1, but this method generates periodic fixed tone due to periodic operation of the

accumulator. The fractional spurious tone will locate in the loop bandwidth and can not be filtered by the low pass loop filter. $\Delta\Sigma$ modulator is adopted to randomize the integer divider sequence to get the fractional number while shaping the quantization noise to high frequency band. The quantization noise is then filtered by the low-pass response of frequency synthesizer [11] [12]. Fractional-N frequency synthesizer can generate fine frequency resolution with high reference frequency and wide loop bandwidth; however loop bandwidth is still limited by $\Delta\Sigma$ quantization noise and fractional spur depending on phase noise requirement.

The commonly used transmitter consists of a digital base-band processor and two digital to analog converter (ADC), single-side-band select mixer to up convert the modulated signals to carrier frequency. However, this architecture suffers from mismatch in the two branches and inaccuracy arising from I/Q quadrature phase. In our design, the transmitter based on indirect frequency synthesizer modulation [13], as shown in Fig.1, can be adopted because of the constant envelope of GFSK/GMSK modulation. In this transmitter, a $\Delta\Sigma$ modulator of sufficient resolution not only sets the centre frequency of channel but also modulates the frequency of oscillation depending on the modulated data. The digital-to-analog converters (DAC) and mixers are eliminated and only one oscillator is required. By analogy to the familiar digital-to-analog converter, this is a digital-to-frequency/phase converter. Non-linear PA can also be used to amplify the constant envelope of the modulated carrier wave to achieve high PAE [14]. This transmitter consumes low power and this architecture is often used in the phase modulation in polar transmitter to achieve multi-mode transmitter.

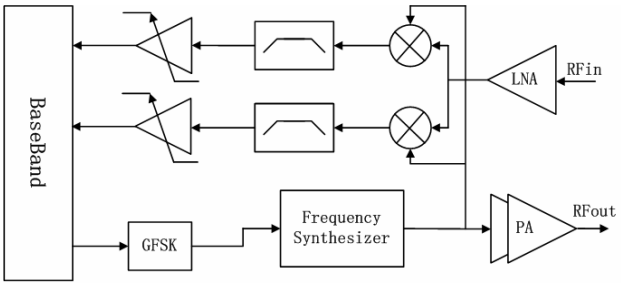

Fig.1 Block diagram of implemented RF transceiver (indirect PLL modulation transmitter)

In this transmitter, wide bandwidth is needed to achieve high data rate. Digital pre-compensation surfers from mismatch between digital compensation circuit and analog low pass filter [13]. Wide loop bandwidth not only reduces the VCO phase noise arising from 1/f and $1/f^3$ noise but also is beneficial for in-loop modulation.

Actually the integer stream is generated by digital circuit and is not random, so the charge pump current generated due to $\Delta\Sigma$ quantization noise is predictable. The current can be expressed by:

$$Q_{cp}[n] = I_{cp} * T_{VCO} * \sum_{k=n0}^{n} e_Q[k] \qquad (1)$$

I_{cp} is charge pump current; T_{VCO} is the period of VCO (when the PLL is locked, T_{VCO} can be treated unchanged); $e_Q[k]$ is the quantization noise generated by $\Delta\Sigma$ modulator.

DAC based quantization noise cancellation method are widely adopted [15] [16] [17] [18] [19]. The cancellation DAC injects the current into the loop filter to compensate the quantization current. If $\Delta\Sigma$ quantization noise is cancelled accurately, the phase noise performance of the fractional-N frequency synthesizer behaves like the integer-N frequency synthesizer, irrespective of the order of $\Delta\Sigma$ modulator [16]. However, non-ideal factors such as PFD/CP nonlinearity, DAC resolution, ratio-dependent jitter, requantization, and DAC/CP gain mismatching deteriorate the performance of noise cancellation method, leaving residual spurious tones.

A high level block diagram of the implement PLL is shown in Fig.2. In this design, PFD/DAC structure [20] is adopted to avoid the mismatch mentioned in the DAC based cancellation technique.

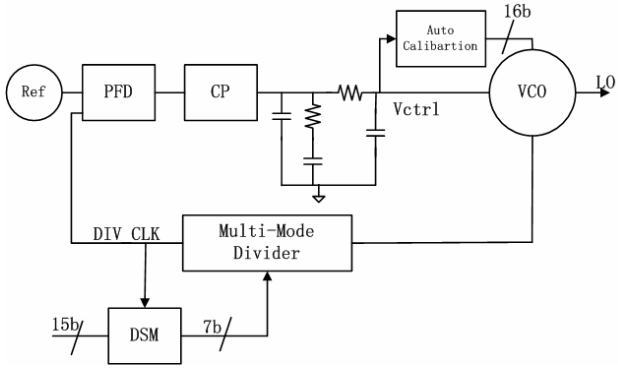

Fig.2 High level block diagram of $\Delta\Sigma$ PLL

The details of the PLL are described throughout the remainder of the paper. Section II describes Voltage Controlled Oscillator (VCO), automatic

calibration technique, third order error-feedback sigma-delta modulator, and PFD/CP linearization technique respectively. Section III presents the measured results.

2 Synthesize Architecture and Circuit Design

The divide ratio in the fractional-N frequency synthesizer is always changing, which makes the loop gain time varying. However, the loop bandwidth is always an order of magnitude lower than the reference frequency and divide ratio variation is much smaller than the average divide ratio. The loop can be treated as time invariant and the nominal divide ratio can be used [21]. The loop of PLL can be represented by time average transfer function:

$$H_{close-loop}(s) = N_{nom} \frac{K_{PD} \bullet I_{CP} \bullet T_{lpf}(s) \bullet K_{VCO}}{N_{nom} + K_{PD} \bullet I_{CP} \bullet T_{lpf}(s) \bullet K_{VCO}} \qquad (2)$$

K_{PD} , I_{CP} , $T_{lpf}(s)$, K_{vco} are the phase frequency detector gain, the charge pump current, low pass loop filter transfer function and the VCO gain.
The loop bandwidth can be expressed by

$$BW = \frac{K_{VCO} \bullet I_{CP} \bullet R_S}{2\pi N_{nom}} \qquad (3)$$

R_S is the value of the resistor to provide a zero in the loop filter.

In this design, the charge pump current is 640uA; the reference frequency is 16MHz; and the loop bandwidth is set to 500 KHz to allow for in-loop modulation. PFD/DAC structure is used to suppress the quantization noise of $\Delta\Sigma$ modulator.

2.1 VCO

Fig.3 shows a schematic of the LC VCO, which is based on pMOS and nMOS cross-coupled pairs with an LC resonant tank. Combination of cross-coupled NMOS and PMOS transistors is utilized to compensate the loss of the LC tank [22]. The cross-coupled pair structure reduce the power consumption and increase the output wave swing, compared to only NMOS or PMOS pair due to current reuse scheme. The LC tank consists of an on-chip spiral inductor with patterned ground shield as well as diode varactors implemented with p+ diffusion in N-well.

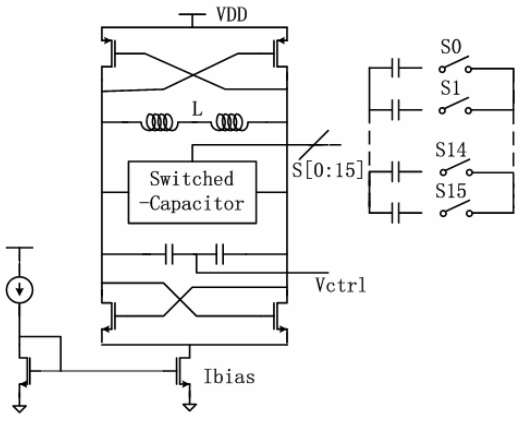

Fig.3 Schematic of VCO

Based on Lesson heuristic Phase noise formula [23], the Q value of inductor must be high for better phase noise performance. In this design, the inductor is generated by using ASITIC, and the Q value of inductor is more than 8, when the oscillation frequency is 5.0 GHz. The characteristic curve of the symmetrical inductor is shown in Fig.4 and Fig.5. As shown in Fig.6, the varator always in accumulation region and depletion region, and never in inversion region, has good monotony. The varactor has good linearity when the gate voltage varies from 0.8V to 1.2V.

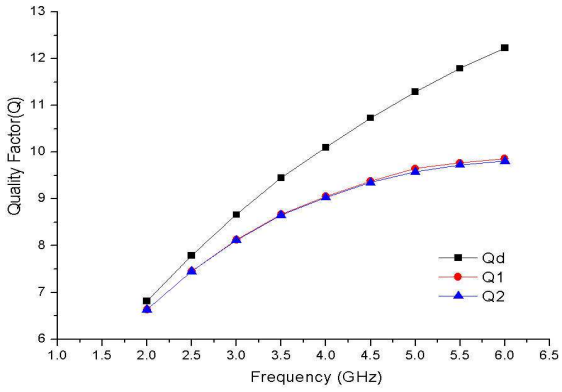

Fig.4 Q value of inductor versus frequency

In order to cover wide tuning range for accommodating process, voltage and temperature (PVT) variation and low supply voltage, the high VCO gain Kvco is necessary. However, high K_{vco} will degrade the phase noise performance and spurious tone severely, so discrete tuning scheme is added to enlarge tuning range and still keep low K_{vco} [24]. In this design, a 16-bit digitally controlled MIM capacitor array is parallel with the resonant tank to achieve large frequency tuning range and to

overcome process variation and temperature changes.

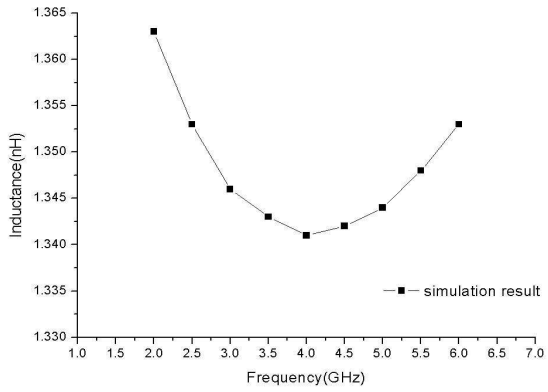

Fig.5 Value of inductor versus frequency

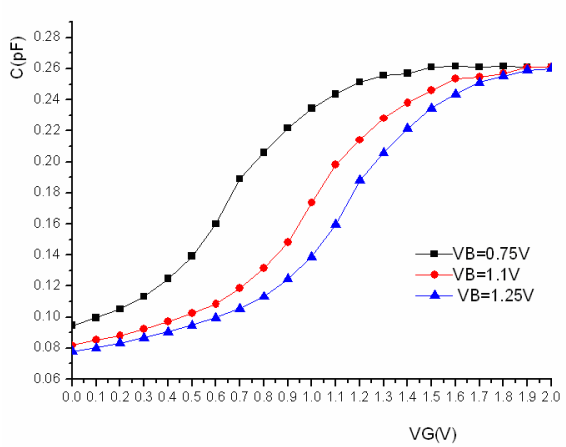

Fig.6 Simulated characteristic of Varactor

The VCO gain is 40MHz/V. The control voltage of fine varactor is tuned from 0.8V to 1.2V, and generation scheme of the controlled bits of switched capacitors is discussed in section 2.2. To decrease phase noise due to switching activities of MIM capacitors, a thermo-decoder is added to decode the binary weighted encode to thermometer encode. Each MIM capacitors are the same value, and every time only one bit MIM capacitor is switched in or out of the LC tank. And this scheme will not change the value of the capacitor abruptly and not disturb VCO oscillating.

The output frequency of VCO is 4.8GHz, and then is divided by two to generate the quadrature 2.4GHz RF frequency. This divide-by-two strategy suffers less I/Q mismatch and a 4.8GHz inductor has high Q value to improve phase noise performance and occupies less area.

2.2 Self-Calibration Technique

The continuous and discrete frequency tuning scheme mentioned in section 2.1 needs a circuit to decide the optimum control bits of switched MIM capacitors. This time cost will be added to intrinsic PLL settling or locking time and low the response of PLL switching activities. There are two approaches to tune frequency range of wideband VCO in a PLL locking operation. One approach is to program the control word externally by memory. Once PLL is fabricated, VCO frequency characteristic curve is got by carefully test operation. When the out frequency of PLL needs to be changed, the controlled bits can be immediately set by using look-up table method. This direct adjusting method can change from one frequency to another frequency and select the optimum frequency band immediately, and is especially useful in communication systems which fast frequency switching is needed. But the loop can not decide the optimum frequency band by itself and needs to be adjusted externally. Another approach is to adaptively change control bits by auto-calibration circuit in the PLL loop [24] [25].Depend on whether the loop is open or closed ,the calibration method can be grouped into open-loop VCO calibration technique or closed-loop VCO calibration technique. The open-loop calibration method disconnects the loop at the loop filter and V_{ctrl} is connected to the reference voltage V_{ref}. In this technique, the counters must accumulate a sufficient amount of counts to ensure the calibration precision and an additional time is need for stabling out put frequency when the calibration is finished and the loop is closed again to fine-tune VCO control voltage. So this calibration method may be low.

In this paper, the close-loop auto-calibration technique is implemented. The auto-calibration process operates in the close-loop manner as shown in Fig.2, which doesn't need to open the loop in the calibration process. As in the normal PLL locking process, PFD checks the phase difference of reference clock and clock from Multi-Mode Divider, and then Charge Pump charges or discharges the loop filter depend on pulse widths of up/down signals, which is generated from PFD, to tune the control voltage of VCO. At the same time, the control voltage V_{ctrl} is also fed into the calibration circuit and is compared to a predefined voltage range (between V_low and V_high). If V_{ctrl} is outside this voltage range excess a specific time, the PLL is considered to be unable to lock properly and calibration circuit starts to work. The unlock situation indicates the VCO sub-band fails to cover the desired frequency. Another VCO sub-band

should be chosen by changing the switched MIM capacitors array in LC tank.

The calibration circuit consists of two comparators, a calibration clock generation circuit, and a counter, shown in Fig.7. The comparators determine whether the control voltage is between V_low and V_high. If not, the Up or Down Signal is assigned. The counter is to count up or down the control bits of switched capacitors based on the Up or Down Signal. After system reset, the counter is set to the middle of the range of sub-bands in order to search for any frequency band immediately. The clock generation circuit is used to generate the clock of the counter. The output clock is generated by dividing the reference clock. The counter clock must be chosen carefully. If the clock is too low, it will low the whole locking process, while the counter clock is high, the loop will oscillate and the control voltage V_{ctrl} will change all the time and can not lock to the locking control voltage.

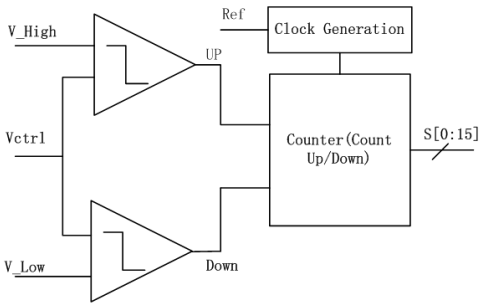

Fig.7 Auto Calibration Circuit

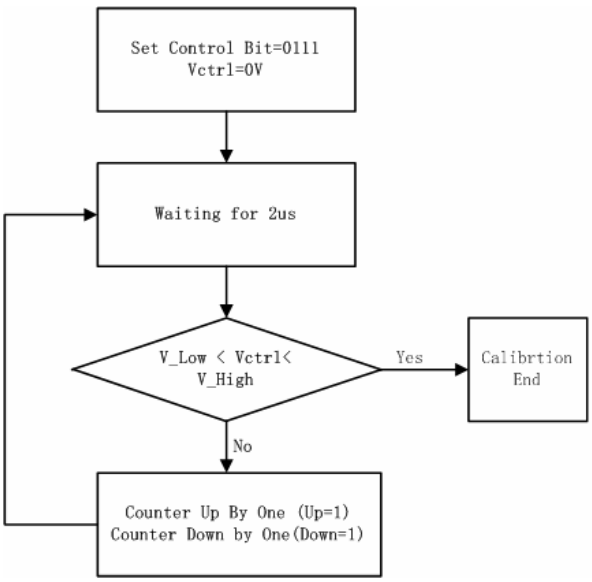

Fig.8 Auto calibration algorithm

When the loop is locked, the control voltage locates between V_low and V_high, and control bits are locked to a certain number. The locking and auto calibration algorithm is shown in Fig.8, and the simulated locking process is shown in Fig.9.

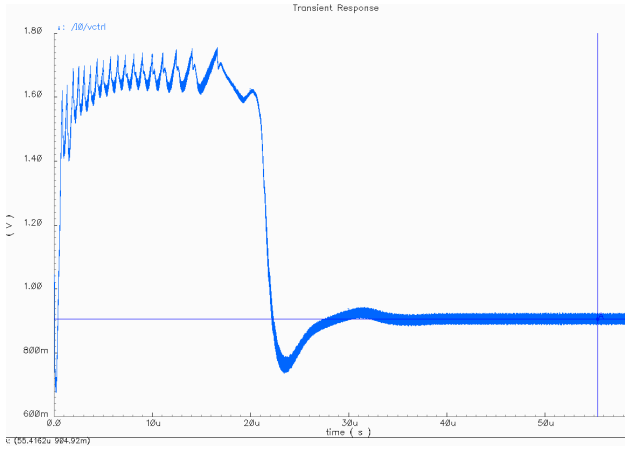

Fig.9 Simulated transient locking process

2.3 Offset Phase Frequency Detector (PFD) and Charge Pump (CP)

Nonlinearity of PFD/CP such as dead zone in PFD, CP static gain mismatch, CP dynamic mismatch is major contributor of in-band Fractional-N noise. In addition, the nonlinearity also causes high frequency $\Delta\Sigma$ quantization noise to fold back to low frequency offset to increase in band noise floor. In this design, an offset tri-state PFD [26], shown in Fig.10, is adopted. Compared to traditional tri-state PFD, the structure achieves only the down pulse varying the pulse width and the up pulse width keeping constant when PLL is in lock condition. The delay in the reset path of PFD is programmable to adapt to PVT variation. Large reset pulse is also avoided to induce the phase noise introduced by charge pump current. The reset delay in this design is set to 3ns.

A cascade current source is used in the discharge branch to improve the output impedance. However, it is not adopted in the upper branch to ensure large output voltage swing, as shown in Fig.11. Up/Down current matching is not necessary in this design because the down current source varies the current pulse width. Additionally, resistive degeneration scheme is employed to reduce the magnitude of current noise. The resistor creates a feedback loop in the current source to lowering the drain current noise in the charge pump [20]. The output noise power is

$$\overline{i}_{noise}^2 = \left| \frac{1}{1+gm_1R+\frac{R}{r_{o1}}} \right|^2 \bullet \overline{i}_{gn}^2 \quad A^2/Hz \qquad (4)$$

$\overline{i}_{gn}^2$ is drain current noise PSD of the current source, r_{o1} is the AC small signal output impedance , gm_1 is tranconductance of current source , R is the value of the degenerative resistor.

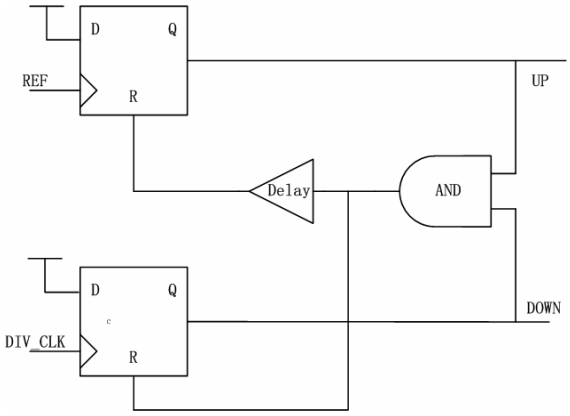

Fig.10 Offset tri-state PFD

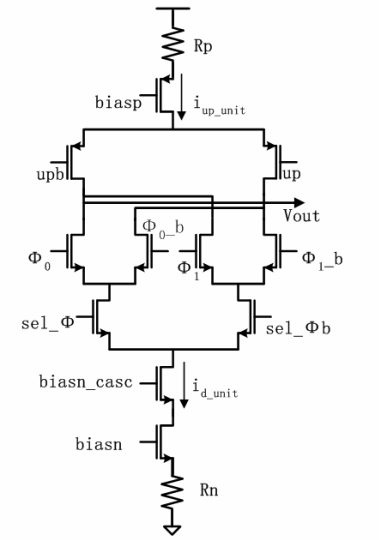

Fig.11 Resistive Degenerated Cascade Charge Pump

2.4 Multi-Mode Divider

The Multi-Mode Divider (MMD) consists of seven divide by 2/3 stages as shown in Fig.12 and Fig.13. The modulus of MMD is controlled by the output of $\Delta\Sigma$ modulator. The instantaneous frequency divider ratio can be any integer value between 128 and 255.The multi-mode divider operates as follow. Once in a division period, the signal "Mod_in" will propagates up in the chain from the last 2/3 divide cell. If this active mode signal "Mod_in" enables the 2/3 cell divide by 3, provided the input p is set to "1". The programmable divide ratio can be expressed

$$T_{OUT} = 2^n \bullet T_{VCO} + 2^{n-1} \bullet T_{VCO} \bullet p_{n-1} + 2^{n-2} \bullet T_{VCO} \bullet p_{n-2}$$
$$+ \cdots + 2 \bullet T_{VCO} \bullet p1 + T_{VCO} \bullet p0$$
$$= (2^n + 2^{n-1} \bullet p_{n-1} + \cdots + p0) \bullet T_{VCO}$$

$p_n, p_{n-1} \cdots p_1, p_0$ is the input bit to decide whether this 2/3 divide cell is able to divide by 3; n is the stages of the multi mode divider.

The first three highest divide by 2/3 stages are implemented with current-mode logic (CML) and the remaining stages are implemented with standard CMOS logic. Level conversion stages interface the differential logic levels of CML and 1.8V CMOS logic. Each CML stages are designed to operate to its self–oscillation frequency [27] and the current consumption decreases every stage to decrease power consumption.

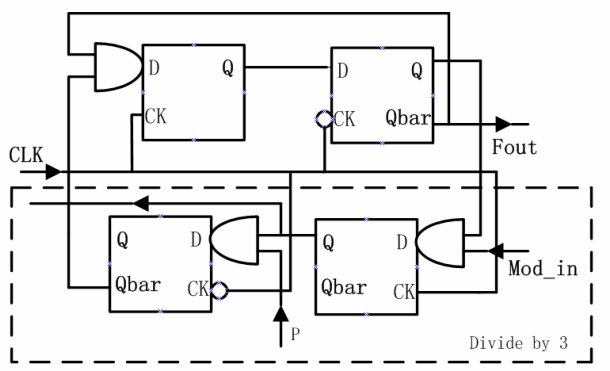

Fig.12 Divide by 2/3 stage

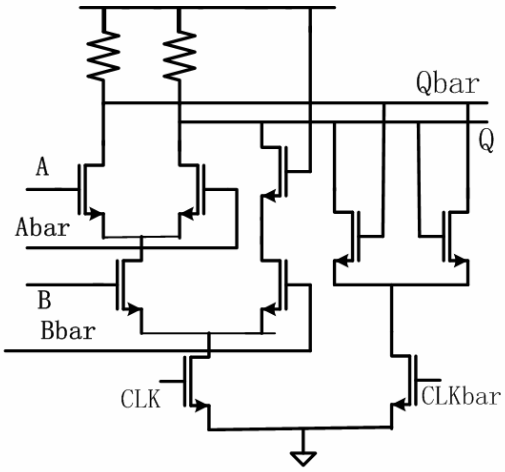

Fig.13 Current Mode Logic implementation of latch with AND gate

2.5 Low Pass Loop Filter

The loop filter is implemented with passive RC network as shown in Fig.14. All capacitors are nMOS gate capacitors with Drain and Source connected to ground. Control bits are added to adjust the value of resistors and capacitors to make loop bandwidth constant through PVT variation. The R3 and C3 filter the quantization noise of ΔΣ modulator. The phase margin of loop is 60°.

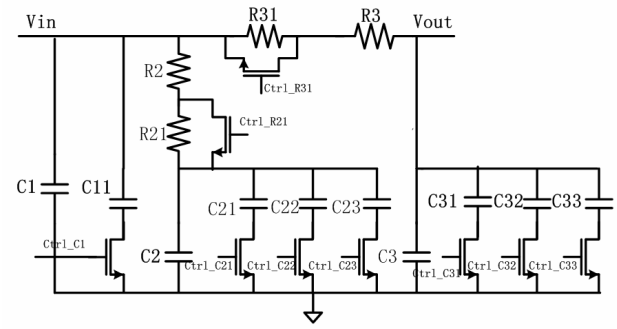

Fig.14 Low Pass Loop Filter

The four order loop filter transfer function is

$$T_{lpf} = \frac{sT_2 + 1}{SC_1(sT_2+1)(sT_3+1) + sC_2(ST_3+1) + sC_3(ST_2+1)}$$

$$T_2 = R_2C_2$$

$$T_3 = R_3C_3 \qquad (5)$$

The problem with fourth-order loop design is maintaining the required loop natural frequency and phase margin when adding extra attenuation [28]. Extra attenuation is implemented by adding an extra frequency pole. The simulated bode plot of the loop is shown in Fig.15.The added pole can attenuate the reference spur -20dB. Wide bandwidth decreases the value of the capacitor and is beneficial for all the blocks to be integrated on the chip.

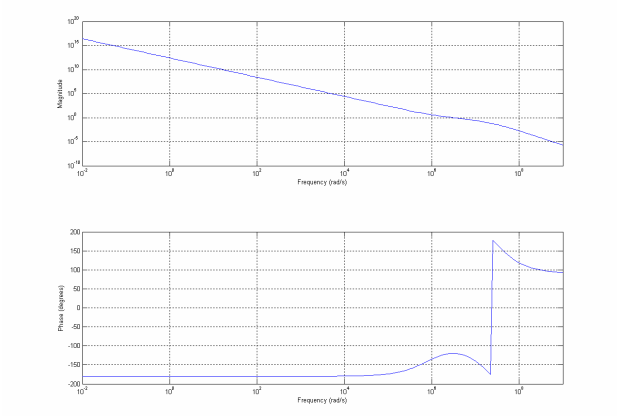

Fig.15 Bode plot of the loop

2.6 Multi-bit Error-feedback ΔΣ modulator

For the ΔΣ modulators in fractional-N frequency synthesizers, two major architectures have been proposed. One is single-stage high-order modulator, and another is multi-stage cascaded modulator, which is also is called MASH modulator. Single-stage high-order ΔΣ modulators effectively push the quantization noise to high frequency offset and immune to non-linearity of the PLL due to having a two-level output, however suffer the stability problem. The input of the modulator is limited to avoid overloading the range of the quantizer. MASH 1-1-1 is implemented by cascading the first-order modulators and stables over the whole input range. Without having feedback and feedforward paths, the MASH modulator is easy to be implemented and also can be pipelined to work fast. But the wide range output integer streams induce high frequency jitter at the PFD output and also incur quantization noise folding due to PFD/CP nonlinearity [11] [26] [29]. The error feedback sigma delta modulator modifies the Butterworth filter in the feedback path to shape the quantization noise to high frequency band and restrain high frequency noise, however still stables over the whole input range, which is shown in Fig.16.The output of the error-feedback modulator is multi-bits. The quantizer is implemented by discarding the LSBs.

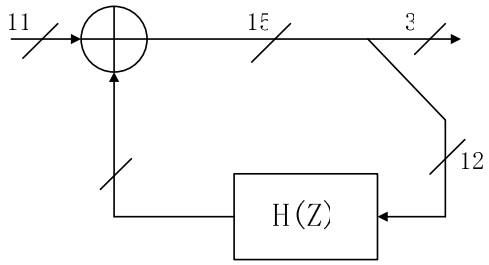

Fig.16 Multi-bit error feedback ΔΣ modulator

The feedback filter transfer function is

$$H_{ntf} = \frac{3Z^{-1}(1-0.5Z^{-1})(1-\frac{4}{3}Z^{-1}+\frac{2}{3}Z^{-2})}{1-Z^{-1}+0.5Z^{-2}} \qquad (6)$$

Compared to MASH modulator, the error-feedback modulator has less high frequency noise, and the simulated quantization noise PSD is shown in Fig.17.

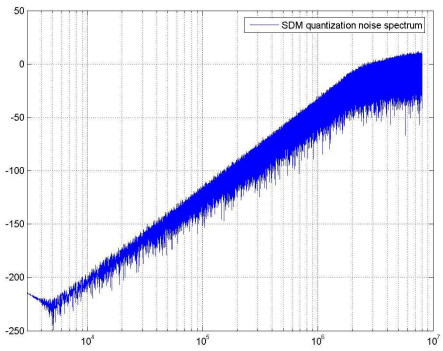

Fig.17 Simulated 3rd error-feedback SDM quantization noise spectrum

3 Measured Performances

A 2.4-GHz CMOS transceiver RF-end prototype chip is implemented in UMC 0.18um process, including LNA、Mixer、PA、Fractional-N frequency synthesizer、polyphase filter and Variable Gain Amplifier (VGA), as shown in Fig.18. This process is a six-metal single poly process. The MIM capacitors are formed using the two top metals, M5 and M6.The VCO control line and the loop filter are place as far as possible from the digital circuit part, including $\Delta\Sigma$ modulator and serial parallel interface (SPI). Guard rings are added to protect VCO from noise. VCO, analog circuit, digital circuit are connected to separate power lines to minimize crosstalk.

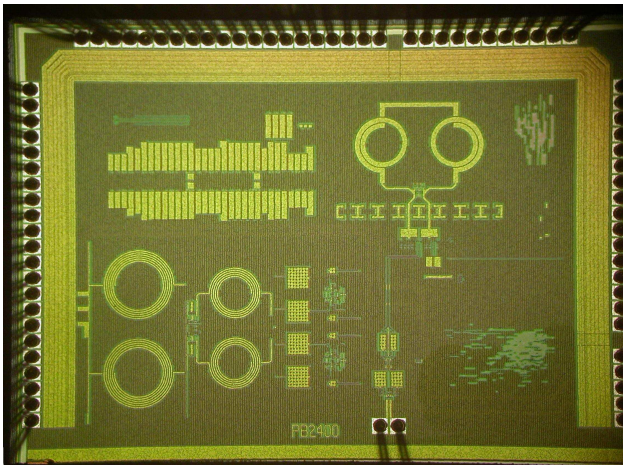

Fig.18 Prototype chip photograph

The measured transfer characteristic curve of VCO is shown in Fig.19

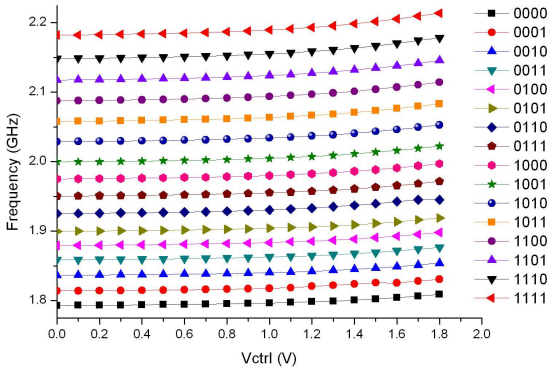

Fig.19 Measured transfer characteristic of VCO

The loop bandwidth of frequency synthesizer is 500 KHz to implement the in –loop GMSK modulation of 1Mbps data rate. The measured phase noise is shown in Fig.20. The prototype achieves -112dBc/Hz at 1MHz offset, -119dBc/Hz at 3MHz offset.

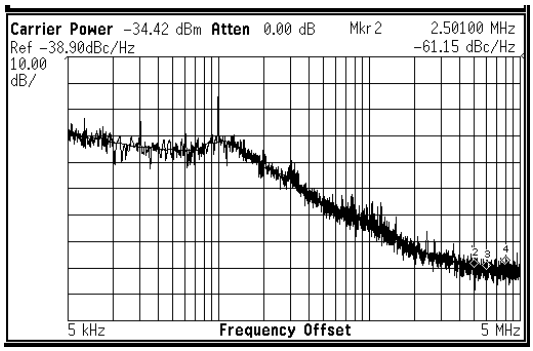

Fig.20 Measured Phase Noise Performance

4 Conclusion

An ISM band Fractional-N frequency synthesizer with automatic calibration technique is present in the paper. High order multi-bit error-feedback sigma-delta modulator and high linearity PFD/CP are adopted to improve the in band phase noise performance. The prototype chip is design in UMC18 RF process, and occupies 1.5*2.3 mm2. The measured phase noise from the closed loop is -112dBc/Hz at 1 MHz offset, -119dBc/Hz at 3MHz offset.

References:

[1] Lincoln Leung Lai Kan, Dennis M. C. Lau, Shuzuo Lou, Alan W. L. Ng, Rachel Dan Wang, A 1-V 86-mW-RX 53-mW-TX Single-Chip CMOS Transceiver for WLAN IEEE 802.11a,

IEEE Journal of SOLID-STATE CIRCUITS, Vol.42, No.9, Sep 2007, pp.1986-1998.

[2] William W.Si, Srenik Mehta, Hirad Samavati, Manolis Terrovitis, Michael Mack, David Su, Bruce Wooley, A 1.9-GHz Single-Chip CMOS PHS Cellphone, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.41, No.12, Dec 2006, pp.2737-2745.

[3] Brian Miller, Robert J. Conley, A Multiple Modulator Fractional Divider, *IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT*, Vol. 40, No.3, Jun 1993, pp.578-583.

[4] Asad A. Abidi, The Path to the Software-Define Radio Receiver, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.42, No.5, May 2007, pp.954-966.

[5] Emad Hegazi, Asad A.Abidi, A 17-mW Transmitter and Frequency Synthesizer for 900-MHz GSM Fully Integrated in 0.35-um CMOS, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.38, No.5, May 2003, pp.782-792.

[6] J. A. Crawford, *Frequency Synthesizer Handbook*, MA: Artech, 1994

[7] B. Razavi, *Phase-locking in high-performance Systems: From Devices to Architecture*, New York: Wiley-Interscience.

[8] T.Riley, M. Copeland, T.Kwasniewski, Delta-sigma modulation in fractional-N frequency synthesizer, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.28, No.5, May 1993, pp.553-559.

[9] H. Hagberg, *Multi-divide frequency division*, U.S. Patent 5948046, Sep, 1999.

[10] B.De Muer, M.J.Steyaert, A CMOS monolithic delta-sigma-controlled fractional-N frequency synthesizer for DCS-1800, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.37, No.7, Jul 2002, pp.835-844.

[11] W.Rhee, A.Ali, B.Song, A 1.1GHz CMOS fractional-N frequency synthesizers for high spectral purity, *IEEE ISSCC Dig. Tech. Papers*, 2000, pp.198-199.

[12] S.Norsworthy, R. Schreier, G.Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*. New York: IEEE Press, 1997.

[13] M.Perrot, T.TewKsbury, C. Sodini, A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.32, No.12, Dec 1997, pp.2048-2060.

[14] Dua Idris Yannick Le Moullec, Patrick Eggers, Design and Impelmentation of Self-Calibration for Digital Predistortion of Power Amplifiers, *WSEAS TRANSACTIONS on CIRCUITS AND SYSTEMS*, Issue 2, Vol.7, Feb 2008.

[15] Sudhakar Pamarti, Lars Jansson, Ian Galton, A Wideband 2.4-GHz Delta-Sigma Fractional-N PLL With 1-Mb/s In-Loop Modulation, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.39, No.1, Jan 2004, pp.49-62.

[16] Enrico Temproriti, Gudio Albasini, Ivan Bietti, Rinaldo Castello, Matteo Colombo, A 700-KHz Bandwidth Sigma-Delta Fractional Synthesizer With Spurs Compensation and Linearization Techniques for WCDMA Applications, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.39, No.9, Sep 2004, pp.1446-1454.

[17] Sudhakar Pamarti, Ian Galton, Phase-Noise Cancellation Design Tradeoffs in Delta-Sigma Fractional-N PLLs, *IEEE TRANSACTION ON CIRCUIT AND SYSTEMS-II: ANALOG AND DIGTIAL SIGNAL PROCESSING*, Vol.50, No.11, Nov 2003, pp.829-838.

[18] Manoj Gupta, Bang-Sup Song , A 1.8-GHz Spur-Cancelled Fractional-N Frequency Synthesizer With LMS-Based DAC Gain Calibration, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.41, No.12, Dec 2006, pp.2842-2851.

[19] Ashok Swaminathan, Kevin J. Wang, Ian Galton, A Wide-Bandwidth 2.4 GHz ISM Band Fractional-N PLL With Adaptive Phase Noise Cancellation, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.42, No.12, Dec 2007, pp.2639-2650.

[20] Scott E. Meninger, Michael H. Perrot, A 1-MHz Bandwidth 3.6-GHz 0.18-um CMOS Fractional-N Synthesizer Utilizing a Hybrid PFD/DAC Structure for Reduced Broadband Phase Noise, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.41, No.4, Apr 2006, pp.966-980.

[21] M.H.Perrot, M.D.Trott, C.G.Sodini, A modeling approach for $\Sigma-\Delta$ fractional-N frequency synthesizers allowing straightforward noise analysis, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.37, No.8, Aug 2002, pp.1028-1038.

[22] Jiun-Wei Hong, Chun-Li Hou, Chun-Ming Chang, Shih-Ting Cheng , Hsin-Yu Su, Current or/And Voltage-Mode Quadrature Oscillators With Grounded Capacitors and Resistors Using FDCCIIs, *WSEAS TRANSACTIONS on CIRCUITS AND SYSTEMS*, Issue 3, Vol.7, Mar 2008.

[23] D.Leeson, A simple model of feedback oscillator noise spectrum, *Proc. IEEE,* Vol.54, No.2, Feb. 1966, pp.239-330.

[24] William B.Wilson , Un-Ku Moon Kadaba R. Lakshmikumar, Ling Dai , A CMOS Self-Calibrating Frequency Synthesizer, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.35, No.10, Oct 2000, pp.1437-1444.

[25] Adem Aktas , Mohammed Ismail, CMOS PLL Calibration Techniques, *IEEE circuits & devices Magazine*, Sep-Oct 2004, pp.6-11.

[26] Bram De Muer, Michiel S. J. Steyaert, On The Analysis of $\Delta\Sigma$ Fractional-N Frequency Synthesizers for High-Spectral Purity, *IEEE TRANSACTION ON CIRCUIT AND SYSTEMS-II: ANALOG AND DIGTIAL SIGNAL PROCESSING*, Vol.50, No.11, Nov 2003, pp.784-793.

[27] S. R. Nors Cicero S. Vaucher, Igor Ferencic, Matthias Loccher, Sebastian Sedvallson, Urs Voegeli , Zhenhua Wang, A Family of Low-Power Truly Modulator Programmable Dividers in Standard 0.35-um CMOS Technology, *IEEE Journal of SOLID-STATE CIRCUITS*, Vol.35, No.7, Jul 2000, pp.1039-1045.

[28] I.V. Thompson, P.V. Brennan, Fourth-order PLL loop filter design technique with invariant natural frequency and phase margin, *IEE Proc.-Circuits Devices Syst.*, Vol.152, No.2, Apr 2005.

[29] I.JIVET, B.DRAGOI, Performance Analysis of Direct Digital Synthesizer Architecture with Amplitude Sequencing, *WSEAS TRANSACTIONS on CIRCUITS AND SYSTEMS*, Issue 1, Vol.7, Jan2008.