Design and Synthesis of a Configurable Fractional Order Hold Device for Sampled-data Control Systems

KOLDO BASTERRETXEA, RAFAEL BÁRCENA, and UNAI UGALDE
Department of Electronics and Telecommunications
Universidad del País Vasco/Euskal Herriko Unibertsitatea (UPV/EHU)
IITUE Bilbao. La Casilla plaza, 3, Bilbao
SPAIN
koldo.basterretxea@ehu.es http://www.ehu.es/apes

Abstract:- Zero-order hold devices (ZOH) are mainly used in digital control applications to obtain the output analog signals of digitally implemented controllers. However, it is proved that special hold devices such as the fractional order hold device (FROH) can improve, if properly tuned, the performance of hybrid control systems. Although the applicability of these devices has been theoretically studied in numerous works, there is no report of real experimentation with digital controllers that include special hold devices for the control signal interpolation. This lack of real application experiments is mainly due to the difficulties encountered in implementing such hold devices with the processing speed and configurability that real-time digital controllers require. This paper describes a totally configurable digital design of a FROH device, adequate for any digital control system platform. The implementation of an 8-bit resolution FROH prototype has been carried out and its performance tested on a field programmable gate array (FPGA).

Key-Words: - Hold device, FROH, configurable hardware, FPGA, digital controller, D/A conversion

1 Introduction

In feedback control systems, the positions of the plant zeros notably bias the achievable performance of operation –see, for instance, [1] and its references-. In the last years –see, [2], [3] and cited references-, various research works have been focused on the behavior of discrete zeros of digitally controlled systems as a function of used signal reconstruction method and sampling period. In this context, it has been proved that using properly adjusted fractional order hold devices (FROH) for control signal reconstruction, a more stable position of discrete zeros can be achieved compared to systems that use the more common zero order hold (ZOH) or first order hold (FOH) devices [4]. In [4] an analytic method is proposed to obtain the optimum value of the FROH parameter for each discretization. Moreover, it is proved as well that there is no limitation in the sampling period for the application of the above mentioned tuning method [5].

While the use of FROH and other advanced hold devices has been studied at theoretical level and experimentation can be performed in simulation environments, there are no real experimentation reports, as far as we know, of hybrid control systems with embedded special hold devices. This is very likely due to the difficulty in achieving an adequate hardware implementation of such a device, which must be highly configurable to meet various digital control requisites (sampling periods, signal resolution etc), and fast enough to make device delay negligible compared to the used sampling period.

In this paper we present the design and implementation of a fully configurable digital FROH device with adjustable gain parameter and fast operation. Implementation has been performed on a FPGA, which assures the configurability of the device for different control requirements, so the obtained device is suitable for any real-time hybrid control system.

2 Sampled-data Control System with FROH-based Signal Interpolation

The design of the FROH device described here has been faced considering the constraints imposed by our actual real-time digital controller experimentation platform, as regards to sampling frequencies, clock signals and word-length. Still, the goal has been to obtain a universal design, easily adaptable to any digital control platform, so a parameterized hardware description has been performed. In this sense, the use of reconfigurable hardware as target technology is of base importance

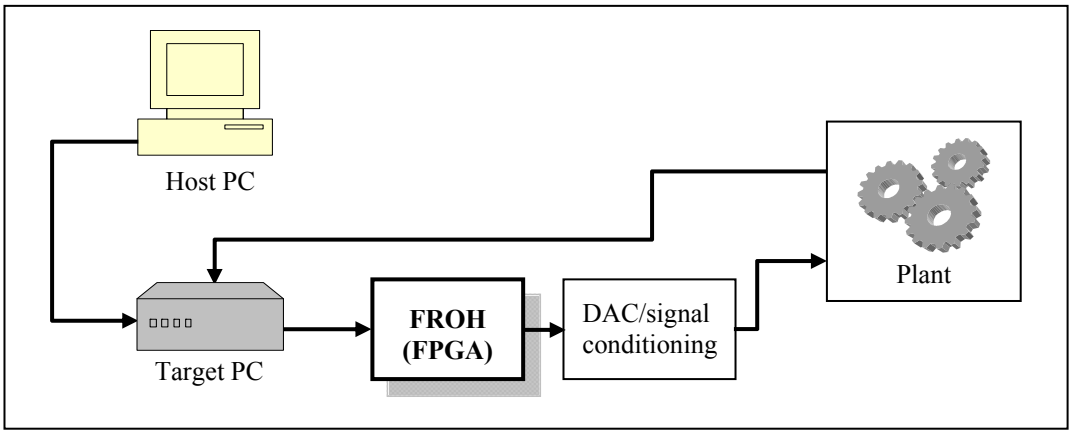

Fig. 1 General scheme of the PC-based real-time hybrid (digital/analog) control system. The special hold device processes the digital control signal.

to assure the required programmability of the device and to allow the necessary modifications in order to adapt the device to the requirements of different controllers. In what follows we briefly describe our hybrid control experimentation platform and its main characteristics.

Fig.1 shows a general view of the real-time control experimentation system based on PC and used as reference for this design. The design and tuning of the digital controllers is made under the Mathworks® programming environment at the host PC. The implementation of the computation of the control algorithms is performed by the *Real Time Workshop*, and the *xPCTarget* package is used to execute the algorithms on a real-time core running in the Target PC. The target PC, together with a multifunction data acquisition card (DAQ), constitute the embedded real-time digital controller which carries out the various control strategies to be experimented over different plants. The FROH device must be placed between the digital output of the DAQ and the DAC/signal conditioning circuitry that feeds the plant's signal input.

The DAQ actually attached to the Target PC is a NI-PCI6024E by National Instruments. Its main characteristics are:

- 8 TTL digital inputs/outputs.
- Two timing outputs with 24 bit resolution.
- 16 analog inputs with 12 bit resolution.
- 2 analog outputs with 12 bit resolution.

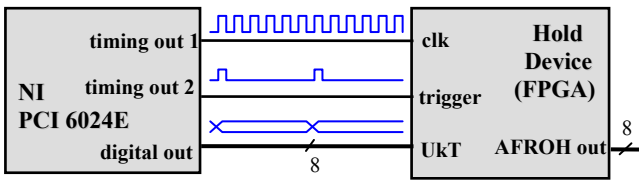

Fig. 2 Signals provided by the NI-PCI6024E DAQ to the hold device. All signals are synchronized by the internal clock of the DAQ.

- 200 Ks/sec sampling frequency.
- 20 MHz internal reference clocking.

Accordingly, the output signals of the DAQ, which constitute the input signals of the hold device, are the following:

- Digital control signal (*UkT*): 8 bit positive normalized value, $UkT \in [0,1)$.
- Clock signal (clk): 1 MHz 50% duty cycle clock obtained from DAQ timing output 1.
- Triggering signal (trigger): triggering pulse signal generated every sampling time and synchronized with the *UkT* output.

The three signals are synchronized over the timing base signal of the DAQ. The choice of a 1 MHz frequency clock signal obeys to the restriction imposed by the DAQ timing output, since above this frequency it produces a poor signal shape, inadequate for clocking. Fig. 2 shows the signaling scheme between the DAQ and the hold system.

It must be emphasized that the delay introduced by the hold system, included D/A conversion and the signal conditioning stage, must be "sufficiently small" compared to the sampling period (T) used by the controller. This means that the maximum delay must be between one and two orders of magnitude below T to assure that the control tuning remains valid for the system. The following section describes in detail the design of the FROH device.

3 The Approximated Fractional Order Hold

A FROH is an adjustable signal hold device for hybrid control systems. Its main advantage over the ZOH and the FOH, as stated before, is its adjustable gain parameter β, which provides more freedom in

the placement of the zeros of the discretized plant and, therefore, may improve the performance of some digitally controlled feedback systems, particularly when the sampling period T is relatively high compared to the plant dynamics. It is a hold device with an adjustable linear hold function and one element of memory. The hold function can be analytically described by the following expression:

$$u(t) = u(kT) + \beta\left[\frac{u(kT) - u((k-1)T)}{T}\right](t - kT) \qquad (1)$$
$$kT \le t \le (k+1)T$$

where T is the sampling period, k represents the k[th] input sample, and β is the adjustable gain parameter. If a digital implementation is made, we obtain a hold function approximated by successive steps (Fig.3). We call this hold device the approximated fractional order hold or AFROH [7].

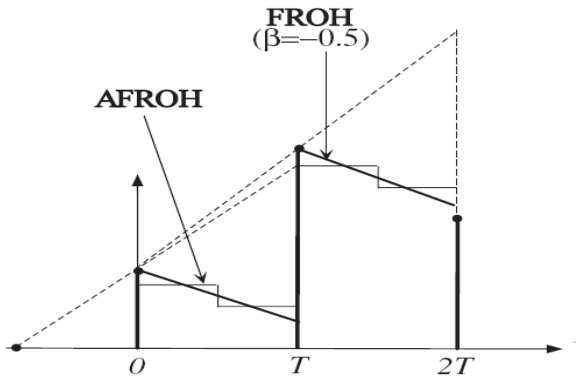

Fig. 3 Hold function of a FROH and a two step AFROH approximation.

Being N the number of steps to approximating the hold linear function, we can write:

$$u(t) = \left(1 + \frac{2l-1}{2N}\right)\beta u(kT) - \left(\frac{2l-1}{2N}\right)\beta u\left((k-1)T\right) \qquad (2)$$

$$\left(k + \frac{l-1}{N}\right)T \le t \le (k + \frac{l}{N})T \qquad (3)$$
$$l = 1, \ldots, N$$

Obviously, the more steps the device is able to produce, the better and smoother approximation to the continuous ideal function is obtained.

In order to estimate the number of steps the digital hold device should produce for approximating the hold function, we analyzed the behavior of a hybrid closed-loop control system including a FROH device. We chose two application examples published in [8] where the response of a second order plant and a more complex fourth order plant, both controlled by a two-degree-of-freedom (a.k.a RST) digital controller is described. The referred work shows the performance improvement of the system when using a properly tuned FROH compared to the same system with a conventional ZOH. The tuning method for β proposed in [8] is based on a frequency domain analysis that allows the improvement of the continuous-time closed-loop performance of the system.

3.1 A simple case

The dynamic of the first plant is described by a second order transfer function,

$$G(s) = \frac{1}{s(s+1)} \qquad (4)$$

which has one ZOH discretization zero. The selected sampling period was T = 0.1s. The gain parameter of the FROH is adjusted to

Figure	**ZOH**	**FROH**	**AFROH_2**	**AFROH_4**	**AFROH_8**	**AFROH_16**	**AFROH_32**	**AFROH_64**
$t_{s,5\%}$	296 ms	160 ms	957 ms	279 ms	247 ms	155 ms	157 ms	159 ms
OS	23.25 %	3.31 %	16.64 %	4.40 %	1,91 %	1.94 %	2.60 %	2,95 %
Energy	6,479	2,906	7,291	4,298	3,499	3,182	3,039	2,971

Table 1: Obtained continuous-response performance figures for the digitally controlled-plant described by (3) for different hold devices**.**

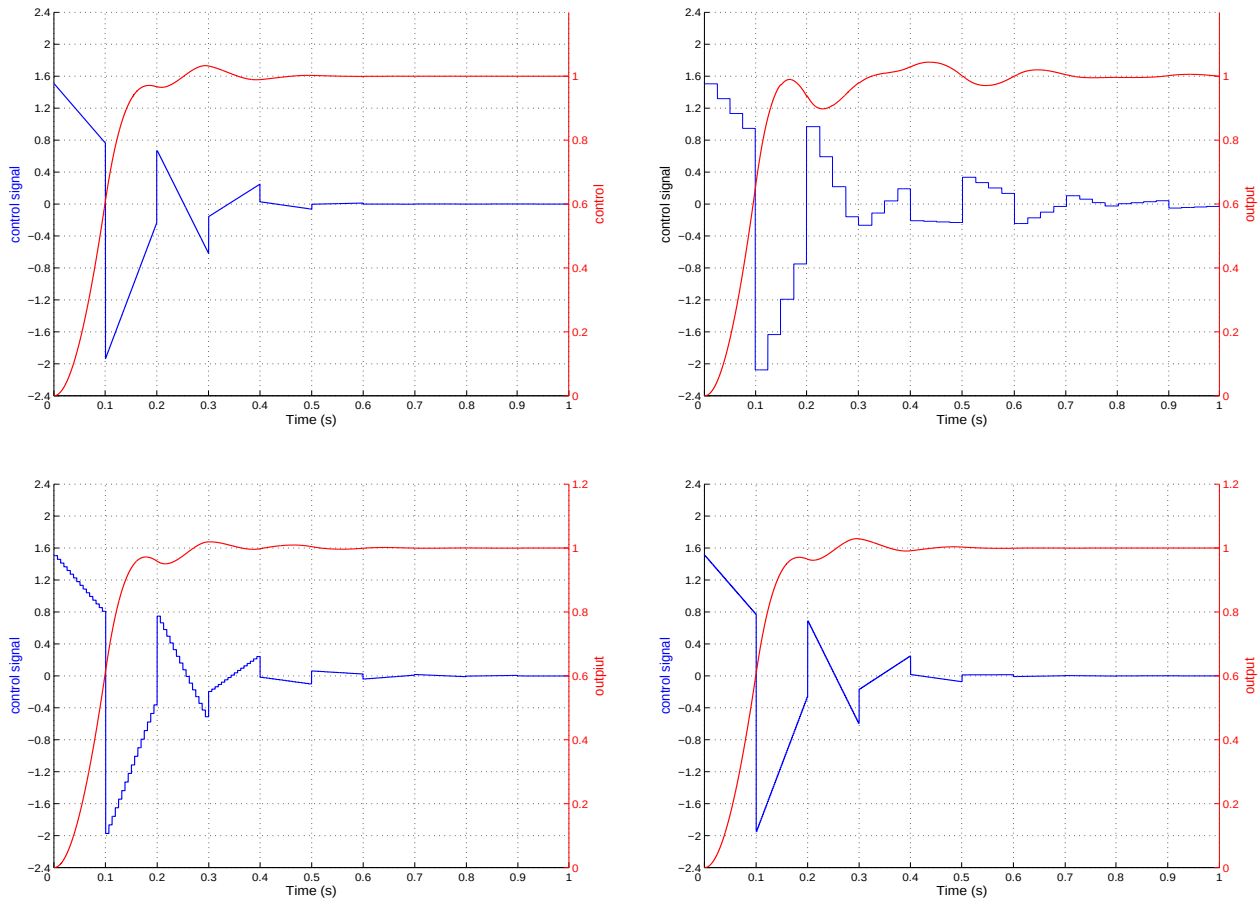

Fig. 4: Continuous-time plant (4) output for an unitary step input and produced control signal by the digital RST controller for different fractional order hold devices: continuous FROH (top left), 4 step AFROH (top right), 16 step AFROH (bottom left), and 64 step AFROH (bottom right).

$$\beta = -0.493743 \qquad (5)$$

and the RST digital controller polynomials are fitted to obtain a convenient output response. Performed simulations show the superiority of the continuous time domain response of the system using the FROH device (see details in [8]).

To perform the experimentation with the AFROH and to analyze the influence of the number of approximating steps on system performance, we substituted the model block of the continuous FROH used in the above mentioned example with a model of the AFROH with an adjustable step number parameter *N*. We compared the obtained results to the figures obtained for the continuous FROH in order to estimate an adequate maximum value for *N* in the design of the AFROH digital device. Table 1 shows obtained continuous time response performance figures when applying a unitary step at the input for the analyzed cases: ZOH, continuous FROH (machine accuracy), 2 step, 4 step, 8 step, 16 step, 32 step and 64 step approximations (AFROH). Selected performance figures for comparison were settling time (5% criterion), overshoot and energy consumed during the transient.

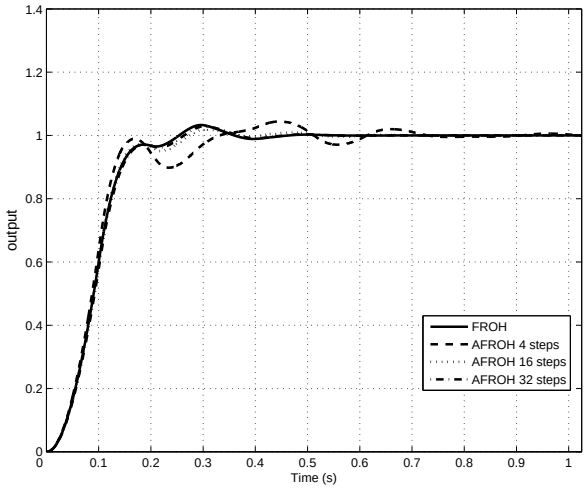

Fig. 5: Output signals comparison graph for the plant described by (4)

Figure	ZOH	FROH	AFROH_2	AFROH_4	AFROH_8	AFROH_16	AFROH_32	AFROH_64
$t_{s,5\%}$	313 ms	239 ms	NaN	587 ms	236 ms	237 ms	238 ms	238 ms
OS	10.89 %	2.07 %	16.64 %	7.63 %	3.65 %	1.98 %	2.01 %	2,03 %
Energy	110,314	66,140	128,400	80,497	70,717	67,892	66,891	66,485

Table 2: Obtained continuous-response performance figures for the digitally controlled-plant described by (4) for different hold devices**.**

From Table 1 we can conclude that an adequate performance, that is, similar to that obtained with the continuous FROH, begins to happen with a 16 step approximation (4 bit timing resolution for a digital design). Below this resolution, the adjustment of β, analytically obtained for the continuous model, is not adequate for the approximated model. Graphical representations of the control signals and the controlled plant outputs are shown in Fig.4 for selected cases. A comparison of produced plant output behavior is depicted in Fig.5 for the same approximation resolutions.

3.2 A more complex case

The fourth relative order plant model proposed for this application example is described by,

$$G(s) = \frac{100}{s(s^3 + 19.9s^2 + 98.25s - 10.025)} \qquad (6)$$

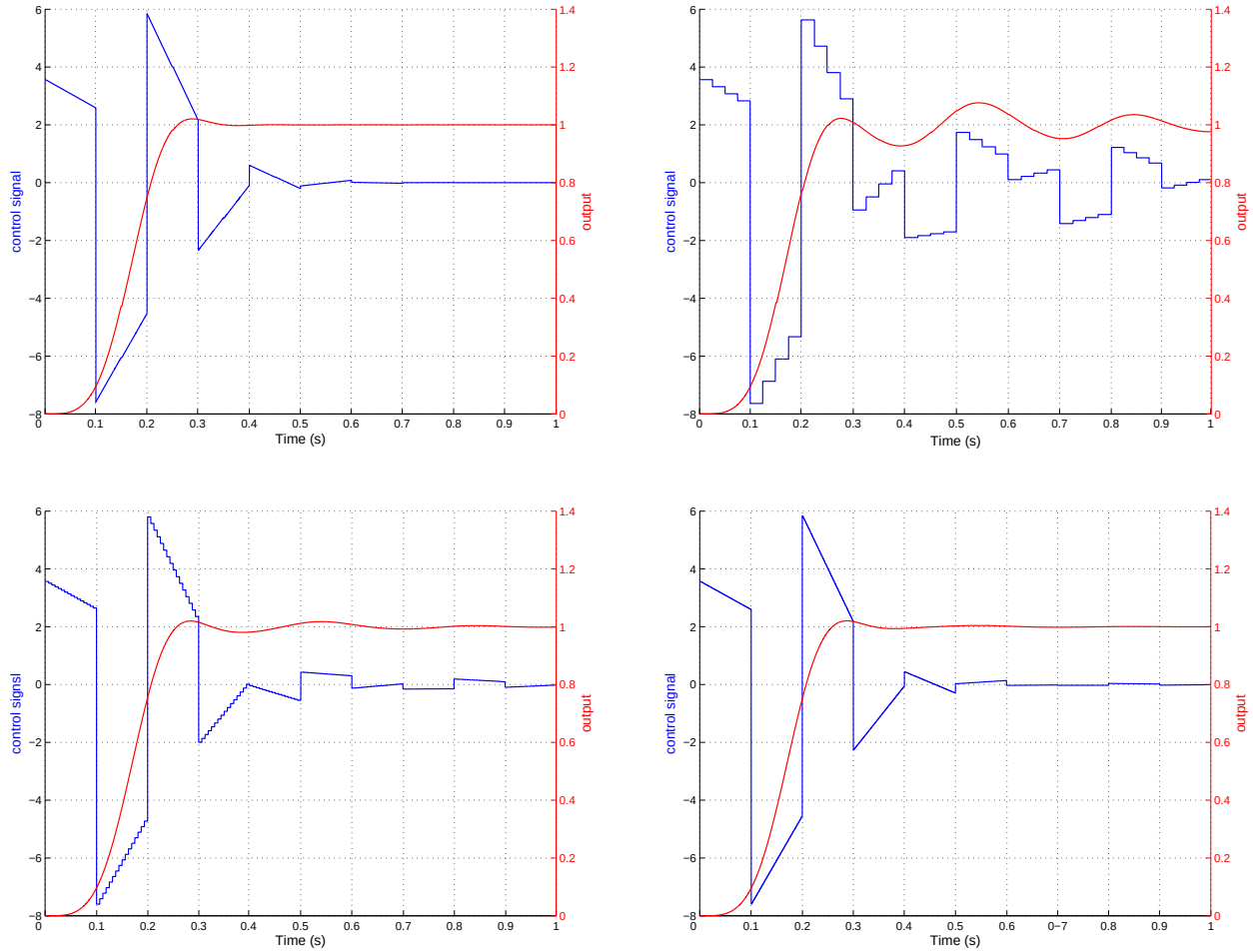

Fig. 6: Continuous-time plant (6) output for an unitary step input and produced control signal by the digital RST controller for different fractional order hold devices: continuous FROH (top left), 4 step AFROH (top right), 16 step AFROH (bottom left), and 64 step AFROH (bottom right).

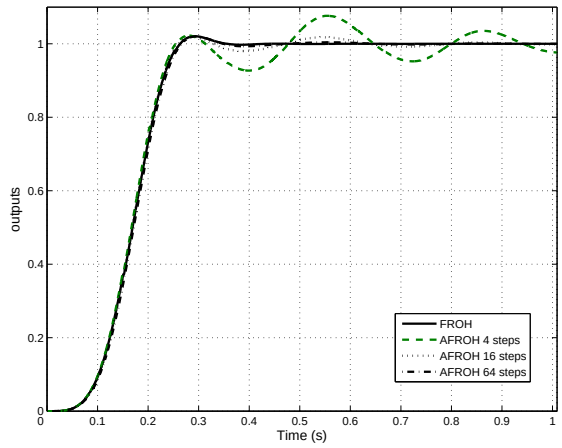

Figure 7: Output signals comparison graph for the plant described by (4)

Selected sampling period was also T = 0.1s. After obtaining the discretized z-domain model of the plant, controller polynomials and closed-loop z-domain response, the optimum value obtained for β was [8]:

$$\beta = -0.274614 \qquad (7)$$

We followed exactly the same experimentation methodology used in the previous example, that is, substitute the FROH model with an AFROH model with selectable N. Table 2 summarizes obtained system performance figures for the analyzed cases. Adequate performance begins, here again, with a 16 step approximation. Fig.6 shows control signals and plant responses for selected cases. In Fig.7 a comparison graph of obtained responses is depicted.

Anyway, let us point out that required timing resolution of the AFROH for an adequate system response is tightly related to the used sampling period T. Hence, to cover a wide range of digital control platforms, and anticipating that sometimes a higher timing resolution would be needed, a 64 step approximation AFROH device is proposed for design and implementation.

4 A Digital Design of the Approximated Fractional Order Hold Device

4.1 Design constraints and configurability issues

Various constraints must be considered when designing a digital AFROH device. First, the gain parameter β of the device must be adjustable. The tuning of β is made off-line and is calculated to obtain an optimum behavior of the controlled system. In addition, we want a selectable value of N within a minimum value N=2 and a maximum value N_{max}, which will be limited by the resolution of the system and its maximum computing speed or clock frequency. The resolution or digital word-length (*res*) of the device will be considered as a design parameter also, as it can vary for different hardware platforms (the word-length in this design is 8 bits). Beside this, it must be considered that the sampling period T may change for different control applications, so this is an element of the vector $\boldsymbol{P}$ of design parameters too: $\boldsymbol{P}$ = [β, res, N, T]. Let us fix the limits of the parameter values, more precisely, of the T/N rate: considering that clock frequency is limited to 1MHz, we will take a minimum value of the sampling period of T_{min}= 0,1ms, so we will limit the value of $N_{\max}$ to 64 steps (powers of two are used as it will be controlled by a binary counter). Therefore, the amount of clock cycles required for each step is $T/(T_{clk}.N_{max})$ = 1,562, which is in the minimum bound because, as we will see, the hold device has a latency of one clock cycle. In case the minimum sampling period would need to be reduced an order of magnitude or so (that is to T = 0,01ms), N_{max} should be limited to 8, which could be adequate for the most demanding plant dynamics.

The circuit has been designed following the block scheme depicted in Fig.8. It can be observed that, even if this design would require two clock signals, all sequential elements are clocked by the same signal of period T_{clk}, conforming a unique clock domain. This way we assure the total synchrony of the system and simplify static timing analysis. To perform the selective timing of the various modules a signal controller block (*counter/timing* in Fig.8), which produces adequately timed control and enable signals, has been designed. The circuit operates internally with double word-length (16 bits) as the block *step* (Fig.8) encloses an internal multiplier to calculate the value to be added to each approximating step in order to produce the next one. This block operates with signed values, allowing the use of negative values of β to generate both negative and positive slopes.

Two additional elements have been attached to the circuit to prevent the output from exceeding the variation range of the control signal which, with an 8-bit word-length, is [0 , 0.99609375]. One is an AND gate placed at the output of the output register, which is fed with the sign bit of the register content and zeroes the output when this bit changes to '1' (negative value). The other one is a comparator that checks the output value and disables the output

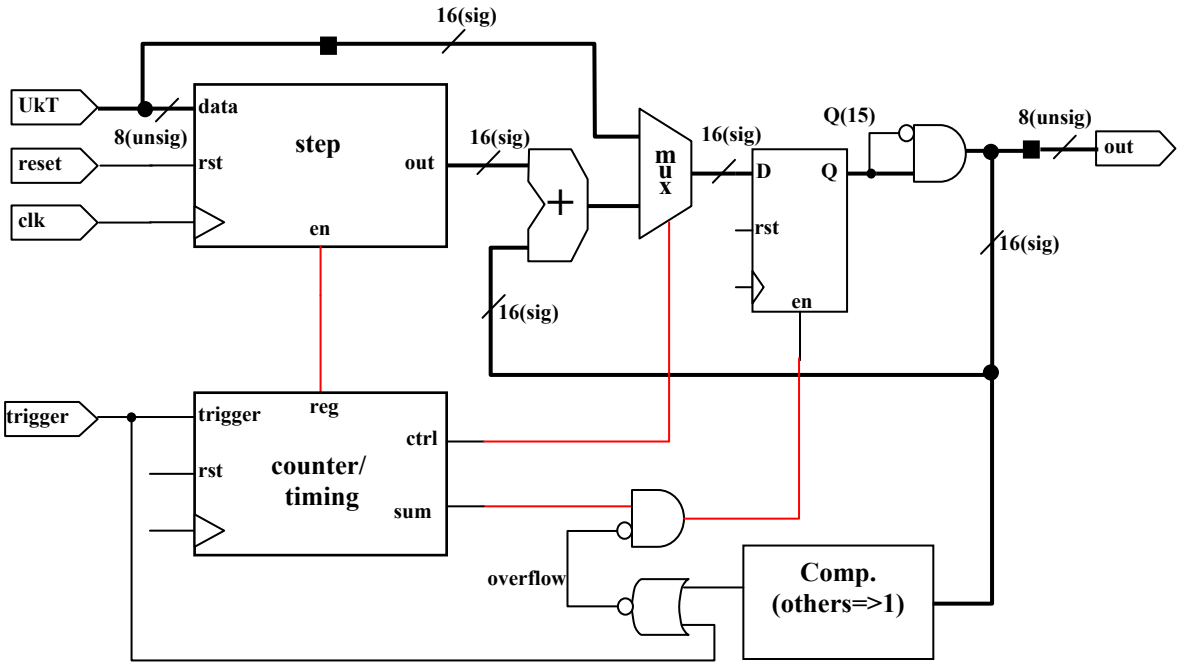

Fig. 8 Block diagram of the digital AFROH device for an 8-bit word-length. Some clocking and reset signals have been omitted for clarity.

register when the maximum limit value is reached. This enable signal is activated again when a new control value is provided at the input (*trigger* = '1'). In fact it is very unlikely that an underflow or an overflow happen because the optimum values of β are usually negative, so the hold function slope make the signal tend to its steady state value.

Let us analyze in detail the operation of the blocks *step* and *counter/timing*:

Counter/timing: The input parameters of this block are T and N (T_{clk} is supposed to be known as well). It encloses two pulse counters, one for the interval of period T, and other one for the interval of period T/N. Combined with a comparator-based logic, it provides three timing signals essentials for the correct operation of the device:

- The signal *ctrl*: This is the input selection signal of the multiplexer. During the first hold interval (first step) this signal is asserted to '1', selecting the system input signal $u(kT)$, which is directly routed to the output register. During the rest of the sampling period this signal is asserted to '0', and the multiplexer transmits the output signal from the adder.
- The signal *sum*: This signal is asserted each time a new step must be generated. Combined with the *overflow* signal, it controls the output register's enable signal. When active, the register content is updated at each clock pulse, adding it to the value provided by the *step* block and so generating the next step.
- The signal *reg*: This signal is activated two clock cycles before a new control value $u(kT)$ is provided to the device. It enables the input register of the *step* block to capture the "previous" value of the control signal $u(k\text{-}1)T$ to calculate the new step amplitude.

Step: The input parameters of this block are N and β. It is an arithmetic block that calculates the signal amplitude that must be added to each step in order to generate the next one. The FROH is a hold device with one memory element, since the previous value of $u(kT)$ must be registered to compute the hold function. Thus, this block performs the operation $[u(kT)\text{-}u((k\text{-}1)T)].\beta/N$. Considering β/N as a configuration parameter rather than as a function variable, this block only encloses a substractor and an internal multiplier that multiplies the difference between successive samples by a constant value.

4.2 Circuit description, synthesis and simulation

A register transfer logic (RTL) VHDL description of the hold device has been written based on the scheme presented in Fig.8 in order to rapidly obtain a working prototype [9]. The word-length (*res*), T, N, and β complete the set of parameters of a parametric hardware description file, assuring the validity of the code under any variation of the vector ***P*** and making the device suitable for any controller. We used Xilinx ISE9.1i for code debugging and

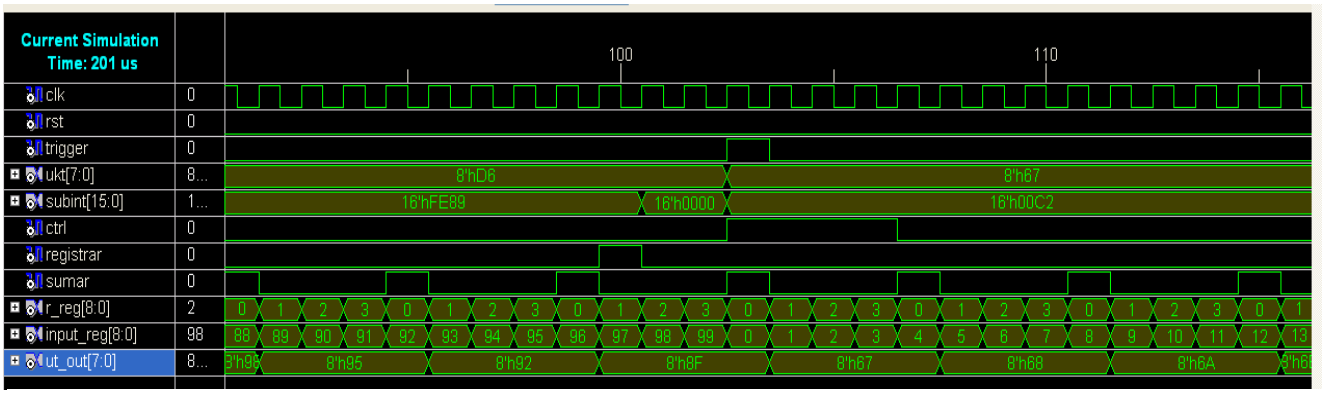

Fig. 9 Simulation output of the AFROH device for T=0,1ms, N=32, and β=-0.8. The waveform diagram shows the moment in which a new control value U(kT) is sampled.

circuit simulation. The synthesis has been made with the XST (Xilinx Synthesis Tool), and placement and routing processes onr a Spartan-3E family FPGA by the Xilinx ISE implementation tools. Fig. 9 shows circuit operation for a sampling period T = 0.1ms, a number of steps N = 32, and β = -0.8.

The circuit latency is one clock cycle, imposed by the output register, as the input is routed directly to this register. Hence, for a T_{clk} = 1μs, we assure that the delay introduced by the hold device is "sufficiently small" compared to T_{min}. Obviously this delay can be reduced by augmenting the clock frequency (if possible).

Field programmable gates arrays are more and more being used in digital controller implementations due to their configurability, reliability and increasing performance and low cost [10],[11]. In this case, the target device has been a Xilinx 3S500efg320-4 FPGA. The synthesis and timing details after placement and routing are listed below:

Macro Statistics

# Multipliers	: 1
9x9-bit multiplier	: 1
# Adders/substractors	: 4
16-bit adder	: 1
9-bit adder	: 2
9-bit subtractor	: 1
# Registers	: 4
16-bit register	: 1
9-bit register	: 3
# Comparators	: 1
9-bit comp. lessequal	: 1

Device utilization summary:

Selected Device : 3s500efg320-4		
# Slices: 49 out of 4656		1%
# Slice Flip Flops:	42 out of 9312	0%
# 4 input LUTs:	88 out of 9312	0%
# IOs:		19
# bonded IOBs:	19 out of 232	8%
# MULT18X18SIOs	1 out of 20	5%
# GCLKs:	1 out of 24	4%

Total equivalent gate count: 1.026

Timing Summary:

Speed Grade: -4
Offset in : best case Achievable 12.118ns
Offset out : best case Achievable 11.648ns
Clk minimum period: 14.170ns

The figures show that maximum clock frequency for this implementation is 73.914 MHz, which would permit the use of controller sampling periods of 0.01ms and less, and to generate more than 64 steps at each sampling period if necessary.

5 D/A conversion

Once the AFROH generates the digital values to approximating the hold function, a D/A conversion must be performed. The conversion scheme to be applied is conditioned by the operation frequency and the maximum delay requirements. The resistor ladder based parallel D/A conversion is the fastest and the most suitable for high frequencies, but an analog circuit is required and its accuracy may be

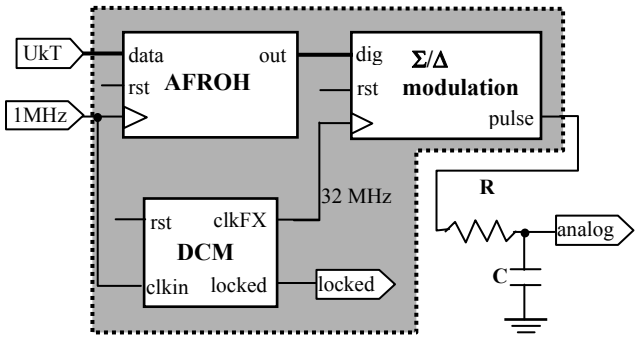

Fig. 10 An embedded DAC conversion for the AFROH based on Σ/Δ modulation

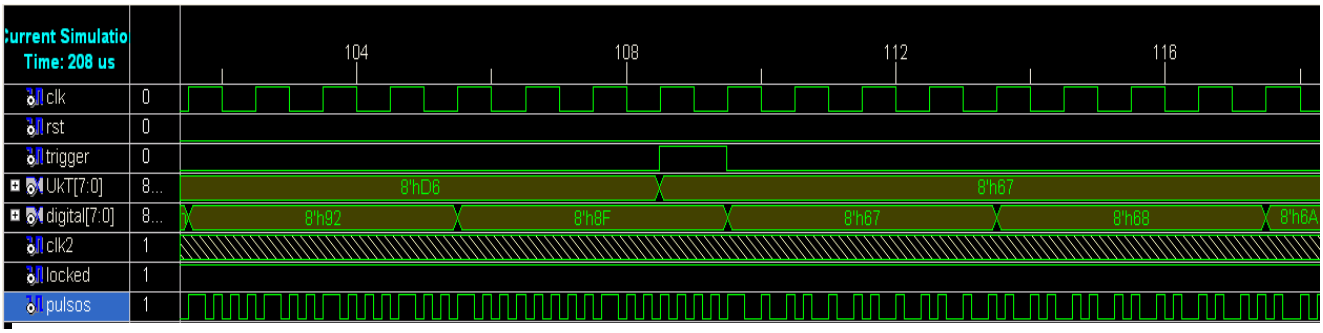

Fig. 11 Output bitstream produced by the hold systems output Σ/Δ modulator (same parameters as in Fig.9).

affected by noise and temperature changes. A more compact option that can be embedded inside the FPGA together with the AFROH, is a pulse-duration based conversion scheme. In addition, pulse modulated signals are suitable to directly drive many electric machines and are widely used in motion control. The simplest option is a Pulse Wide Modulation (PWM) circuit followed by a passive first order low-pass filter, but PWM-based D/A conversion have some drawbacks. First, since the frequency of the output bitstream is the same as the input rate, its bandwidth is relatively wide and large time constants are needed for the output filter. Second, the noise from pulse generation tends to concentrate at this frequency, so it is not filtered at the output. Both of these problems are reduced with a sigma-delta modulator [12].

Hence, a sigma-delta modulator has been embedded and connected to the AFROH output (Fig. 10). However, keeping the resolution of the system would require a very high clock frequency. In our case, even considering the restrictions imposed to the design, the worst case (T_{min} = 0,1ms and N = 64), would require 256 clock pulses each 1μs to keep a 8 bit resolution modulation, and that means a 256 MHz clock frequency. To implement a first prototype we have reduced the D/A resolution to 5 bits. That means producing a 32 MHz clock signal, and this is precisely the maximum frequency we can obtain from a Spartan-3E DCM (Digital Clock Manager) frequency synthesizer output when a 1MHz clock is applied to its input. This resolution reduction requires scaling down the input, but this only implies a hardwired bit shifting. The simulation of the whole system operation is depicted in Fig. 9.

6 Conclusion

Implementation of special hold devices such as the FROH for real-time digital control has always been troublesome because of required operation speed and device configurability. Nowadays, the spread and cost reduction of high performance reconfigurable hardware provide the means to face the design and implementation of such a device for real-time hardware-in-the-loop experimentation with advanced digital controllers. The configurability of FPGAs allows for a parametric design that assures the adaptability of the hold devices to the controller changing requirements: control signal resolution, sampling period, parameter tuning of the hold device, and accuracy of the hold function approximation. The implementation of the FROH described here is a first step to achieve an advanced digital controller experimentation bench with special hold devices, which we hope that will allow us to go deeper into this attractive research field.

References:

[1] K. J. Åström, and B. Wittenmark, *Computer controlled systems. Theory and design,* Prentice-Hall, Englewood Cliffs, New Jersey. 3rd edition, 1997.

[2] M. J. Blachuta, On zeros of pulse transfer function', *IEEE Trans. Automat. Contr.*, Vol.44, No.6, 1999, pp. 1229-1234.

[3] M. de la Sen,, R. Bárcena, and A. J. Garrido, On the intrinsic limiting zeros as the sampling period tends to zero, *IEEE Trans. Circuits Syst. Part I*, Vol.48, No.7, 2001, pp. 898-900.

[4] R. Bárcena, M. de la Sen, and I. Sagastabeitia, Improving the stability properties of the zeros of sampled systems with fractional order hold, *IEE Proc. Control Theory Appl.*, Vol.147, No.4, 2000, pp. 456- 464.

[5] R. Bárcena, and M. de la Sen, On the sufficiently small sampling period for the convenient tuning of fractional-order hold circuits, *IEE Proc. Control Theory Appl.,* Vol. 150, No. 2, 2003, pp.183- 188,.

[6] R. Bárcena, M. de la Sen, I. Sagastabeitia, and J. M. Collantes, Discrete control for a computer hard disk by using a fractional order hold

device. *IEE Proc. Control Theory Appl.*, Vol.148, No.2, 2001, pp.117- 124.

[7] M. Ishitobi and Q. Zhu, Zeros of sampled systems with fractional order hold implemented by zero order hold, IEEE International Conference on Intelligent Processing Systems, (1997), 698-702.

[8] U. Ugalde, R. Bárcena, and K. Basterretxea, Ripple-Free Control Response by Using a Fractional Order Hold Device, *WSEAS Transactions on Systems*, to be published.

[9] P. V. Joshi, Use of VHDL in Rapid Prototyping, *WSEAS Transactions on Circuits and Systems*, Vol. 3, No. 5, (2004), 1085-1090.

[10] B. D. M. Bustillo, C. J. Italo, C. B. Carlos, and Q. M. Leonel, Design of a Logic Arithmetical Unit and its Application to Control of Motors, *WSEAS Transactions on Circuits and Systems*, Vol. 2, No. 4, (2003), 698-703.

[11] C-H. Chen, Discrete-event System Modelling and Hardware Synthesis of Hybrid Control System, *WSEAS Transactions on Circuits and Systems*, Vol. 5, No. 8, (2006), 1296-2734.

[12] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing. Principles, Algorithms and Applications,* Third Edition, Prentice Hall, Madrid, 1998, pp. 596-597.