

Design and Synthesis of a Configurable Fractional Order Hold Device for Sampled-data Control Systems

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Abstract:- Zero-order hold devices (ZOH) are mainly used in digital control applications to obtain the output analog signals of digitally implemented controllers. However, it is proved that special hold devices such as the fractional order hold device (FROH) can improve, if properly tuned, the performance of hybrid control systems. Although the applicability of these devices has been theoretically studied in numerous works, there is no report of real experimentation with digital controllers that include special hold devices for the control signal interpolation. This lack of real application experiments is mainly due to the difficulties encountered in implementing such hold devices with the processing speed and configurability that real-time digital controllers require. This paper describes a totally configurable digital design of a FROH device, adequate for any digital control system platform. The implementation of an 8-bit resolution FROH prototype has been carried out and its performance tested on a field programmable gate array (FPGA).

Key-Words: - Hold device, FROH, configurable hardware, FPGA, digital controller, D/A conversion

1 Introduction

In feedback control systems, the positions of the plant zeros notably bias the achievable performance of operation –see, for instance, [1] and its references-. In the last years –see, [2], [3] and cited references-, various research works have been focused on the behavior of discrete zeros of digitally controlled systems as a function of used signal reconstruction method and sampling period. In this context, it has been proved that using properly adjusted fractional order hold devices (FROH) for control signal reconstruction, a more stable position of discrete zeros can be achieved compared to systems that use the more common zero order hold (ZOH) or first order hold (FOH) devices [4]. In [4] an analytic method is proposed to obtain the optimum value of the FROH parameter for each discretization. Moreover, it is proved as well that there is no limitation in the sampling period for the application of the above mentioned tuning method [5].

While the use of FROH and other advanced hold devices has been studied at theoretical level and experimentation can be performed in simulation environments, there are no real experimentation reports, as far as we know, of hybrid control systems with embedded special hold devices. This is very likely due to the difficulty in achieving an

adequate hardware implementation of such a device, which must be highly configurable to meet various digital control requisites (sampling periods, signal resolution etc), and fast enough to make device delay negligible compared to the used sampling period.

In this paper we present the design and implementation of a fully configurable digital FROH device with adjustable gain parameter and fast operation. Implementation has been performed on a FPGA, which assures the configurability of the device for different control requirements, so the obtained device is suitable for any real-time hybrid control system.

2 Sampled-data Control System with FROH-based Signal Interpolation

The design of the FROH device described here has been faced considering the constraints imposed by our actual real-time digital controller experimentation platform, as regards to sampling frequencies, clock signals and word-length. Still, the goal has been to obtain a universal design, easily adaptable to any digital control platform, so a parameterized hardware description has been performed. In this sense, the use of reconfigurable hardware as target technology is of base importance

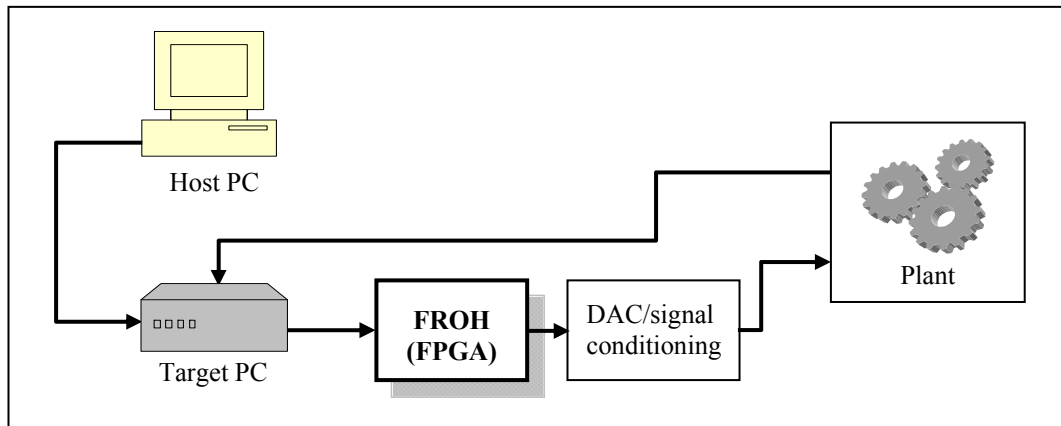


Fig. 1 General scheme of the PC-based real-time hybrid (digital/analog) control system. The special hold device processes the digital control signal.

to assure the required programmability of the device and to allow the necessary modifications in order to adapt the device to the requirements of different controllers. In what follows we briefly describe our hybrid control experimentation platform and its main characteristics.

Fig.1 shows a general view of the real-time control experimentation system based on PC and used as reference for this design. The design and tuning of the digital controllers is made under the Mathworks® programming environment at the host PC. The implementation of the computation of the control algorithms is performed by the *Real Time Workshop*, and the *xPCTarget* package is used to execute the algorithms on a real-time core running in the Target PC. The target PC, together with a multifunction data acquisition card (DAQ), constitute the embedded real-time digital controller which carries out the various control strategies to be experimented over different plants. The FROH device must be placed between the digital output of the DAQ and the DAC/signal conditioning circuitry that feeds the plant’s signal input.

The DAQ actually attached to the Target PC is a NI-PCI6024E by National Instruments. Its main characteristics are:

- 8 TTL digital inputs/outputs.
- Two timing outputs with 24 bit resolution.
- 16 analog inputs with 12 bit resolution.
- 2 analog outputs with 12 bit resolution.

- 200 Ks/sec sampling frequency.
- 20 MHz internal reference clocking.

Accordingly, the output signals of the DAQ, which constitute the input signals of the hold device, are the following:

- Digital control signal (UkT): 8 bit positive normalized value, $UkT \in [0,1)$.
- Clock signal (clk): 1 MHz 50% duty cycle clock obtained from DAQ timing output 1.
- Triggering signal (trigger): triggering pulse signal generated every sampling time and synchronized with the UkT output.

The three signals are synchronized over the timing base signal of the DAQ. The choice of a 1 MHz frequency clock signal obeys to the restriction imposed by the DAQ timing output, since above this frequency it produces a poor signal shape, inadequate for clocking. Fig. 2 shows the signaling scheme between the DAQ and the hold system.

It must be emphasized that the delay introduced by the hold system, included D/A conversion and the signal conditioning stage, must be “sufficiently small” compared to the sampling period (T) used by the controller. This means that the maximum delay must be between one and two orders of magnitude below T to assure that the control tuning remains valid for the system. The following section describes in detail the design of the FROH device.

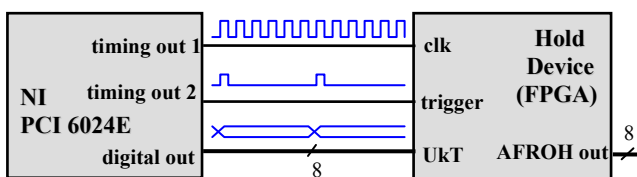


Fig. 2 Signals provided by the NI-PCI6024E DAQ to the hold device. All signals are synchronized by the internal clock of the DAQ.

3 The Approximated Fractional Order Hold

A FROH is an adjustable signal hold device for hybrid control systems. Its main advantage over the ZOH and the FOH, as stated before, is its adjustable gain parameter β , which provides more freedom in

the placement of the zeros of the discretized plant and, therefore, may improve the performance of some digitally controlled feedback systems, particularly when the sampling period T is relatively high compared to the plant dynamics. It is a hold device with an adjustable linear hold function and one element of memory. The hold function can be analytically described by the following expression:

$$u(t) = u(kT) + \beta \left[\frac{u(kT) - u((k-1)T)}{T} \right] (t - kT) \quad (1)$$

$kT \leq t \leq (k+1)T$

where T is the sampling period, k represents the k^{th} input sample, and β is the adjustable gain parameter. If a digital implementation is made, we obtain a hold function approximated by successive steps (Fig.3). We call this hold device the approximated fractional order hold or AFROH [7].

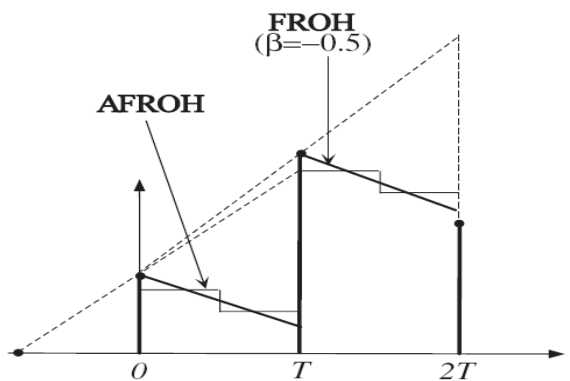


Fig. 3 Hold function of a FROH and a two step AFROH approximation.

Being N the number of steps to approximating the hold linear function, we can write:

$$u(t) = \left(1 + \frac{2l-1}{2N} \right) \beta u(kT) - \left(\frac{2l-1}{2N} \right) \beta u((k-1)T) \quad (2)$$

$$\left(k + \frac{l-1}{N} \right) T \leq t \leq \left(k + \frac{l}{N} \right) T \quad (3)$$

$l = 1, \dots, N$

Obviously, the more steps the device is able to produce, the better and smoother approximation to the continuous ideal function is obtained.

In order to estimate the number of steps the digital hold device should produce for approximating the hold function, we analyzed the behavior of a hybrid closed-loop control system including a FROH device. We chose two application examples published in [8] where the response of a second order plant and a more complex fourth order plant, both controlled by a two-degree-of-freedom (a.k.a RST) digital controller is described. The referred work shows the performance improvement of the system when using a properly tuned FROH compared to the same system with a conventional ZOH. The tuning method for β proposed in [8] is based on a frequency domain analysis that allows the improvement of the continuous-time closed-loop performance of the system.

3.1 A simple case

The dynamic of the first plant is described by a second order transfer function,

$$G(s) = \frac{1}{s(s+1)} \quad (4)$$

which has one ZOH discretization zero. The selected sampling period was $T = 0.1s$. The gain parameter of the FROH is adjusted to

Figure	ZOH	FROH	AFROH_2	AFROH_4	AFROH_8	AFROH_16	AFROH_32	AFROH_64
$t_{s,5\%}$	296 ms	160 ms	957 ms	279 ms	247 ms	155 ms	157 ms	159 ms
OS	23.25 %	3.31 %	16.64 %	4.40 %	1,91 %	1.94 %	2.60 %	2,95 %
Energy	6,479	2,906	7,291	4,298	3,499	3,182	3,039	2,971

Table 1: Obtained continuous-response performance figures for the digitally controlled-plant described by (3) for different hold devices.

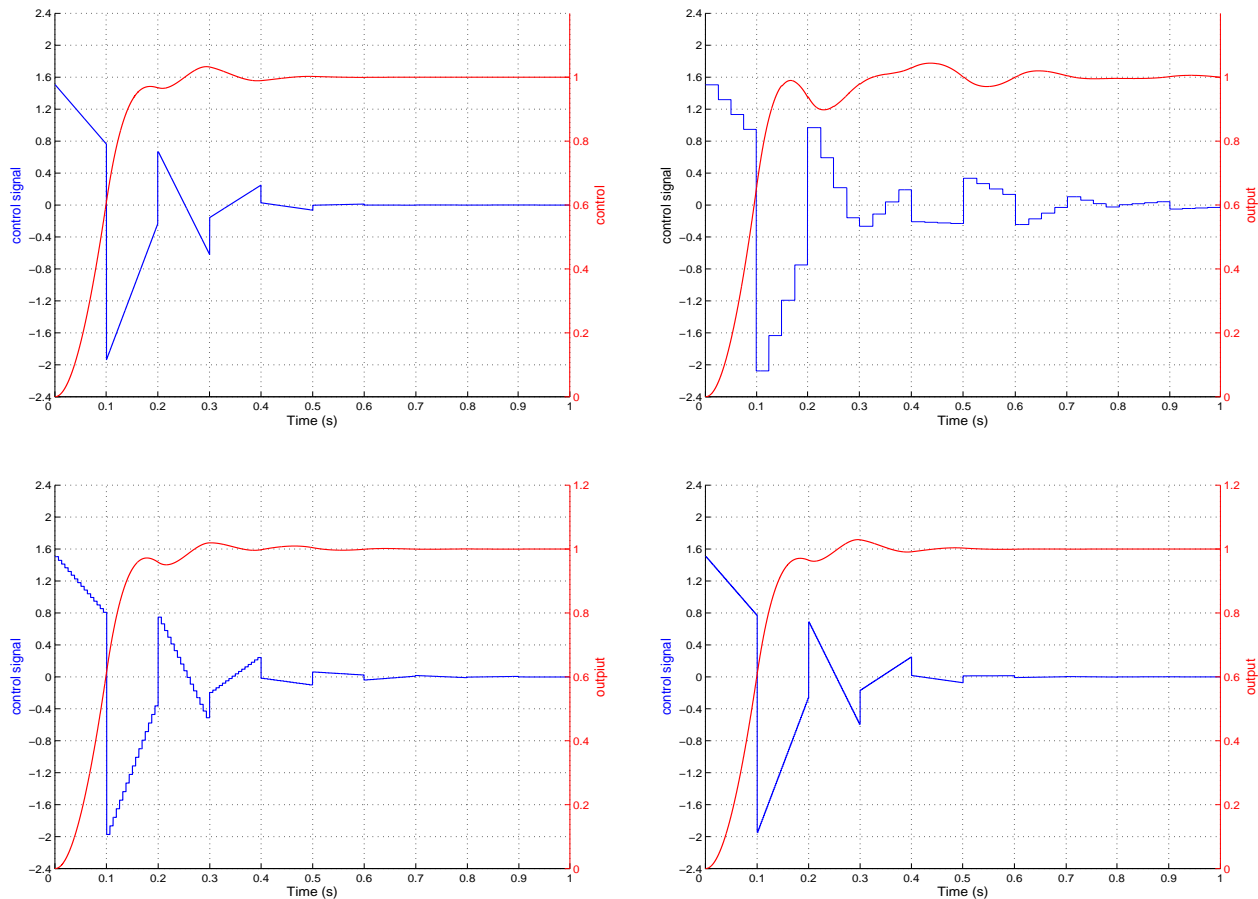


Fig. 4: Continuous-time plant (4) output for an unitary step input and produced control signal by the digital RST controller for different fractional order hold devices: continuous FROH (top left), 4 step AFROH (top right), 16 step AFROH (bottom left), and 64 step AFROH (bottom right).

$$\beta = -0.493743 \quad (5)$$

and the RST digital controller polynomials are fitted to obtain a convenient output response. Performed simulations show the superiority of the continuous time domain response of the system using the FROH device (see details in [8]).

To perform the experimentation with the AFROH and to analyze the influence of the number of approximating steps on system performance, we substituted the model block of the continuous FROH used in the above mentioned example with a model of the AFROH with an adjustable step number parameter N . We compared the obtained results to the figures obtained for the continuous FROH in order to estimate an adequate maximum value for N in the design of the AFROH digital device. Table 1 shows obtained continuous time response performance figures when applying a unitary step at the input for the analyzed cases: ZOH, continuous FROH (machine accuracy), 2 step,

4 step, 8 step, 16 step, 32 step and 64 step approximations (AFROH). Selected performance figures for comparison were settling time (5% criterion), overshoot and energy consumed during the transient.

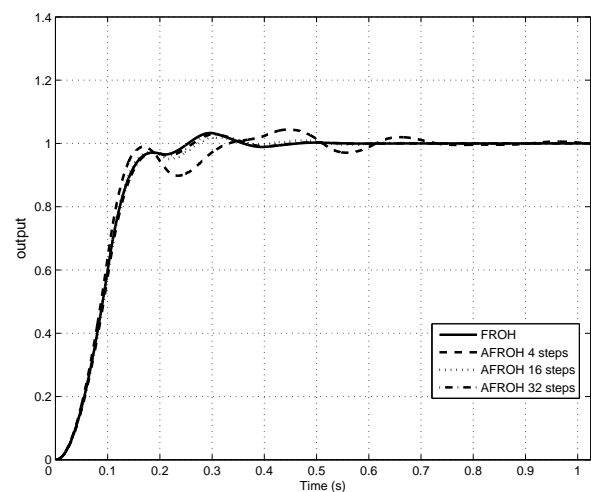


Fig. 5: Output signals comparison graph for the plant described by (4)

Figure	ZOH	FROH	AFROH_2	AFROH_4	AFROH_8	AFROH_16	AFROH_32	AFROH_64
$t_{s,5\%}$	313 ms	239 ms	NaN	587 ms	236 ms	237 ms	238 ms	238 ms
OS	10.89 %	2.07 %	16.64 %	7.63 %	3.65 %	1.98 %	2.01 %	2,03 %
Energy	110,314	66,140	128,400	80,497	70,717	67,892	66,891	66,485

Table 2: Obtained continuous-response performance figures for the digitally controlled-plant described by (4) for different hold devices.

From Table 1 we can conclude that an adequate performance, that is, similar to that obtained with the continuous FROH, begins to happen with a 16 step approximation (4 bit timing resolution for a digital design). Below this resolution, the adjustment of β , analytically obtained for the continuous model, is not adequate for the approximated model. Graphical representations of the control signals and the controlled plant outputs are shown in Fig.4 for selected cases. A comparison of produced plant output behavior is depicted in

Fig.5 for the same approximation resolutions.

3.2 A more complex case

The fourth relative order plant model proposed for this application example is described by,

$$G(s) = \frac{100}{s(s^3 + 19.9s^2 + 98.25s - 10.025)} \quad (6)$$

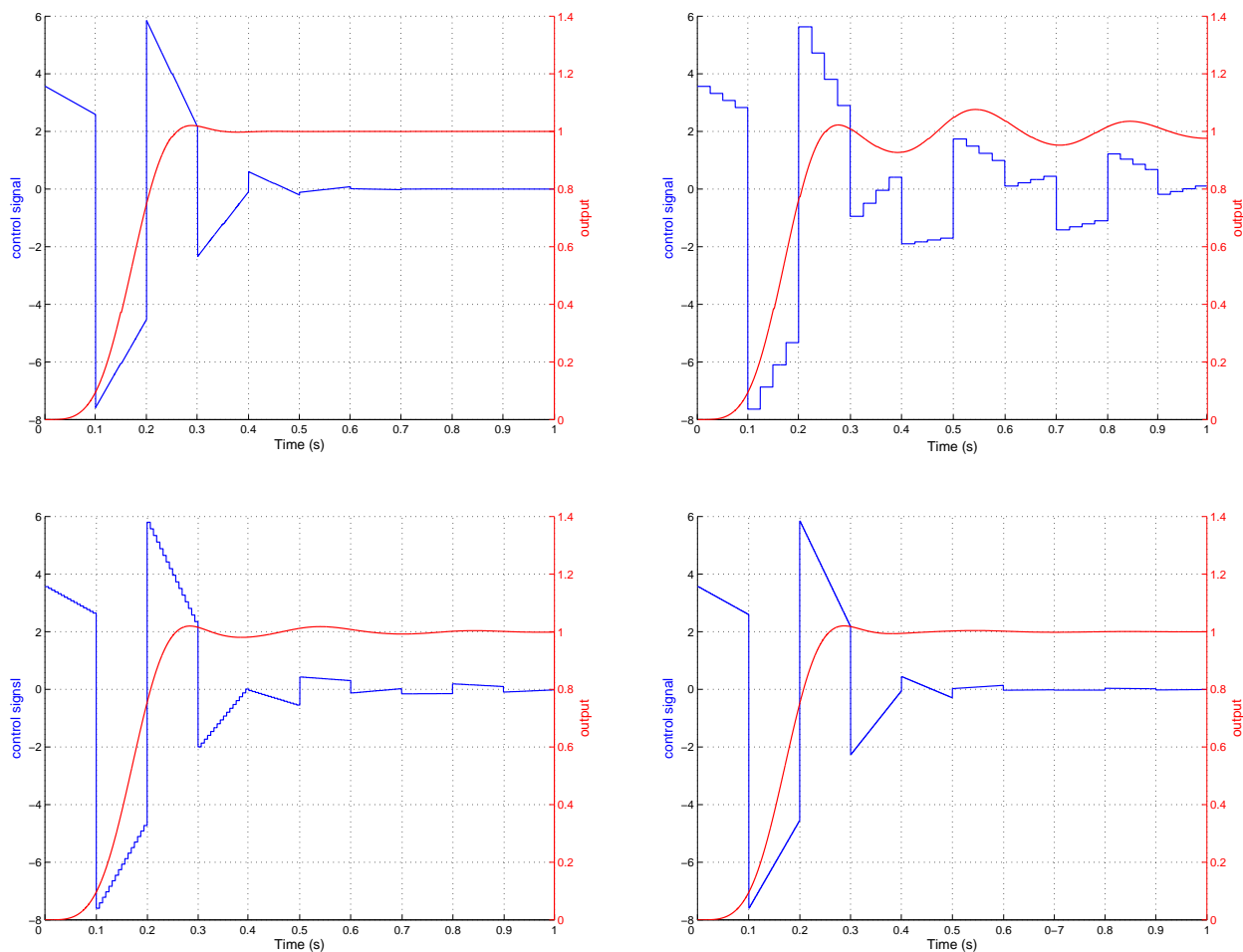


Fig. 6: Continuous-time plant (6) output for an unitary step input and produced control signal by the digital RST controller for different fractional order hold devices: continuous FROH (top left), 4 step AFROH (top right), 16 step AFROH (bottom left), and 64 step AFROH (bottom right).

