Optimal Voltage Assignment Approach for Low Power Using ILP

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Abstract: - In this paper, we proposed an optimal voltage assignment approach which determines the proper voltage for each gate in the gate level netlist using dual supply voltages. To the best of our knowledge, it is the first work to integrate the impact of the level shifters into the integer linear programming (ILP) formulations. The objective of the paper is to minimize the total power, including the gates and the level shifters, under the given delay constraints. For the gate level netlist, the voltage assignment approach, which determines the delay for gates and wires and the power for the gates and level shifters, is proposed. To reduce the runtime for the ILP constraints, we also propose the node-based concept to formulate the timing constraints. Finally, we optimally assign the voltages for all gates. The ILP formulations are solved by using the ILP solver (LINGO 10.0) and the experimental results with ISCAS circuits indicate the significant improvement on total power using the dual supply voltages.

Key-Words: - Dual Voltage, Low Power, Timing Constraint, Integer Linear Programming, Delay, Optimal

1 Introduction

Power is an emergency issue for the modern integrated circuit design. Obviously, the high speed devices have the high power consumption and vice versa. To enlarge the standby time for the portable electronic equipments, we should minimize the total power. On the other hand, the specifications for timing will also be kept when we reduce the power consumptions. It means that we need to take tradeoff between the power consumption and the chip performance. According the low-power timing-driven relative papers, the most effective method is the multiple supply voltages technique and it has been proposed to minimize the power consumption [1].

Recently, the multiple voltage assignment methods are proposed to reduce the power consumption in the physical design, such as the high level synthesis [2][3], gate level synthesis [4], floorplanning stages [5], placement [6] and the transistor level circuits [7]. Some approaches minimize the total power by utilizing the heuristic methods [1][6][7][8]. Without the global view, the authors presented the greedy method to assign the voltage for each gate by considering the sensitivity of gate [8]. Kulkarni *et al.* studied two previous works and proposed an ECVS-based approach to further reduce the power for the gate-level netlist

using only two supply voltages [9]. However, some methods only handled the two supply voltages and usually did not obtain the optimal voltage assignment.

In contrast to the greedy methods, some researches proposed the integer linear programming (ILP) method to optimize the user-defined objectives [10], including minimization of the total power consumption [11][12][13]. The authors proposed ILP formulations to reduce the leakage power and insert the buffer to improve the glitch power [11]. Nguyen et al. provided the three-stage approach, including the ILP formulations to assign the supply voltage to each gate, but they did not consider the impact of level shifters under two supply voltages [12]. Chai and Kuehlmann proposed the ILP formulations and applied them to solve two problems, including the minimization of leakage and peak current [13]. However, the runtime of the ILP-based ways are inefficient because they do not consider the volumes of constraints.

The main contributions of our ILP-based formulations are as follows. First, we propose a novel concept of the node-based approach to reduce the volumes of timing constraints and our method efficiently obtains the assignment for the dual voltages. Second, our proposed approach both

efficiently obtains the optimal solution and effectively improves the total power. Third, our ILP-based method can be easily extended to integrate the level shifters into the ILP constraints.

The organization of the paper is as bellow. Section 2 formulates the voltage assignment problem and defines some terminologies in our ILP formulations. The ILP-based formulation and a simple example are given in Section 3. Finally, the experimental results and the conclusions are attached in Section 4 and 5.
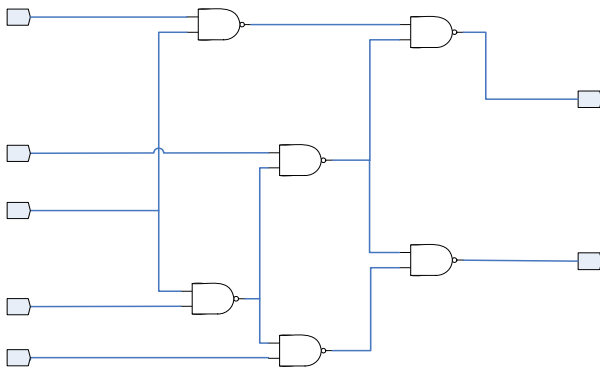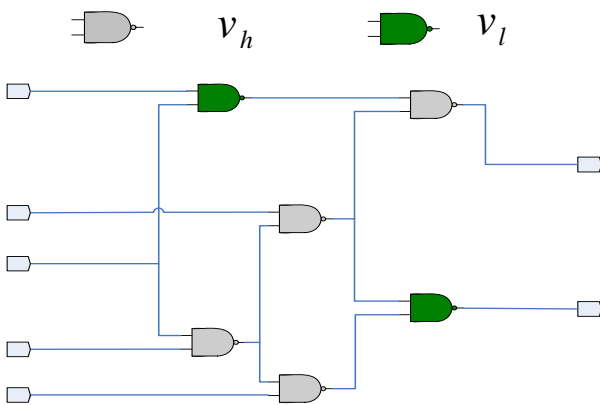

Figure 1. A gate level netlist by using NAND gate.

Figure 2. A voltage assignment for low power.

2 Preliminary

In this section, we discuss the motivation, terminology used in the ILP formulations and define the low power voltage assignment problem.

2.1 Motivation

In the gate level netlist, we transform the connection between the gates into the ILP formulations. Our ILP formulations can achieve the optimal voltage assignment using the dual supply voltages. Traditionally, the previous works usually greedily find the voltage assignment, but the solutions are not optimal or near-optimal. Hence, we want to formulate the voltage assignment problem into the ILP formulations which achieve the optimal solution. Under the two kinds of voltages (v_h and v_l), we will assign the proper voltage for each gate in Figure 1(a). We know that if the timing constraints can be transformed into the integer linear programming, the optimal voltage assignment can be found under the given timing constraints. Figure 1(b) shows the optimal voltage assignment to meet the timing constraint by using three supply voltages. This example in Figure 1 motivates us how to solve the dual supply voltage assignment problem by the integer linear programming to find the optimal solution.

2.2 Terminology

We apply ILP formulation to model the dual supply voltage problems to minimize the total power with the timing constraints. Two binary variables x_i^h and x_i^l are the 0/1 integer variables. In this subsection, we will define the terminology as follows.

$G = \{g_1, g_{2,\dots}, g_{|G|}\}$: the set of gates

$W = \{w_1, w_{2,\dots}, w_{|W|}\}$: the set of wires

$L = \{l_1, l_{2,\dots}, l_{|W|}\}$: the set of level shifters and

l_i means the level shifter on wire w_i

$d(g_i)$: delay of gate g_i

$d(w_i)$: delay of wire w_i

$p(g_i)$: power of gate g_i

$v(g_i)$: voltage of gate g_i

$p(l_i)$: power of level shifter l_i

If $l_i = 0$, it means that there is no level shifter on wire w_i, otherwise there is one level shifter on wire w_i.

$d_{path}(g_i, g_j)$: the path delay from g_i to g_j

$d_{path}(g_i) = \max\{d_{path}(g_i, g_j) \mid g_i \in PI$

and there is a path from g_i to $g_j\}$:the fanout delay of gate g_i. We add a level shifter to keep the voltage stability for the voltage conflict between the

low to high voltages.

$$P_{gate} = \sum_{i=1}^{|G|} p(g_i) : \text{the power consumption of all}$$

gates

$$P_{level\_shifter} = \sum_{i=1}^{|W|} p(l_i) : \text{the power consumption of}$$

all level shifters

$$P_{total} = P_{gate} + P_{level\_shifter} : \text{the total power}$$

consumption of the gate level netlist.

D_{con} : the delay constraint of the netlist.

Besides, $x_i^h = 1$ ($x_i^l = 1$), if the gate is assigned the high (low) supply voltage, otherwise $x_i^h = 0$ ($x_i^l = 0$) the gate is not assigned the high (low) supply voltage. We know that $1 \le i \le n$, where n denotes the number of gates.

2.3 Problem definition
The gate level netlist which is composed by the multiple functions logic gates, is formulated as a DAG (directly acyclic graph). Given a G = (V, E), which V and E are the n gates and the m wires, respectively. For a gate i with dual supply voltages has dual power consumptions and dual gate delays. Under the timing constraints of all routing paths, our objective is to optimize the total power consumption of all gates and level shifters under the dual supply voltages.

3   Our ILP Formulation
In this section, we will describe the ILP-based method in detail. Three advantages of our approach are listed in the next sub-section. Furthermore, we give a sample to demo the concept of our algorithm.

In our ILP formulations, l_i is a binary variable to represent if there is a level shifter on w_i:

$$l_i = \begin{cases} 1 & \text{if there is a level shifter on } w_i; \\ 0 & \text{otherwise.} \end{cases} \quad (1)$$

Hence, our objective function is defined as follows,

3.1 Objective function
In this paper, we define the dual voltages assignment problem as follows,

$$\text{Minimize } (\alpha \times P_{gate} + \beta \times P_{level\_shifter}) \quad (2)$$

Subjective to

$$x_i^h \in \{ 0, 1 \}; \quad x_i^l \in \{ 0, 1 \} \quad (3)$$

$$d(g_i) = x_i^h \times d^h(g_i) + x_i^l \times d^l(g_i); \quad (4)$$

$$p(g_i) = x_i^h \times p^h(g_i) + x_i^l \times p^l(g_i); \quad (5)$$

$$P_{gate} = \sum_{i=1}^{|G|} p(g_i) \quad (6)$$

$$d_{path}(g_i) = \max\{d_{path}(g_i, g_j) \mid g_i \in PI \} \quad (7)$$

$$M \times (1 - l_k) + (v\_g_j - v\_g_i) > 0; \quad (8)$$

$$M \times (l_k) + (v\_g_i - v\_g_j) \ge 0; \quad (9)$$

$$P_{level\_shifter} = \sum_{i=1}^{|W|} p(l_i) \quad (10)$$

where P_{gate} and $P_{level\_shifter}$ are the power of the total gates and the level shifters. All constraint are discussed as follows in detail,

3.2   Integer constraints
In the paper, some 0/1 binary variables are described. The binary variables are as following, x_i^h and x_i^l are used to determine the supply voltages for each gate i. l_i is applied to determine if there is a level shifter will be inserted on the wire w_i.

3.3   Delay constraints for gates
In our ILP formulations, the delays are assigned to respond to the high and low supply voltages. Hence, the delay of each gate is determined as the follows,

$$d(g_i) = x_i^h \times d^h(g_i) + x_i^l \times d^l(g_i); \qquad (11)$$

$$x_i^h + x_i^l = 1; \qquad (12)$$

where $d^h(g_i)$ and $d^l(g_i)$ denote the gate delay

responding to high and low supply voltages.

3.4 Power constraints for gates

In this paper, the powers are also assigned to respond to the high and low supply voltages. Therefore, for a single gate, the power consumption is represented as follows,

$$p(g_i) = x_i^h \times p^h(g_i) + x_i^l \times p^l(g_i); \qquad (13)$$

$$x_i^h + x_i^l = 1; \qquad (14)$$

Then, the total power of all gates are given as follows,

$$P_{gate} = \sum_{i=1}^{|G|} p(g_i) \qquad (15)$$

where p^h, p^l and P_{gate} represent the power of

gate with the high, low supply voltage and the total

power of gates, respectively.

3.5 Delay constraints for the paths

Traditionally, for the all paths, we list all devices, such as the gates, wires and level shifters. Hence, we obtain the ILP constraints of delay for all paths as follows,

$$\max\{d_{path}(g_i, g_j) \mid \qquad g_i \in PI, \ g_j \in PO\} \le D_{con} \qquad (16)$$

However, for the large size gate level netlist, the edges information is so huge that the ILP solver (LINGO) is not able to load the ILP constraints. It means that it is not suite to list all timing constraints by the path-based concept because the number of the ILP constraints is grown exponentially. Hence, we have to reduce the

number of the ILP constraints. For the problem, we present a node-based method to reduce the volumes of ILP constraints. A novel node-based concept, which just checks the timing relationship for the neighbor gates, is provided to improve the ILP constraints.

In Figure 3, the delay of the primary output (PO) of the gate is defined and applied to reduce the volumes of ILP constraints. For gate 1 and gate 2, the delay of the primary output (PO) is named as "$d_{path}(g_1)$" and "$d_{path}(g_2)$", respectively. Instead of the path-based idea, the relationships between the gate 1 and 2 are as follows,

$$\begin{cases} d_{path}(g_1) + d(w_1) + d(g_3) \le d_{path}(g_3) \\ d_{path}(g_2) + d(w_2) \le d_{path}(g_3) \\ d_{path}(g_i) \le D_{con} \end{cases} \qquad (11)$$
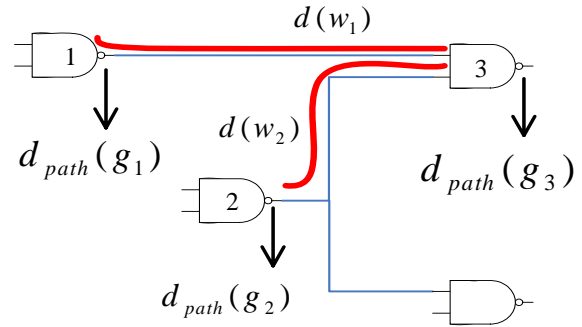

Figure 3. The node-based ILP constraints

3.6 Power/delay constraints for level shifter

After solving the previous problem, we check the voltage relationship and determine if we have to insert the level shifter for the edge w_k which connects the nodes x_i and x_j by using the binary variable l_k. In this paper, we only discuss for the dual supply voltages.

Actually, our ILP formulations can extend to formulate the k ($k>=2$) voltages and get the optimal solution. For the ILP formulation, it is useful to translate the if-then-else statement into our ILP constraints. The following is the corresponding constraints,

$$\begin{aligned} &if \ (v(g_i) \ge v(g_j)) \\ &\qquad l_k = 0; \\ &else \\ &\qquad l_k = 1; \end{aligned} \qquad (12)$$

For convenience, we can use the following notions to represent the variables into the above formula.

$$v\_g_i = v(g_i) \qquad (13)$$

$$v\_g_j = v(g_j) \qquad (14)$$

The formula can be rewrote as follows,

$$
\begin{aligned}
&if\ (v\_g_i \geq v\_g_j) \\
&\qquad l_k = 0; \\
&else \\
&\qquad l_k = 1;
\end{aligned}
\qquad (15)
$$

To formulate the above statement, we add an upper bound M, which is a constant larger than the value of $|v\_g_i - v\_g_j|$. Hence, we have the following constraints,

$$
\begin{cases}
M \times (l_k) + (v\_g_i - v\_g_j) \geq 0 \\
M \times (1 - l_k) + (v\_g_j - v\_g_i) > 0
\end{cases}
\qquad (16)
$$

According to the above discussion, the ILP formulations are easily to integrate the level shifter (v_g_i and v_g_j are supply voltages, respectively). By considering the impact of level shifter, the ILP constraints for the relationship among the gate 1, 2 and 3, can be rewrote as follows,

$$
\begin{cases}
d_{path}(g_3) \geq d_{path}(g_1) + d(w_1) + \\
\qquad\qquad d(l_1) + d(g_3); \\
d_{path}(g_3) \geq d_{path}(g_2) + d(w_2); \\
D_{con} \geq d_{path}(g_3);
\end{cases}
\qquad (17)
$$

where $d(l_1)$ and $d_{path}(g_3)$ denote the delay of level shifter and the delay for primary output of the gate 3, respectively. Besides, $d(w_1)$ is the wire delay of wire w_1.
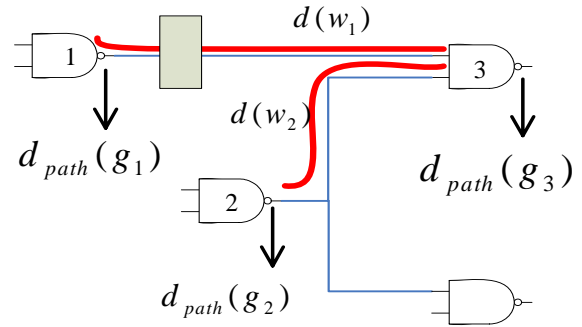

Figure 4. The node-based ILP with level shifter

Therefore, the total power of level shifters are summarized as follows,

$$P_{level\_shifter} = \sum_{i=1}^{|W|} p(l_i) \qquad (18)$$

where $P_{level\_shifter}$ and $p(l_i)$ are the total power consumption of the level shifters. For example, in Figure 5(a), the wire w_k between gates g_i and g_j should be inserted a level shifter if the low supply voltage is assigned to gates g_i and the high supply voltage is assigned to g_j, respectively. Hence, the binary value l_k is assigned to be 1, otherwise assigned to be 0.
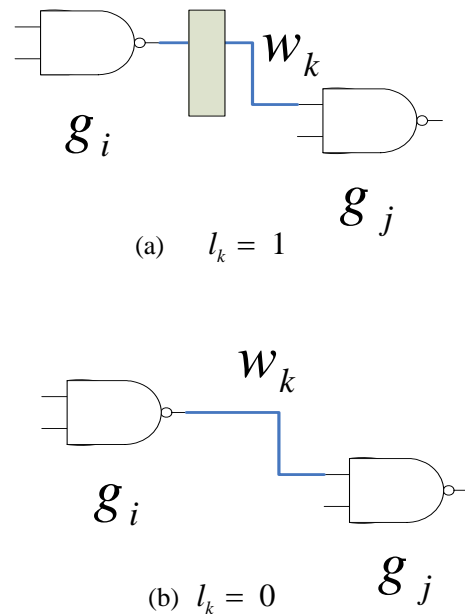

(a) $l_k = 1$

(b) $l_k = 0$

Figure 5.   The level shifter assignment on the wire w_k.

4 An example for ILP formulations

In a chip design (Figure 6), the gate delays of the high supply voltage are randomly assigned from 1000ps to 9000ps. The wire delays are assigned from 1000ps to 9000ps.The power consumption for the gate is generated by the formula which described the relationship between the delay and power. Furthermore, we ignore the power and delay of the level shifter because we do not have the exact technique parameters. Because our ILP formulation can consider the level shifter, see subsection 3.6. It is easily to integrate the effect of the level shifters when we receive the confident parameters of the level shifter. We give the timing constraints 52000ps (=52ns) for each routing path and the delay of each path must be less than 25000. In fact, our ILP formulations still work normally even though the delay and power data for the gates and wires. Therefore, our approach is effective to find the solution when the post-placement stage is performed to back annotate. Because of lack the delay and power data for the ISCAS circuits, we randomly assigned the delay for the gates (for the high and low supply voltages) and assign the power of the gates by the formula. We also ignore the input transaction and output loading when the supply voltages of some gates are changed. In the section, we describe the circuit example for the problem, the whole ILP formulations for the example under the power and timing constraints mentioned above, the model selection for the example and discuss the optimal solution for the example, respectively.

4.1 Program description

The problem data contains the delay constraints for the gates and wires, the power constraints for gates and the voltage constraints for the level shifters. In the example, the gate delays for the primary inputs (PI) and primary outputs (PO) are also given the same as the interior gates. Furthermore, the total power consumption of the gates, including the PI, PO, interior gates, can be optimized. Finally, the delays of all paths, must be satisfied with the delay constraints.

4.2 The ILP formulations

The objective of the paper is to minimize the total power consumption, including the PI, PO and interior gates. The partial ILP formulations for the example are given as follows,

```
min=Gchpow0+Gchpow1+Gchpow2+Gchpow3+Gchpow4+
    Gchpow5+Gchpow6+Gchpow7+Gchpow8+Gchpow9+
    Gchpow10;

!delay constraint for all paths;
Gdly_con=52000;

! delay for gates constraints;
Ggdly1_0=2000;
Ggdly1_1=3000;
Gdlyra1_2=5;
Ggdly2_0=(Ggdly1_0*Gdlyra1_2)/4;
Ggdly2_1=(Ggdly1_1*Gdlyra1_2)/4;
!power for gates are assigned;
Gpow1_0=3600;
Gpow1_1=1600;
Gpowra1_2=2;
Gpow2_0=(Gpow1_0*Gpowra1_2)/4;
Gpow2_1=(Gpow1_1*Gpowra1_2)/4;

!0/1Binary variable ;
Bx1_0+Bx2_0=1;
Bx1_1+Bx2_1=1;

!delay selection for gates;
Gchdly0=Ggdly1_0*Bx1_0+Ggdly2_0*Bx2_0;
Gchdly1=Ggdly1_1*Bx1_1+Ggdly2_1*Bx2_1;
Gchpow0=Gpow1_0*Bx1_0+Gpow2_0*Bx2_0;
Gchpow1=Gpow1_1*Bx1_1+Gpow2_1*Bx2_1;

!node_based delay constraints;
Gtime0+Gwdly0_4+Gchdly4<=Gtime4;
Gtime1+Gwdly1_11+Gwdly11_4+Gchdly4<=Gtime4;
Gtime1+Gwdly1_11+Gwdly11_6+Gchdly6<=Gtime6;
Gtime2+Gwdly2_5+Gchdly5<=Gtime5;
```

4.3 Model selection

The selection results are obtained by the LINGO 10. The objective of the example is 21966. The result captured is as follows,

Global optimal solution found at iteration: 59
Objective value = 21966
Non-zero variables:

Variable	Value	Meaning
BX1_0	0.000000	0.000000
BX2_0	1.000000	0.000000

The variables denote which kinds of supply voltage are assigned to the gates. For example, BX1_1 and Bx2_1 denote the binary variables for gate 1 and gate 1 is assigned to the low supply voltage. It means that the optimal voltage assignment under the dual supply voltage is 21966. Our ILP formulations can find the optimal solution efficiently according the discussion of node-based concept.
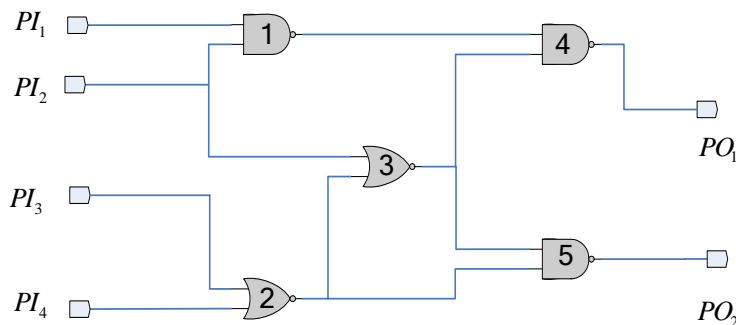
4.3 Level shifter assignment

Compared to the voltage assignment with all high supply voltages, our ILP-based method can optimize the total power consumption, including the dynamic power for gates and level shifters. In Figure 6(b) the power consumption with all high supply voltage is 39704. Actually, some gates located at the non-critical path can be replaced to the low supply voltages. In Figure 6(c), gates 1 and 5 are replaced to the low supply voltage and the total power consumption is reduced to 23166. Hence, we observe that our ILP formulations can find the optimal solution. Besides, we can keep the voltage constraints between the low and high supply voltages and only three level shifters are needed by our ILP formulations. We observe that all the other methods obtain the higher cost the optimal solution.
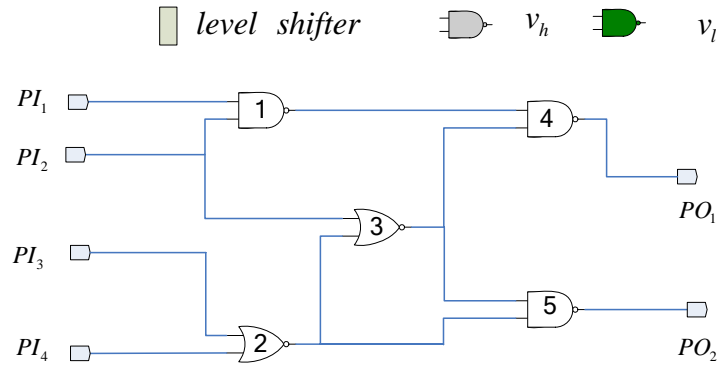
(a) An original gate level netlist

(b) All gates with the high supply voltages
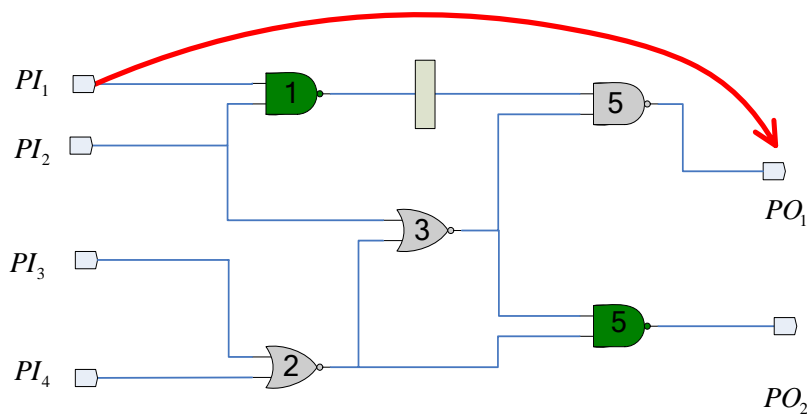
(c) A level shifter is added under dual supply voltages

Figure 6.   Illustration of the voltage assignment under timing constraints.

Table I.   Improvement on the total power under one and dual supply voltages ($\beta = 0$).

	Primary input	No. of gate	Total power consumption			Runtime(sec.)
			I	II	IMP (%)	II
c17	5	13	57704	37528	35.0	0
c432	36	203	798112	445646	44.2	1
c499	41	275	1040652	542668	47.9	1
c880	60	469	1873268	974912	48.0	0
c1355	41	619	2564292	1365554	46.7	2
c1908	33	938	3925828	2022810	48.5	2
c2670	233	1566	6584296	3345778	49.2	3
c3540	50	1741	7349824	3817040	48.1	2427
c5315	178	2608	11273770	5804380	48.5	8
c6288	32	2480	10625050	5663668	46.7	28
c7552	207	3827	16213990	8192718	49.5	3600
avg					46.6	552

I and II denote the one and dual supply voltage. IMP(%) denotes the improvement on the power.

Table II. The Optimal Power under the Relaxing Delay Constraints ($\beta = 0$)

	$1.05 \times D_{max}$			$1.10 \times D_{max}$			$1.20 \times D_{max}$			$1.30 \times D_{max}$		
	I	II	IMP	I	II	IMP	I	II	IMP	I	II	IMP
c17	57704	29428	49.00	57704	29140	49.50	57704	28852	50.00	57704	28852.00	50.00
c432	798112	399920	49.89	798112	399056	50.00	798112	399056	50.00	798112	399056.0	50.00
c499	1040652	520902	49.94	1040652	520326	50.00	1040652	520326	50.00	1040652	520326.0	50.00
c880	1873268	938812	49.88	1873268	936634	50.00	1873268.	936634	50.00	1873268	936634.0	50.00
c1355	2564292	1283586	49.94	2564292	1282146	50.00	2564292	1282146	50.00	2564292	1282146	50.00
c1908	3925828	1965218	49.94	3925828	1962914	50.00	3925828	1962914	50.00	3925828	1962914	50.00
c2670	6584296	3294164	49.97	6584296	3292148	50.00	6584296	3292148	50.00	6584296	3292148	50.00
c3540	7349824	3676640	49.98	7349824	3674912	50.00	7349824	3674912	50.00	7349824	3674912	50.00
c5315	11273770	5643510	49.94	11273770	5636886	49.99	11273770	5636886	49.99	11273770	5636886	49.99
c6288	10625050	5315694	49.97	10625050	5312526	49.99	10625050	5312526	49.99	10625050	5312526	49.99
c7552	16213990	8109586	49.98	16213990	8106994	50.00	16213990	8106994	50.00	16213990	8106994	50.00

I and II denote the one and dual supply voltage. IMP(%) denotes the improvement on the power

5   Experimental Result

For considering the impact of the level shifters, our ILP formulations are automatically generated by using C++ language and solve the ILP constraints by LINGO 10 [14] on the Intel Core2 CPU 1.86GHz 1.87GHz machine with the 3GB memory. For the LINGO 10, we modify the relative parameters for convergence without degenerating the quality of voltage assignment. The objective is to optimize the total power under the timing constraints. Because of the lack of the gate delay information for the ISCAS benchmarks, the delays of the gates and wires are randomly assigned. For the power of gates, we also randomly assign the power consumption for each gate. Besides, we ignore the loading effects of the level shifters after inserting the level shifters to the routing paths and just integrate the impacts of the level shifters into our ILP constraints. Because we lack the level shifter's information, such as the delay and power, we assume the weight β for the level shifter is zero. In section 3, we explain in detail that why our ILP formulations can handle three supply voltages under the timing constraints.

First, we investigate the improvement on total power consumption among the dual supply voltages. In Table I, the symbols I and II represent the voltage assignment under the one and dual supply voltages. Compared to total power consumption under all high supply voltages, the improvement on the power consumption of II is 46.6% in average. To show clearly, we draw the improvement on total power in Figures 7 and 8. We observe that the average improvement on power is close to the 50%, i.e. the power ratio from the high to low supply voltages. Because our ILP formulations need to meet the timing constraints, some gates located at the critical paths are assigned to the high supply voltages.

Second, by applying the node-based concept, the volumes of our ILP constraints are significantly reduced and the LINGO solves the ILPP constraints very efficiently. For the benchmark with one supply voltage, we get the optimal solution efficiently. Furthermore, for the large benchmarks under the dual supply voltages, we achieve the optimal solutions in accepted runtime.

Third, we investigate the improvement on total power consumption under the different timing constraints, i.e. the relaxing timing constraints. In Table II, we examine our ILP formulations under the different timing constraints ($1.05 \times D_{max}$, $1.10 \times D_{max}$, $1.20 \times D_{max}$ and $1.30 \times D_{max}$, where D_{max} denotes the maximum delay under the one supply voltage, i.e. all gates are assigned the high supply voltages). From the table, we observe that the total power consumptions are significantly improved. Because the power ratio of the high to middle supply voltage are given as the 0.5, the upper bound of the total power improvement is 50%. It means that all gates

are changed their high supply voltages to the middle supply voltages. Similarly, the delay ratio from high to middle supply voltage is 1.25, the upper bound of improvement on the maximum delay is $1.25\,D_{max}$. From the table, compared to timing constraint $1.2\,D_{max}$, we observe that there is almost no improvement on power consumption under $1.3\,D_{max}$.

To explore the improvement trend of total power consumption in detail, we plot the power improvement results under the different timing constraints in Figure 9 by using the C7552 benchmark. From the Figure 8, the curve denotes the improvement on total power. Actually, there is no improvement under the $1.20\,D_{max}$ and $1.30\,D_{max}$. This is because the gates located at the critical path have been changed to the low supply voltages.

6   Conclusion and Future Work

In the paper, we present an optimal voltage assignment approach to optimize the total power consumption, including the gates and the level shifters. For a gate level netlist, our ILP formulations automatically optimize the voltage assignment for each gate under dual supply voltages. Compared the traditional path-based concept for the constraints of all routing paths, the ILP formulation can achieve the optimal assignment solution efficiently. Compared to the result of all high supply voltage assignment, we discover that the power consumption is further minimized by 46.6%. Hence, our ILP formulations are both efficient and effective obtain the optimal solution with the accepted runtime because we reduce the volumes of ILP constraints by using the node-based concept.

The ILP formulations can easily extend to handle the multiple supply voltages to minimize the circuit performance under the power consumption constraints. Besides, we also easily incorporate the impact on the several level shifters.

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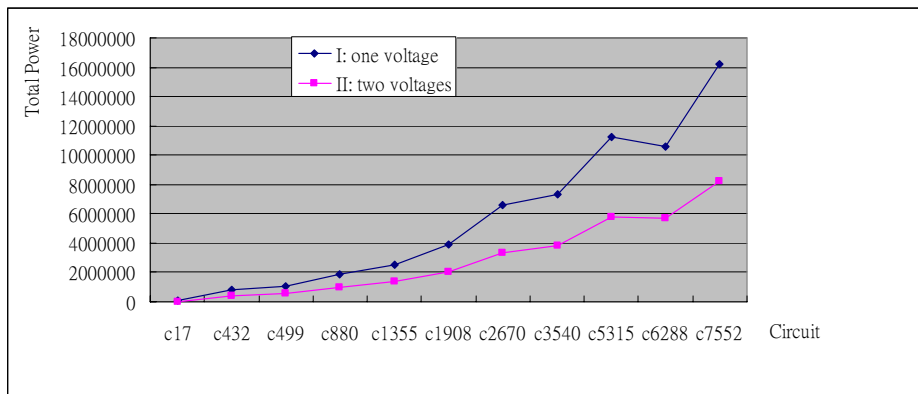[14] *LINGO user's guide*, LINGO systems inc.

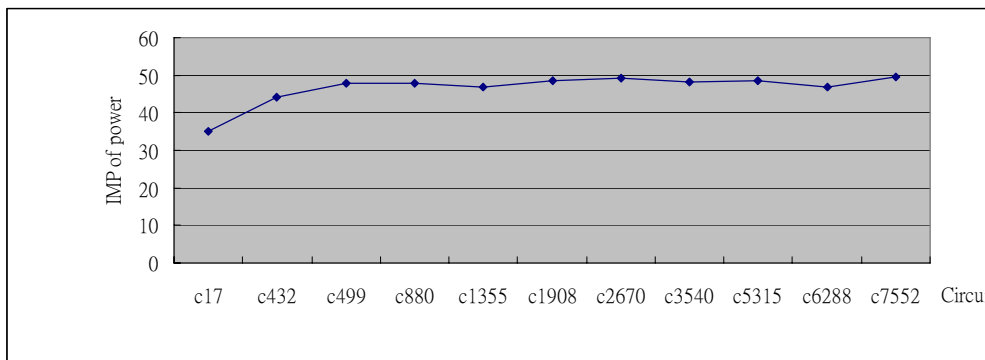Figure 7. The total power consumption under one and dual supply voltages.

Figure 8. The improvement on power consumption under one and dual supply voltages.
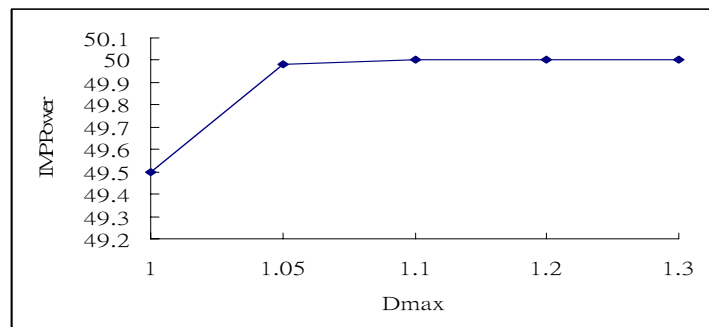

Figure 9. Power improvement under the relaxing delay constraints (C7552).