Behavioural Modelling of On-Chip Optical Interconnect with Potential Applications for Testing Linking-with-Light Circuits and Systems

HJ KADIM School of Engineering LJMU Liverpool L3 3AF, UK *h.j.kadim@ljmu.ac.uk*

Abstract - An integrated circuit (IC) or a system where light beams displace wires or metallic interconnects to pass signals between different subsystems requires new test techniques. Based on a knowledge of light properties and the transmitting medium, possible factors or parameters that may affect the propagation of light and the consequent changes in the expected output can be identified. Using these parameters as the ingredients, a mathematical model is constructed to study the effect of parameter fluctuations on the on-chip optical interconnect and hence providing information that will assist in identifying abnormal deviations in circuit's behaviour.

Key-Words: - Optical interconnect, test, modelling, parameter fluctuations, SoC

1 Introduction

The benefits of miniaturisation, higher packing densities, higher circuit speeds, and lower power dissipation have been keys in the evolutionary progress leading to todays' computers and communication systems. These systems offer superior performance, reduced cost per function, and reduced physical size, in comparison with their predecessors. However, communication within a computer is by moving data across electrical connectors, which have a lower bit rate compared to that of the computer's microprocessor. A microprocessor may process data at an extraordinary rate, but this is compromised when data travel over the copperconnections that link the processor to local memory or peripherals, by the order of 1:10. The bit-rate of electrical connectors is influenced by a number of parameters such as parasitic resistance, capacitance, and inductance [1][2][3]. All these parasitic factors depend heavily on the geometry of the wire, and hence influence the bit rate. This dependency on geometry puts constraints on the bit rate. For instance, the bit rate is proportional to the cross section of a wire, but falls with the square of its length. An increase in the cross-section of a wire to accommodate high rate of data is not an option considering the growing demand for highly dense integrated circuits. The gap between the bit rate for a wire and that of, for instance, a microprocessor-core will increase considerably with the continual development in semiconductor technology and processor architecture. Hence, wires as a means for signal transfer cannot allow for the realisation of full potential of next generation computing systems. Therefore, communication between printed circuit boards (PCB), computers, chips within a PC, and intellectual property (IP) cores within systemon-a-chip (SoC) is to be based on photons rather than electrons for passing signals.

The idea of passing data signals between source and destination is similar to that of telecommunications systems. A light beam is modulated with an electrical signal using, for example, a laser diode. The modulated light beam passes through a set of lenses and then through a transmitting medium to be collected and directed by another set of lenses to be received and converted into an electrical signal using a photodiode. Fig.1 shows the basic principles of the electronic/optical interconnect.





Linking-with-light circuits and systems have the advantage over metallic solutions in that the circuit/system can easily be reconfigured by rerouting the light beams to different parts of the circuit. The key components to achieve that are photo-detector array and vertical-cavity surface-emitting lasers (VCSELs). The array of VCSELs could be connected directly to the circuit- transmitting nodes of one IP-core and the light beam is aligned to an array of photodetectors connected to the corresponding receiving nodes of another, as illustrated in Fig.2.



Fig.2. Re-routing light in optical-chip

Furthermore, the high interconnection density of paralleloptical links relieve the bottleneck in interconnect capacity that causes problems to system designers. However, the realisation of such a breed of integrated circuits requires test techniques that allow behaviour abnormality in both the electronic and the optical parts of a circuit to be detected.

The paper has been divided as follows: Section 2 introduces the proposed approach. Analytical modelling expressions are presented in Section 3. Concluding remarks are given in Section 4.

2 Testing Linking-with-Light SoC

There are well-established techniques for testing digital ICs [4][5], also accurate measures of testability for such circuits [5][6]. Techniques for testing analogue circuits were presented in [7][8], where it was shown and extensively applied that simulation, sensitivity, and other numerical and analytical methods can help in both analogue design and in analogue circuit testing. With the increasing complexity of circuits and systems the cost of all aspects of test activity is continually increasing. The provision of built-in-testing facilities has been to offer a cost effective alternative. Many IC designers have supported design for testability (DFT) in the form of scan insertion for digital and mixed-signal circuit designs [9][10]. Fig.3 shows a test access mechanism whereby a test can be applied and responses of an IP(s) can be collected and examined for abnormal functional behaviour.



Fig.3 Abstract representation of the IEEE 1149.4 standard for mixed-signal test [11]

Test techniques and methods - such as those mentioned above – assume metallic interconnects as a means of transferring signals between functional blocks of an integrated circuit. Hence, they are not capable of detecting abnormality that may occur over the on-chip optical interconnects. One way of approaching the problem of testing linking-withlight circuits and systems is by isolating the electronic section from the optical section, excluding the light source, of the chip. This can be achieved by introducing a slight modification to the interface of Fig.3 to allow for the outputs of light detectors to be monitored externally via optical I/O. With this modification, IPs and on-chip optical interconnect can be exercised independently or collectively. During the chip normal operation an IP-core can be a source or destination depending on the signal-flow. Considering an optical link between two IP-cores, any abnormality in the functional behaviour of the source-IP will influence the property of the transmitted light and thus an indication of functional abnormality. Based on light properties and transmission medium possible parameters that affect the performance of the onchip optical interconnect and hence the subsequent changes in transmission between IP-cores can be identified. If such information is stored in a database, deviation optical-interconnect in

performance and hence possible functional abnormality during the chip's normal operation can be continuously assessed.

3 Modelling of Parameters

An optical interconnect can be thought of as a layer of a semiconductor material (e.g. GaAs) is sandwiched between two layers of a semiconductor material that has a larger energy gaps (e.g. ALGa) and a smaller refractive index. The active region is within the sandwiched layer; the refractive index differences between this and the surrounding layers cause light to be confined to the active region due to the phenomenon of internal reflection. The propagation of light within the active layer can be measured as a function of the attenuated field in the surrounding layers, as shown in Fig.4 [12][13].



Fig.4 On-chip optical link between IPs.

Parameters such as absorption, temperature and refractive index influence the propagation of light in the active region. Fluctuations in one or more parameters may have a negative effect on the propagation of light, as they may result in a part of the electromagnetic energy is lost with the consequent decrease in the amplitude of the guided wave. This means that some of the light rays are lost and, hence, cannot reach the detector on the other end of the active region. The average transmitted power between the light source of one IP and the light-detector of another IP is decreased by a factor of $e^{-\alpha z}$ (∞ : attenuation constant)

$$P_r = P_t e^{-b\alpha z} \tag{1}$$

where $P_{r:}$ power at detector, P_{SL} : transmitted power, b: constant

The attenuated power is given by:

$$P_{Att}\{P_{det\,ector}, P_{int\,erconnect}, P_{source}\} = P_t - P_t e^{-b\alpha z}$$
(2)
or

$$P_{Att} = P_{Lz} = P_t (1 - e^{-b\alpha z}) \Big|_{z=0}$$
(3)

where P_{Lz} is the attenuated power ' P_{Att} ' at z = 0.

$$P_{Lz}^{-}(z) = P_{Lz} e^{-\kappa \alpha z} \Big|_{z \neq 0}$$
(4)

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where P_z^- is the power at z > 0. k: constant

If P_{Lz}^{-} represents the attenuated power in the region between z = 0 and z = L, then parameter fluctuations that influence the propagation of light into the weaveguide could be modelled as infinitesimal changes within the main transfer function which has P_{Lz} as input and P_{Lz}^{-} as an output, as shown in Fig.5.



Fig.5 Representation of Parameters

Considering varying effects caused by the surrounding layers, the rate of change in the field with time at z = 0 and z = x can be expressed as follows:

$$\Delta P_{Lz} = (\gamma_i \alpha_{n_{z=0}} - \gamma_i \alpha_{n_{z=L}}) P_{Lz} \Delta t$$
⁽⁵⁾

Using (5) and from Fig.4 and Fig.5, the relationship between P_{Lz} and P_{Lz}^- - in Laplace transform - is given by [14]:

$$\Re_{p_{Att}}^{p_{Lz}}(s) = s \Re_{p_{Att}}^{p_{Lz}}(0) + \frac{n_{\rho}}{n_{z,\rho}} \Re_{p_{Att}}^{p_{Lz}}(0)$$
(6)

where

$$\Re_{p_{Att}}^{p_{Lz}}(0) = \frac{1}{(s^2 + \frac{\gamma_{j_z}}{\gamma_i} \alpha_{n_z} s + \frac{n_{\rho}}{n_{z,\rho}} \frac{\gamma_{j_z}}{\gamma_i} \alpha_{n_z}) \quad (7)$$

with

$$s = -\frac{a}{2} \left(1 \pm \sqrt{1 - \frac{4b}{a}}\right) \bigg|_{a = \frac{\gamma_{j_z}}{\gamma_i} \alpha_{n_z}}; b = \frac{n_{\rho}}{n_{z,\rho}}}$$
(8)

where c: speed of light; $n_{z,\rho}^{\sim}$: parameter associated with the surrounding layers - it is a function of distance 'z' and ρ ; ρ : a parameter that is a function of time, e.g. temperature. γ_i and γ_j are parameters representing absorption processes at z =0 and z = L, respectively.

The value of 's' indicates a decaying function. However, the function exhibits an oscillatory behaviour if and only if (4b/a >> 1). An increase in (4b/a) triggers an increase in the frequency, but the envelope remains the same.

Equation (6) consists of two parts: the derivative of the original functional behaviour and a scaled version of the original behaviour. If the ratio between the $n_{z,\rho}$ and $n = f\{\gamma_i, \gamma_j\}$ is large the functional behaviour is a scaled version of the original behaviour. Otherwise, the derivative term contributes more to the response and has a greater effect.

For (i) a fixed value of 'L' or a fixed value of L and t. (where $t \in \rho$), and (ii) $n_{z,\rho} \cong n_{\rho}^{\sim}$:

$$\Re_{p_{Lz_i}}^{p_{\bar{L}z_i}} = \frac{s+1}{(s^2 + \frac{\gamma_{j_z}}{\gamma_i}\alpha_{n_z}s + \frac{\gamma_{j_z}}{\gamma_i}\alpha_{n_z})}$$
(9)

The functional behaviour of the attenuated field consists of the original functional behaviour plus its derivative. The value of s in the numerator is independent of changes in the refractive index. Hence, such changes have no effect on the amplitude of the function, as indicated by the sensitivity equations (10).



fluctuations.

Establishing a relationship between changes in the transmitted light and parameter fluctuations can aid in testing linking-with-light circuits and systems. The analytical expressions can estimate the expected responses which, independent of the circuit/system operation, can be compared against the measured light responses to identify inconsistencies in the system performance. A noticeable drift between the estimated light intensity and that measured at the detector is an indication of abnormality in the circuit's functionality. To ensure consistence performance of circuit/systems a test can be applied at regular intervals. From the

analytical expressions, it is possible to identify possible changes in the expected responses and their corresponding changes in light intensity. If this information is stored in a database, then it can be used to detect changes outside the norm.

4 Conclusion

Based on light properties and transmission medium possible parameters that affect the optical link and hence the subsequent changes in transmission between IP-cores can be identified. The work presented in this paper is based on the premise that linking-with-light circuits and systems - that have some of its parameters fluctuate outside predefined limits - exhibit abnormal behaviour.

Although optical connections are already available for connecting circuit boards within a computer, they are not yet commercially available for connecting subsystems within a chip optically. This could be contributed to many problems associated with the realization of hybrid (optical and electronic) IC circuits and systems. On such a problem is that GaAs, Indium Phosphide and other III-V compounds have a different lattice constant than silicon. However, it has been anticipated that advances in semiconductor technology within the next decade will enable manufacturers to meet the demand for the integration of optical and electronic elements on a single IC.

References:

- L. Coulibaly, H.J. Kadim. "Analytical Ramp Delay Model for Distributed On-Chip RLC Interconnects," 47th IEEE Inter. Midwest Symposium on Circuits and Systems, Japan, July 2004, pp I-457–I-460.
- [2] H.J. Kadim, "State-Space for Examination of Cross-Coupling Effects on Circuit Parameters", WSEAS Trans. on Circuits and Systems, Issue 8, Vol. 5, No.1, 2006, pp. 1147-1152, ISSN: 1109-2734.
- [3] A. Vittal, L. Chen, M. Sadowski, K. Wang, S. Yang, "Crosstalk in VLSI interconnect," IEEE Transactions on Computer-Aides design of Integrated Circuits and Systems, vol. 18, No. 12, 1999, pp. 1817-1824..
- [4] H.J. Kadim, G.E. Taylor, "Logic Value Assignment Contribution to Testability Analysis", IEEE International Symposium on Circuits and Systems, London, UK, 1994, pp. 195-198.

- [5] M. L. Bushhnell, V.D. Agrawal, "Essentials of Electronics Testing for Digital Memory & Mixed-signal VLSI Circuits", Kluwer Academic Pub., USA, 2000.
- [6] B. Chess, T. Larrabee, "Creating small fault dictionaries," IEEE Trans. Computer-Aided Design of integrated circuits and systems, vol. 18, No.3, 1999, pp. 346-356.
- H.J. Kadim, "Mathematical Modelling of Parameter Fluctuations with Applications to Fault Detection in Analogue VLSI Circuits", Radioelectronics and Informatics Journal, Issue No. 1, 2004, pp 103-108.
- [8] C. Chao, H. Lin, L. Milor, "Optimal Testing of VLSI Analogue Circuits", IEEE Trans. Computer-Aided Design, Vol.16, January 1997, pp. 58-77.
- [9] I. Gosh, N. Jha, S. Bhawmik, "A BIST Scheme for RTL Circuits based on Symbolic Testability Analysis", IEEE, Trans. on Computer-Aided Design of Integrated circuits & Sys., Vol. 19, No.1, January 2000, pp. 111-128.
- [10] N. A. Touba, E.J. McCluskey, "Bit-fixing in sequences for scan BIST," IEEE, Trans. on Computer-Aided Design of Integrated circuits & Sys., Vol. 20, No.4, 2000, pp. 545-555.

- [11] H.J. Kadim: "A Proposed Sensor-Configuration and Sensitivity Analysis of Parameters with Applications to Biosensors", in Stephen Wong and Chung-Sheng Li (Ed.): 'Life Science Data Mining, Science, Engineering and Biology Informatic, Vol. 2' (World Scientific Publishers December 2006), Chapter 16.
- [12] H.J. Kadim, "Predictive Analysis for Robust Operation with Applications to Autonomous Biosensors", NASA/ESA Int. Conf. on Adaptive Hardware and Systems, Edinburgh, UK, 5-8 August 2007, pp. 220-224.
- [13] H.J. Kadim, "Modelling of Anticipatory Behaviour for Self-Control and Adaptability with Potential Applications to Defence Systems", ECSIS Symposium on Bio-Inspired Learning and Intelligent Systems for Security, Edinburgh, UK, 2007, pp.91-94.
- [14] H.J. Kadim, "Analytical Modelling of Power Attenuation under Parameter Fluctuations with Applications to Self-Test and Repair", NASA/ESA Int. Conf. on Adaptive Hardware and Systems, Istanbul, June 2006, pp. 309-312.