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Current-Starved Pseudo-Floating Gate Amplifier

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Abstract: In this paper we present Current-Starved Pseudo-Floating Gate (CSPFG) inverters with capacitive feedback. The analog CSPFG inverter suppresses low frequencies due to the active, local feedback. This inverter can be used in designing circuits and amplifiers where high frequency signal processing is the main goal. One good area of use is in filter design where a narrow band pass or reject filter is to be designed. Typical applications are detection of high frequency components in sensor signals, i.e. airbag sensors. AC simulation of the inverter is presented to show that the circuit is suited for high performance filter design. Linearity simulations of the analog CSPFG inverters shows the good transient properties suited for amplifier design.

Key–Words: Analog, CMOS, Floating gate, Inverter, Amplifier, Filter.

1 Introduction

Transistor were discovered in the search for a semiconductor based amplifying component in late 1940's. Since then there has been a large improvement in the electrical and physical properties of the transistors enabling design of more complex circuits and amplifiers. OP-Amps have been the dominating amplifier circuit due to their flexibility and simplicity. Many techniques and circuits have been presented to improve the OP-Amps and amplifiers, these improvements include power consumption, accuracy, noise, bandwidth [1, 2] and speed. Examples are Switch cap [3], Auto-Zero Amplifiers(AZA) [4], chopper-stabilized amplifiers [5] and in some extend neuromorphic electronics [6]. These systems often use a digital clock as a tool to achieve these improvements. Inverters are also one of the simplest amplifiers available, widely used in digital circuits and systems to logically invertert signals. One drawback of using inverters as amplifiers is that in CMOS case for it to work both PMOS and NMOS must in saturation region. This is a small region where the both transistors are turned on resulting in a class A Amplifier. Class A amplifiers dissipate power constantly even if there is no input signal at all, resulting in large waste of power when used as large power amplifiers. On the other hand this results in reduction of thermal variation and eliminates crossover distortion, which makes the circuit linear and faster, suited for small power applications. In this paper we present a new type of amplifier based on Inverters, or more accurate Pseudo-Floating Gate (PFG)[7] inverter [8]. These amplifiers are purely analog, high speed and power conservative. One advantage compared to operational amplifiers is that the bandwidth of the active component (amplifier) can be changed without adding external components or changing the design of the circuit, well suited for filter design. The first analog circuit based on CSPFG was a band pass amplifier presented by Y. Berg et al [9, 10]. One important property of that amplifier was that the pass area could vary simply by changing a few bias voltages.

This paper is organized into following sections: section one was the introduction. Section 2 presents the Pseudo Floating Gate (PFG). Detailed simulation results of a analog CSPFG inverter is shown in section 2. We discus the transient properties, the gain and linearity of the analog CSPFG inverter when used as amplifier. AC simulations of the analog CSPFG inverter is also shown and discussed. In section 2.2 a cascade connection of the CSPFG inverters is presented. Section 3 presents 3 circuits designed using CSPFG inverter along with their transient and AC simulations. In section 3.1 a differential amplifier, section 3.2 a variable delay-line and in section 3.3 a differentiator based on CSPFG inverters is presented. Section 4 is devoted to filters. In this section a band pass filter and a band stop filter along with their AC and transient simulations are presented. Section 5 concludes the work presented in this paper. The simulations presented in this paper are being done in the Cadence environment with 90 nm CMOS transistor models from STM with a VDD equal 1.2 volts and threshold voltage of 0.25 volts.

2 Pseudo Floating-Gate circuits

Floating-gate (FG) circuit design [11, 12, 13] offers various advantages. Due to the ability to shift the transistor threshold voltages seen from the capacitively coupled input terminal, the analog designer will be able to design low power circuits operating at low supply voltages [14]. Floating-gates need to be initialized or programmed and there are 2 main approaches: Non-Volatile Floating-Gate (NFG)[15, 16] and Semi-Floating-Gate (SFG) [17, 18]. Various programming approaches exist in the NFG, like utilization of UV-conductances [15], Fowler Nordheim Tunneling and Hot Electron Injection [12]. These techniques have their drawbacks. The UV-conductance approach is difficult to re-program and the tunneling injection technique needs high voltages. On big disadvantage of NFG technique is that charges can be trapped in the floating gate during processing and can result in change of threshold voltage and inaccuracy in the circuit. Semi-Floating-Gate uses a clock for the initialization, thus not suited for pure analog circuit design, but suited for Multi-Valued-Logic digital circuit design. Pseudo-Floating-Gate (PFG) borrows ideas from both NFG and SFG without being purely floating. Large valued resistors weakly control the offset voltage at the floating gate node thus avoiding problems like trapped charges and the need for programming. Since the floating gates are not entirely floating, these are denoted Pseudo Floating-Gate[5].

2.1 Analog CSPFG inverter

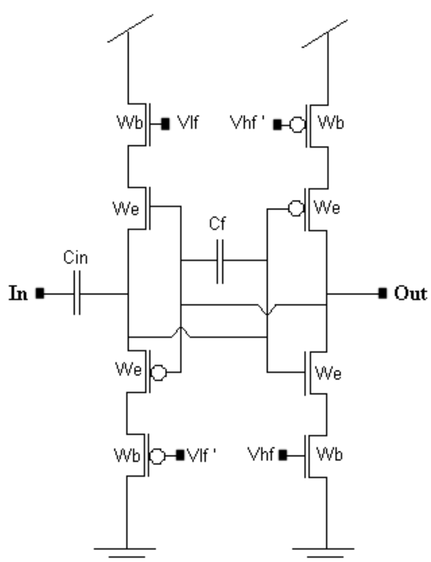

Figure 1: *Schematic of the analog CSPFG inverter.*

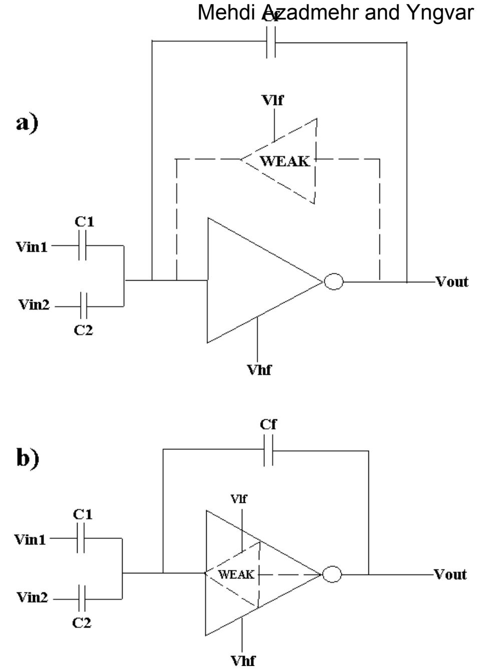

Figure 2: *Symbol of the analog CSPFG inverter, a) is the old symbol used in earlier publications, b) is the proposed new symbol that is simpler and more compact.*

The schematic of an analog CSPFG inverter is shown in figure 1 and the symbol in figure 2. The circuit is a current-starved inverter with a weak positive feedback. The positive feedback circuitry is basically a current-starved inverter where the PMOS transistors are connected between the output and GND and the NMOS transistors between output and VDD, the opposite of the inverter. This positive feedback has 2 important functions in the circuit, it sets the operational point (DC level) of the circuit and it decides the lower cut-off frequency. Bias voltages on Vhf and Vlf limit the current flowing through the inverter and the feedback circuitry respectively. In the symbol the biases Vlf' and Vhf' are excluded since they are biased $VDD - Vlf$ and $VDD - Vhf$ respectively in all circuits designed and presented in this paper. The input capacitance, Cin, block DC signals from the other circuitry connected to the inputs and make the circuit floating. Multiple input circuits can be achieved using parallel input capacitances as shown in figure 2. In this case C1 and C2 can also be used for weighting the input [19] signals compared to each other simply by choosing the right values. The closed loop gain of the circuit can be adjusted by changing the value of the feedback capacitor, Cf compared to the input capacitor Cin and is given by:

$$A_{CSPFG} \approx -\frac{\Sigma C_{in}}{C_f} \tag{1}$$

Assuming the inverter is ideal with a large gain and Vhf larger than vdd/2.

2.1.1 Transient response

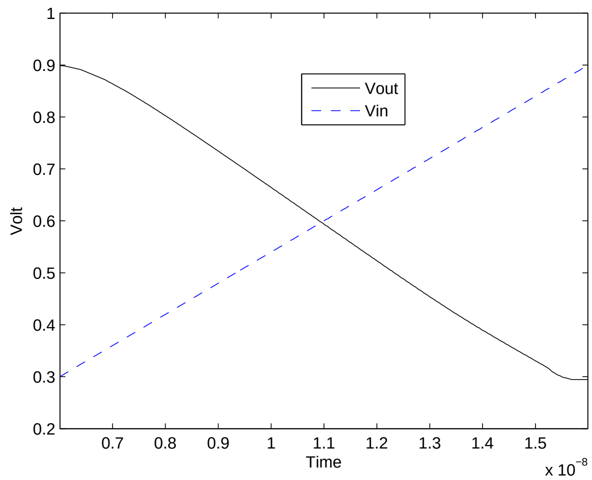

Figure 3: *Transient response of the analog CSPFG inverter.*

Figure 3 shows the transient response of the 2 input analog CSPFG inverter. In this simulation the voltage on Vhf is set to 0.42V and Vlf to 0.40V. The inputs $Vin1$ and $Vin2$ are shorted and swept from 0.3 to 0.9 volts in a time period of $10ns(50MHz)$. The solid line represents the circuit response and the dashed line the input stimuli. The time delay of the circuit is not constant because of its dependent on the bias voltage, Vhf. The time delay is neglected because the aim of this simulation is the voltage response of the circuit, this is discussed more in section 2.2. From the figure we see that the circuit has a linear response in the range 0.3 to 0.9 volts and flats out for voltages above and below this region. The operating voltage (dc level) of the circuit is VDD/2, where the 2 lines cross.

Figure 4 shows the gain of the amplifier. This graph is the derivate of the output voltage divided by the derivate of the input voltage. The negative sign is due to the circuits inverting property. We can see that the Gain is increasing until the input is ca 0.4 volts. Then the circuit is linear until 0.8 volts where the Gain is decreased again. Between 0.5 volts and 0.7 volts we

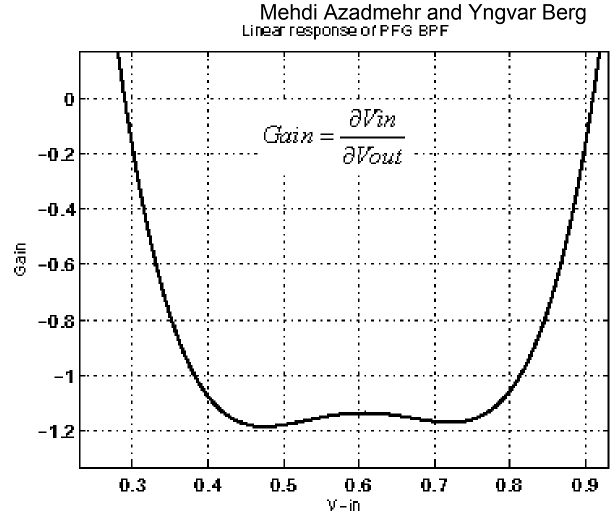

Figure 4: *The gain of the analog CSPFG inverter.*

have an almost flat area indicating a linear gain of approximately 1.2. The results indicates a symmetrical behavior around VDD/2.

2.1.2 AC response

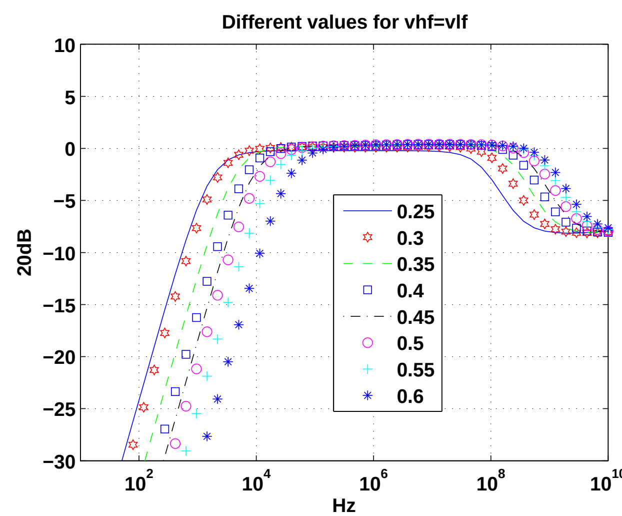

Figure 5: *The AC response of the analog CSPFG inverter for different values of Vhf, assuming Vlf = Vhf.*

Figure 5 Shows the AC response of the analog CSPFG amplifier when the bias voltages, Vhf and Vlf are varied from 0.25 to 0.6 volts simultaneous. We can see that the forwarding inverter suppresses high frequencies depending on the value of Vhf, but it can operate on frequencies as high as 800 MHz. The positive feedback suppresses low frequencies based on the voltage on Vlf. The lowest frequencies that can pass are as low as 3 KHz.

If the capacitors Cin and Cf are equal, the transfer function of the circuit can be obtained by:

$$\frac{V_{out}}{\frac{1}{SC_l}} = -gm(V_{in} + V_{out})$$

$$\frac{SC_l V_{out}}{g_m} = -V_{in} - V_{out}$$

$$\tau = \frac{C_l}{g_m} => S\tau V_{out} = -V_{in} - V_{out}$$

$$H(S)_{lowpass} = \frac{V_{out}}{V_{in}} = \frac{-1}{1+\tau S} \quad (2)$$

Equation 2 shows that the inverter has a 1 order low pass filter behavior. We can estimate the cut-off frequencies by using simple transistor models and assuming that the starving transistor operates in the linear region:

$$f_{max} \approx \frac{\beta_{Wb} V_{hf_{effective}}}{2C_l VDD} \quad (3)$$

where $V_{hf_{effective}} = Vhf - Vt$. A reasonable value for the forward limiting current is 10uA yielding a max frequency of approximately 800MHz for Cl = 5fF and VDD = 1.2. If the current limiting transistors operate in weak inversion the current may be approximated by:

$$f_{max} \approx \frac{2n\beta_{We} U_T^2 e^{\frac{V_{hf}}{nUT}}}{2C_l VDD} \quad (4)$$

2.2 Cascade of CSPFG inverters

A cascade coupling of analog CSPFG inverters is shown in figure 6. The inverters are connected to each other through capacitors C. The feedback capacitors Cf_1 to Cfn are given a value so that the gain of each inverter i equal to 1 and thus a total gain of 1. The Vhf_1 to Vhf_n are biased with the same voltage and Vlf_1 to Vlf_n biased equally.

Figure 7 shows the transient response of 9 CSPFG inverters connected in series. The results are the response of the 1. 3. 5. 7. 9th inverter. The input stimulus is also plotted and has the inverse value of the responses. One important feature is the delay caused by the inverters in the cascade connection. From the figure we see that each inverter is adding a time delay to the signal, this is discussed in details in section 5. Another feature that can be seen is that the sharp edges of the input signal are becoming rounder for each output toward the 9th inverter. This is duo to the gain of each inverter in the series connection. The increase of gain can also be observed as a sharpening of the transition from maximum value $900mV$ to minimum $300mV$.

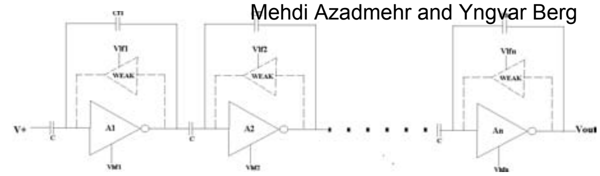

Figure 6: *Analog CSPFG amplifier with n inverters connected in series.*

Figure 8 shows the gain of 9 CSPFG inverters connected in series. The results are the gain of the 1. 3. 5. 7. 9th inverter. The negative sign is due to the inverting result since the odd number inverters are measured. We can see that as the amount of series inverters increases, linearity of the circuit decreases, but the gain increases.

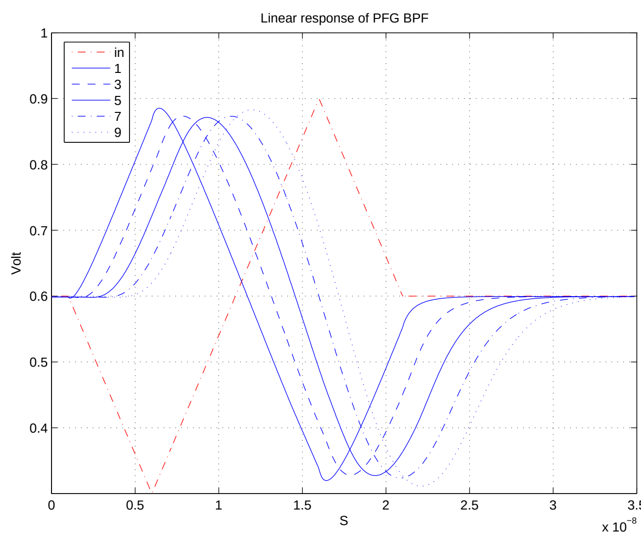

Figure 7: *Transient response of the 1,3,5,7,9th inverter in the analog CSPFG amplifier where 9 inverters are connected in series. The red, dashed line is the input stimuli.*

Figure 9 shows the AC response of 9 CSPFG inverters connected in series. The results are the response of the 1. 3. 5. 7. 9th inverter. The figure shows that for each step in this series of inverters we achieve a sharper transition band. This sharpness is valid both for the lower and the higher transition band. We see that for higher frequencies, around $10^{10}Hz$ we have a increase in the signal. This is

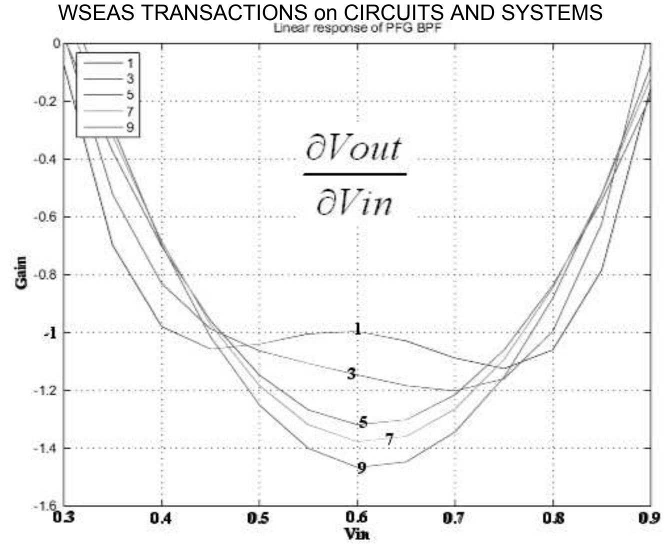

Figure 8: *The gain of the 1,3,5,7,9th analog CSPFG amplifier inverters connected in series, the legend box in the figure is the number of inverters.*

caused by the capacitive connection that connects the input to the output for higher frequencies. The increase of gain and sharpening of the transition band presented in this section can be used to improve CSPFG filters.

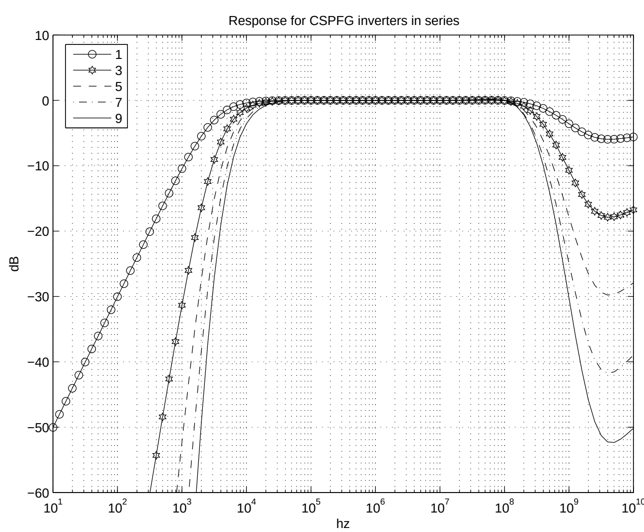

Figure 9: *AC response of the 1,3,5,7,9th inverter in the analog CSPFG amplifier where 9 inverters are connected in series.*

3 CSPFG circuits

In this section we present some circuit examples implemented using CSPFG inverters. The main focus will be the use of CSPFG inverters as amplifier. CSPFG filters are presented separately in a section 4, due to the extend of this topic.

3.1 Differential amplifier

The differential CSPFG amplifier is shown in figure 10. The inverter A1 inverts the signal from V- input and is summed in point V1 with V+. The results is attenuation of similar values at the inputs and amplification for others. This behavior is shown in figure 11.

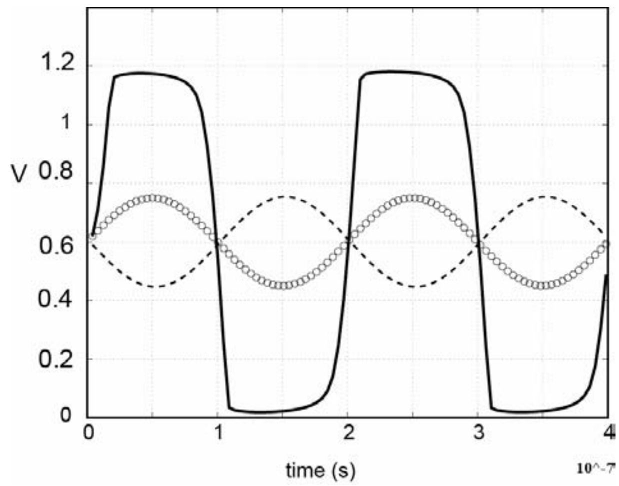

Figure 11: *Response of the differential CSPFG amplifier.*

Figure 12 shows the output current of the amplifier for different values Vhf. The current exhibit a tanh shape for large input values and a sinh shape for small inputs. In this figure we see the effect of the 2 input analog CSPFG inverter on the Filter compared to the filter published in [5] as increasing gain. This can also be observed in the transconductance of the CSPFG amplifier shown in Figure 13. The transconductance has increased from $2 \times 10^{-7} gm$ to $5 \times 10^{-5} gm$ for $Vhf1 = 0.6V$. The combination of sinh and tanh shaped output current is evident, and the linear region is determined by $Vhf1$ and $Vhf3$. We can observe that the linear range for $Vhf1 = 0.6V$ and $Vhf3 = 0.58V$, assuming 3% distortion, is close to $160mV (80mV)$.

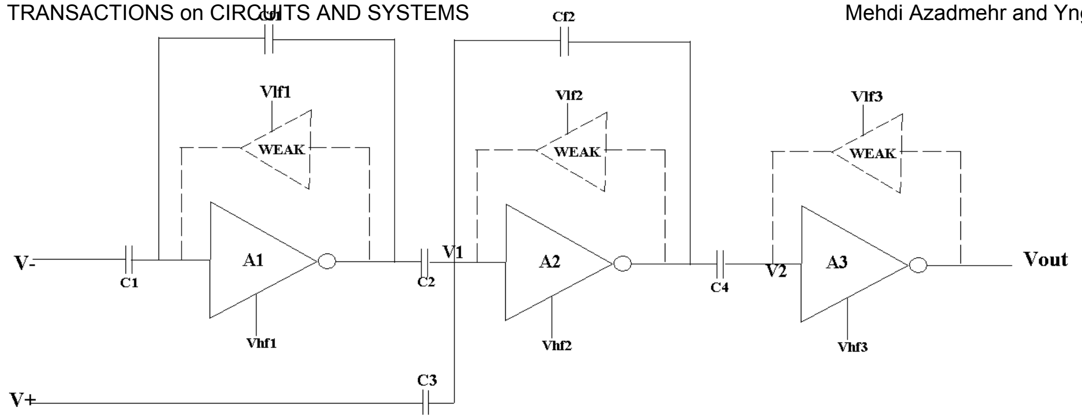

Figure 10: *Differential CSPFG amplifier.*

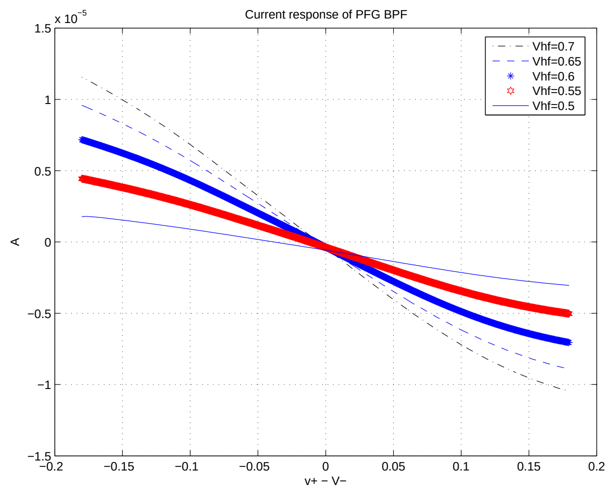

Figure 12: *The output current of the CSPFG amplifier for different values on Vhf1, assuming that Vhf3=Vhf1+20mV*

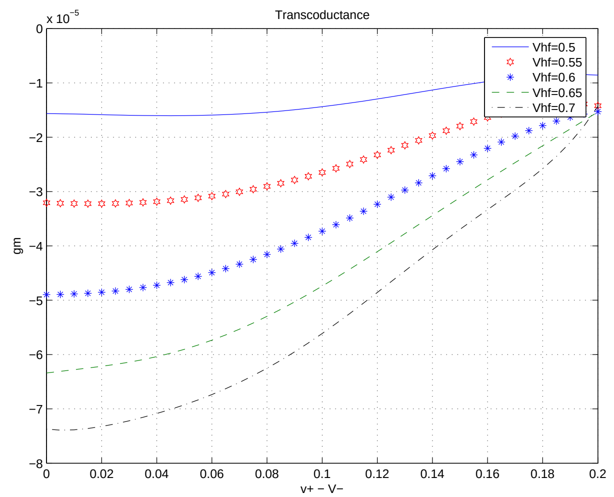

Figure 13: *The Transconductance of the CSPFG amplifier for different values of Vhf1.assuming that Vhf3=Vhf1+20mV*

3.2 Analog delay-line

Current-Starved inverters are being used widely as delay-lines for use in Delay-Locked-Loop (DLL) [20, 21]. Although the current-Starved inverter is an analog circuit, it is being used as a digital circuit that operated for the only values of vdd(1) and GND(0). Current-Starved PFG inverters enable the use of these circuits as delay-line in analog circuits due to the adjustable gain and a DC operating point. Figure 14 shows the delay of 4 analog CSPFG inverters connected in series for different values for Vhf. In this simulation the input signal is a sinus wave with a frequency of 100MHz and a amplitude of 300mV presented as blue circles. The output signals are also sine shaped with the same frequency, but a increasing delay as the Vhf decreases. Table 1 lists the time delay and the phase shift for each Vhf value.

Vhf	0.4	0.45	0.5	0.55	0.6
Time delay	0.61 nS	0.35 nS	0.22 nS	0.17 nS	0.13nS
Phase shift	219^o	126^o	79^o	61^o	46^o

Table 1: Delay response in s and in degree for Vhf values from 0.4 to 0.6

3.3 Differentiator

Figure 15 shows a CSPFG Differentiator. The differentiator is made of the forwarding inverter A1 and a feedback circuitry consisting analog inverters A2 and A3. This circuit produces an output voltage that is