

Current-Starved Pseudo-Floating Gate Amplifier

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Abstract: In this paper we present Current-Starved Pseudo-Floating Gate (CSPFG) inverters with capacitive feedback. The analog CSPFG inverter suppresses low frequencies due to the active, local feedback. This inverter can be used in designing circuits and amplifiers where high frequency signal processing is the main goal. One good area of use is in filter design where a narrow band pass or reject filter is to be designed. Typical applications are detection of high frequency components in sensor signals, i.e. airbag sensors. AC simulation of the inverter is presented to show that the circuit is suited for high performance filter design. Linearity simulations of the analog CSPFG inverters shows the good transient properties suited for amplifier design.

Key-Words: Analog, CMOS, Floating gate, Inverter, Amplifier, Filter.

1 Introduction

Transistor were discovered in the search for a semiconductor based amplifying component in late 1940's. Since then there has been a large improvement in the electrical and physical properties of the transistors enabling design of more complex circuits and amplifiers. OP-Amps have been the dominating amplifier circuit due to their flexibility and simplicity. Many techniques and circuits have been presented to improve the OP-Amps and amplifiers, these improvements include power consumption, accuracy, noise, bandwidth [1, 2] and speed. Examples are Switch cap [3], Auto-Zero Amplifiers(AZA) [4], chopper-stabilized amplifiers [5] and in some extend neuromorphic electronics [6]. These systems often use a digital clock as a tool to achieve these improvements. Inverters are also one of the simplest amplifiers available, widely used in digital circuits and systems to logically invert signals. One drawback of using inverters as amplifiers is that in CMOS case for it to work both PMOS and NMOS must in saturation region. This is a small region where the both transistors are turned on resulting in a class A Amplifier. Class A amplifiers dissipate power constantly even if there is no input signal at all, resulting in large waste of power when used as large power amplifiers. On the other hand this results in reduction of thermal variation and eliminates crossover distortion, which makes the circuit linear and faster, suited for small power applications. In this paper we present a new type of amplifier based on Inverters, or more accurate Pseudo-Floating Gate (PFG)[7] inverter [8].

These amplifiers are purely analog, high speed and power conservative. One advantage compared to operational amplifiers is that the bandwidth of the active component (amplifier) can be changed without adding external components or changing the design of the circuit, well suited for filter design. The first analog circuit based on CSPFG was a band pass amplifier presented by Y. Berg et al [9, 10]. One important property of that amplifier was that the pass area could vary simply by changing a few bias voltages.

This paper is organized into following sections: section one was the introduction. Section 2 presents the Pseudo Floating Gate (PFG). Detailed simulation results of a analog CSPFG inverter is shown in section 2. We discuss the transient properties, the gain and linearity of the analog CSPFG inverter when used as amplifier. AC simulations of the analog CSPFG inverter is also shown and discussed. In section 2.2 a cascade connection of the CSPFG inverters is presented. Section 3 presents 3 circuits designed using CSPFG inverter along with their transient and AC simulations. In section 3.1 a differential amplifier, section 3.2 a variable delay-line and in section 3.3 a differentiator based on CSPFG inverters is presented. Section 4 is devoted to filters. In this section a band pass filter and a band stop filter along with their AC and transient simulations are presented. Section 5 concludes the work presented in this paper. The simulations presented in this paper are being done in the Cadence environment with 90 nm CMOS transistor models from STM with a VDD equal 1.2 volts and threshold voltage of 0.25 volts.

Floating-gate (FG) circuit design [11, 12, 13] offers various advantages. Due to the ability to shift the transistor threshold voltages seen from the capacitively coupled input terminal, the analog designer will be able to design low power circuits operating at low supply voltages [14]. Floating-gates need to be initialized or programmed and there are 2 main approaches: Non-Volatile Floating-Gate (NFG)[15, 16] and Semi-Floating-Gate (SFG) [17, 18]. Various programming approaches exist in the NFG, like utilization of UV-conductances [15], Fowler Nordheim Tunneling and Hot Electron Injection [12]. These techniques have their drawbacks. The UV-conductance approach is difficult to re-program and the tunneling injection technique needs high voltages. On big disadvantage of NFG technique is that charges can be trapped in the floating gate during processing and can result in change of threshold voltage and inaccuracy in the circuit. Semi-Floating-Gate uses a clock for the initialization, thus not suited for pure analog circuit design, but suited for Multi-Valued-Logic digital circuit design. Pseudo-Floating-Gate (PFG) borrows ideas from both NFG and SFG without being purely floating. Large valued resistors weakly control the offset voltage at the floating gate thus avoiding problems like trapped charges and the need for programming. Since the floating gates are not entirely floating, these are denoted Pseudo Floating-Gate[5].

2.1 Analog CSPFG inverter

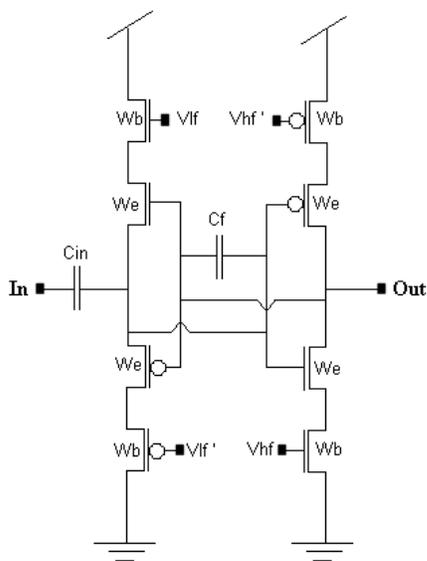


Figure 1: Schematic of the analog CSPFG inverter.

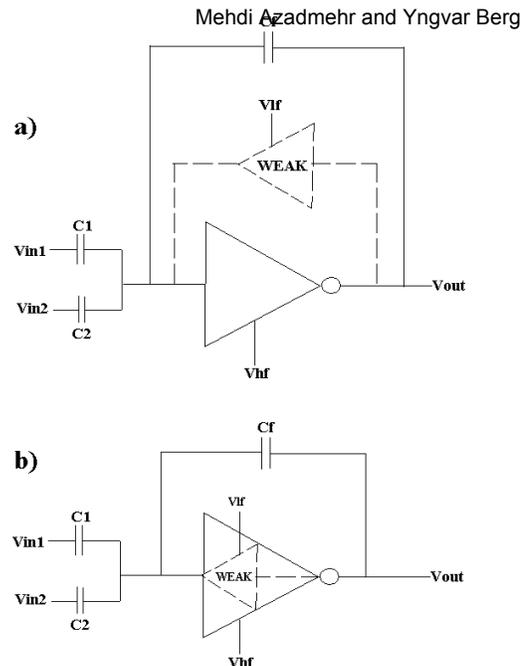


Figure 2: Symbol of the analog CSPFG inverter, a) is the old symbol used in earlier publications, b) is the proposed new symbol that is simpler and more compact.

The schematic of an analog CSPFG inverter is shown in figure 1 and the symbol in figure 2. The circuit is a current-starved inverter with a weak positive feedback. The positive feedback circuitry is basically a current-starved inverter where the PMOS transistors are connected between the output and GND and the NMOS transistors between output and VDD, the opposite of the inverter. This positive feedback has 2 important functions in the circuit, it sets the operational point (DC level) of the circuit and it decides the lower cut-off frequency. Bias voltages on Vhf and Vlf limit the current flowing through the inverter and the feedback circuitry respectively. In the symbol the biases Vlf' and Vhf' are excluded since they are biased $VDD - Vlf$ and $VDD - Vhf$ respectively in all circuits designed and presented in this paper. The input capacitance, Cin , block DC signals from the other circuitry connected to the inputs and make the circuit floating. Multiple input circuits can be achieved using parallel input capacitances as shown in figure 2. In this case C1 and C2 can also be used for weighting the input [19] signals compared to each other simply by choosing the right values. The closed loop gain of the circuit can be adjusted by changing the value of the feedback capacitor, Cf compared to the input capacitor Cin and is given by:

$$A_{CSPFG} \approx -\frac{\Sigma C_{in}}{C_f} \tag{1}$$

Assuming the inverter is ideal with a large gain and V_{hf} larger than $v_{dd}/2$.

2.1.1 Transient response

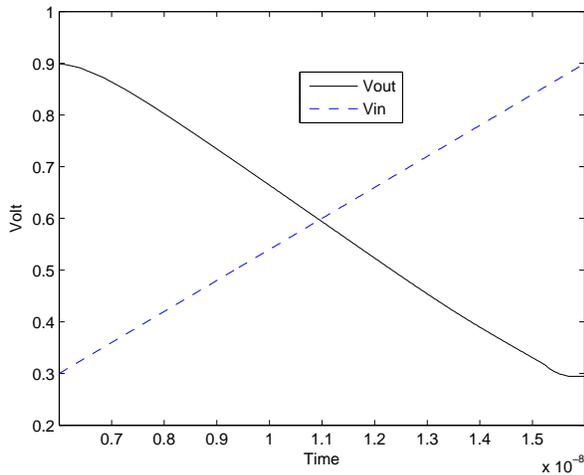


Figure 3: *Transient response of the analog CSPFG inverter.*

Figure 3 shows the transient response of the 2 input analog CSPFG inverter. In this simulation the voltage on V_{hf} is set to 0.42V and V_{lf} to 0.40V. The inputs V_{in1} and V_{in2} are shorted and swept from 0.3 to 0.9 volts in a time period of 10ns(50MHz). The solid line represents the circuit response and the dashed line the input stimuli. The time delay of the circuit is not constant because of its dependent on the bias voltage, V_{hf} . The time delay is neglected because the aim of this simulation is the voltage response of the circuit, this is discussed more in section 2.2. From the figure we see that the circuit has a linear response in the range 0.3 to 0.9 volts and flats out for voltages above and below this region. The operating voltage (dc level) of the circuit is $V_{DD}/2$, where the 2 lines cross.

Figure 4 shows the gain of the amplifier. This graph is the derivate of the output voltage divided by the derivate of the input voltage. The negative sign is due to the circuits inverting property. We can see that the Gain is increasing until the input is ca 0.4 volts. Then the circuit is linear until 0.8 volts where the Gain is decreased again. Between 0.5 volts and 0.7 volts we

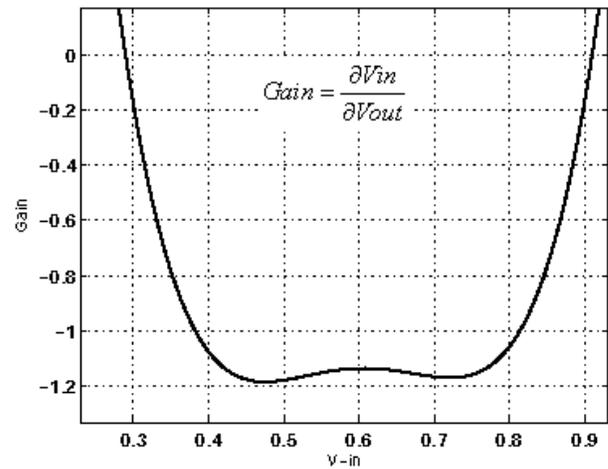


Figure 4: *The gain of the analog CSPFG inverter.*

have an almost flat area indicating a linear gain of approximately 1.2. The results indicates a symmetrical behavior around $V_{DD}/2$.

2.1.2 AC response

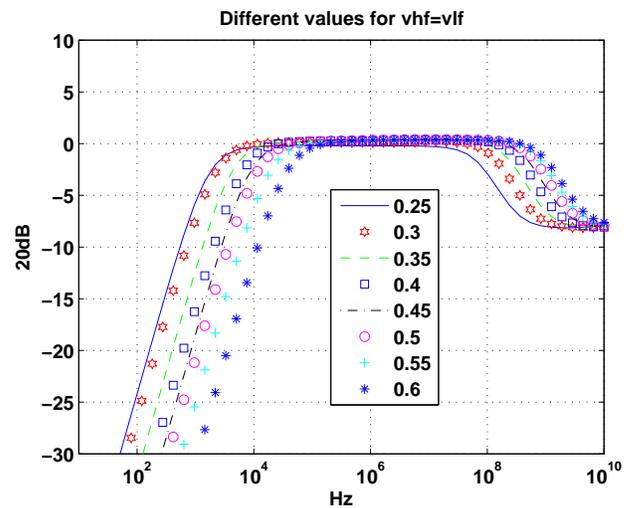


Figure 5: *The AC response of the analog CSPFG inverter for different values of V_{hf} , assuming $V_{lf} = V_{hf}$.*

Figure 5 Shows the AC response of the analog CSPFG amplifier when the bias voltages, V_{hf} and V_{lf} are varied from 0.25 to 0.6 volts simultaneous. We can see that the forwarding inverter suppresses high frequencies depending on the value of V_{hf} , but it can operate on frequencies as high as 800 MHz. The positive feedback suppresses low frequencies based on the

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voltage on V_{lf} . The lowest frequencies that can pass
are as low as 3 KHz.

If the capacitors C_{in} and C_f are equal, the transfer
function of the circuit can be obtained by:

$$\begin{aligned} \frac{V_{out}}{\frac{1}{sC_l}} &= -gm(V_{in} + V_{out}) \\ \frac{sC_l V_{out}}{gm} &= -V_{in} - V_{out} \\ \tau &= \frac{C_l}{gm} \Rightarrow s\tau V_{out} = -V_{in} - V_{out} \\ H(S)_{lowpass} &= \frac{V_{out}}{V_{in}} = \frac{-1}{1 + \tau S} \end{aligned} \quad (2)$$

Equation 2 shows that the inverter has a 1 order
low pass filter behavior. We can estimate the cut-off
frequencies by using simple transistor models and as-
suming that the starving transistor operates in the lin-
ear region:

$$f_{max} \approx \frac{\beta_{Wb} V_{hfeffective}}{2C_l V_{DD}} \quad (3)$$

where $V_{hfeffective} = V_{hf} - V_t$. A reasonable
value for the forward limiting current is 10uA yield-
ing a max frequency of approximately 800MHz for
 $C_l = 5fF$ and $V_{DD} = 1.2$. If the current limiting tran-
sistors operate in weak inversion the current may be
approximated by:

$$f_{max} \approx \frac{2n\beta_{We} U_T^2 e^{\frac{V_{hf}}{nU_T}}}{2C_l V_{DD}} \quad (4)$$

2.2 Cascade of CSPFG inverters

A cascade coupling of analog CSPFG inverters is
shown in figure 6. The inverters are connected to each
other through capacitors C . The feedback capacitors
 C_{f1} to C_{fn} are given a value so that the gain of each
inverter i equal to 1 and thus a total gain of 1. The
 V_{hf1} to V_{hfn} are biased with the same voltage and
 V_{lf1} to V_{lfn} biased equally.

Figure 7 shows the transient response of 9 CSPFG
inverters connected in series. The results are the re-
sponse of the 1. 3. 5. 7. 9th inverter. The input stimu-
lus is also plotted and has the inverse value of the re-
sponses. One important feature is the delay caused by
the inverters in the cascade connection. From the fig-
ure we see that each inverter is adding a time delay to
the signal, this is discussed in details in section 5. An-
other feature that can be seen is that the sharp edges of

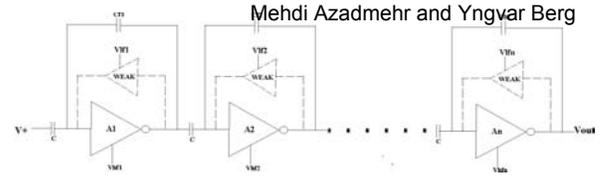


Figure 6: Analog CSPFG amplifier with n inverters
connected in series.

the input signal are becoming rounder for each output
toward the 9th inverter. This is due to the gain of each
inverter in the series connection. The increase of gain
can also be observed as a sharpening of the transition
from maximum value $900mV$ to minimum $300mV$.

Figure 8 shows the gain of 9 CSPFG inverters
connected in series. The results are the gain of the
1. 3. 5. 7. 9th inverter. The negative sign is due to
the inverting result since the odd number inverters are
measured. We can see that as the amount of series in-
verters increases, linearity of the circuit decreases, but
the gain increases.

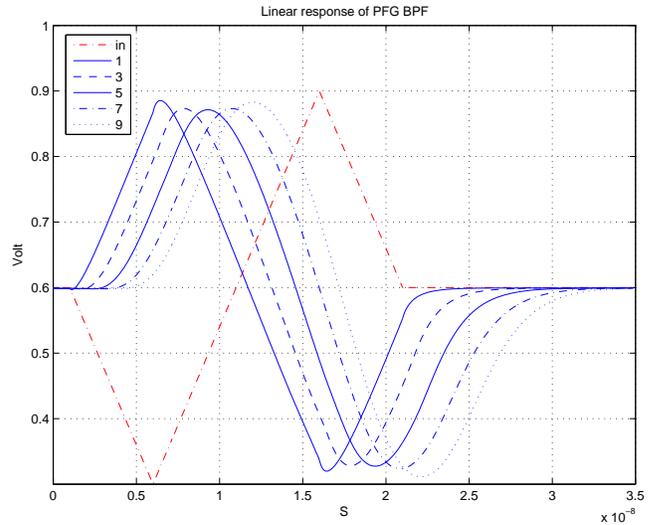


Figure 7: Transient response of the 1,3,5,7,9th in-
verter in the analog CSPFG amplifier where 9 invert-
ers are connected in series. The red, dashed line is the
input stimuli.

Figure 9 shows the AC response of 9 CSPFG
inverters connected in series. The results are the re-
sponse of the 1. 3. 5. 7. 9th inverter. The figure
shows that for each step in this series of inverters
we achieve a sharper transition band. This sharpness
is valid both for the lower and the higher transition
band. We see that for higher frequencies, around
 $10^{10}Hz$ we have a increase in the signal. This is

3 CSPFG circuits

In this section we present some circuit examples implemented using CSPFG inverters. The main focus will be the use of CSPFG inverters as amplifier. CSPFG filters are presented separately in a section 4, due to the extend of this topic.

3.1 Differential amplifier

The differential CSPFG amplifier is shown in figure 10. The inverter A1 inverts the signal from V- input and is summed in point V1 with V+. The results is attenuation of similar values at the inputs and amplification for others. This behavior is shown in figure 11.

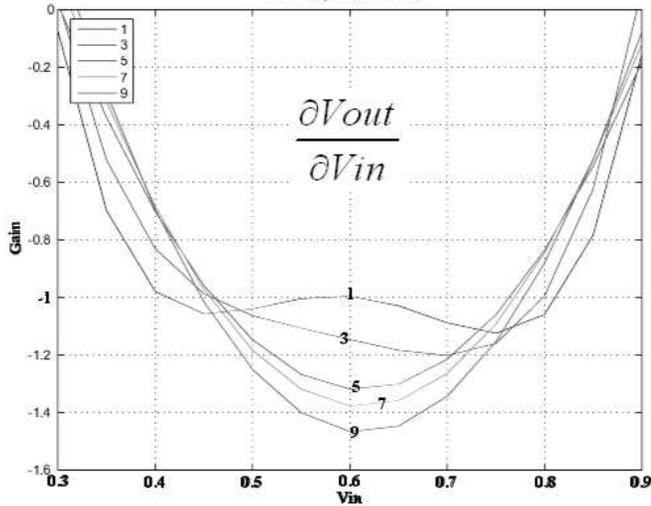


Figure 8: The gain of the 1,3,5,7,9th analog CSPFG amplifier inverters connected in series, the legend box in the figure is the number of inverters.

caused by the capacitive connection that connects the input to the output for higher frequencies. The increase of gain and sharpening of the transition band presented in this section can be used to improve CSPFG filters.

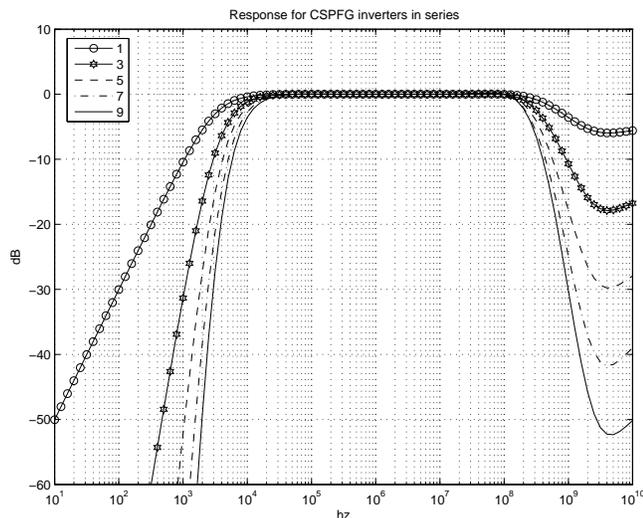


Figure 9: AC response of the 1,3,5,7,9th inverter in the analog CSPFG amplifier where 9 inverters are connected in series.

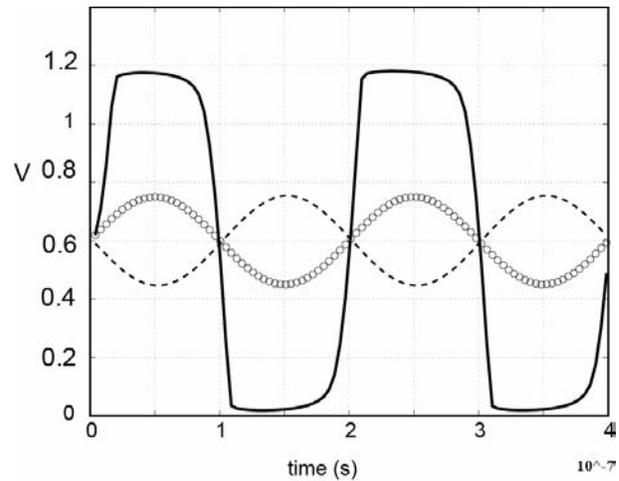


Figure 11: Response of the differential CSPFG amplifier.

Figure 12 shows the output current of the amplifier for different values V_{hf} . The current exhibit a tanh shape for large input values and a sinh shape for small inputs. In this figure we see the effect of the 2 input analog CSPFG inverter on the Filter compared to the filter published in [5] as increasing gain. This can also be observed in the transconductance of the CSPFG amplifier shown in Figure 13. The transconductance has increased from $2 \times 10^{-7} gm$ to $5 \times 10^{-5} gm$ for $V_{hf1} = 0.6V$. The combination of sinh and tanh shaped output current is evident, and the linear region is determined by V_{hf1} and V_{hf3} . We can observe that the linear range for $V_{hf1} = 0.6V$ and $V_{hf3} = 0.58V$, assuming 3% distortion, is close to $160mV$ ($80mV$).

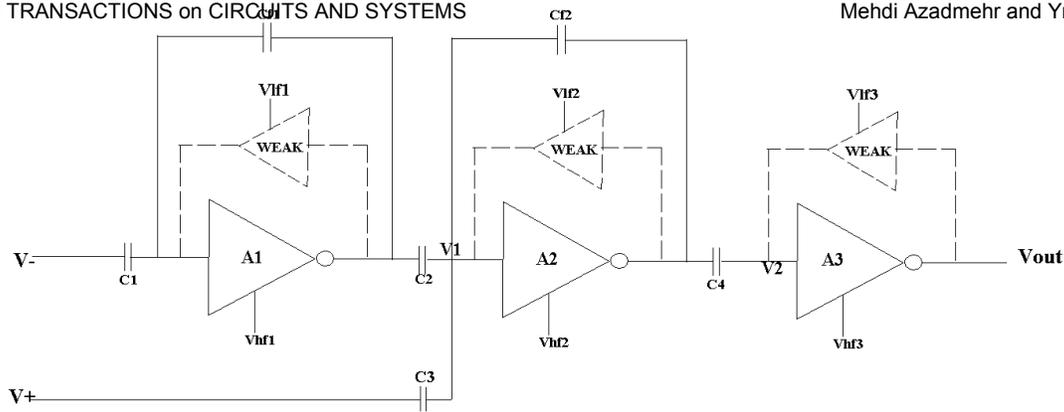


Figure 10: Differential CSPFG amplifier.

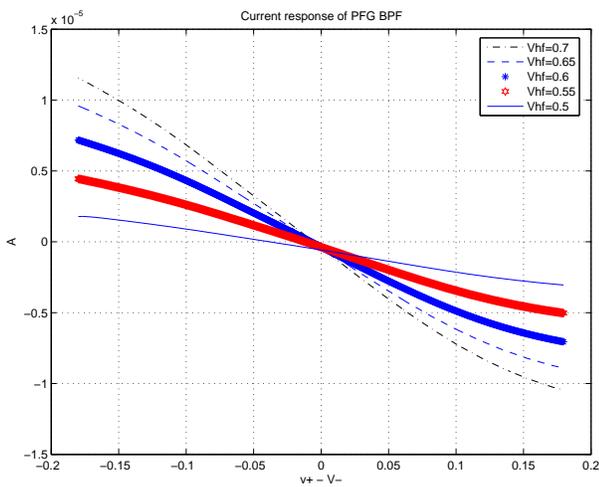


Figure 12: The output current of the CSPFG amplifier for different values on V_{hf1} , assuming that $V_{hf3} = V_{hf1} + 20mV$

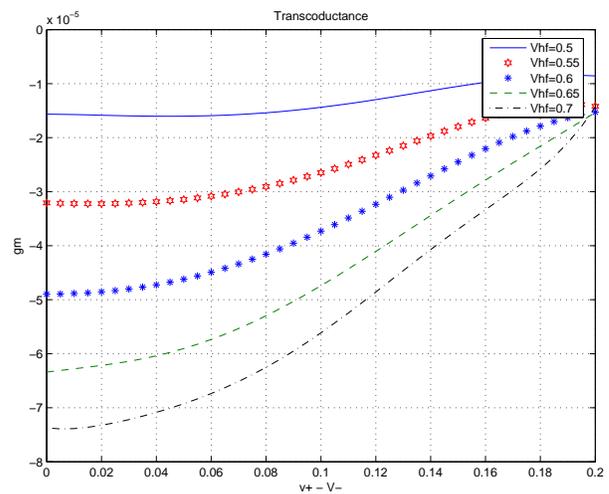


Figure 13: The Transconductance of the CSPFG amplifier for different values of V_{hf1} . assuming that $V_{hf3} = V_{hf1} + 20mV$

3.2 Analog delay-line

Current-Starved inverters are being used widely as delay-lines for use in Delay-Locked-Loop (DLL) [20, 21]. Although the current-Starved inverter is an analog circuit, it is being used as a digital circuit that operated for the only values of vdd(1) and GND(0). Current-Starved PFG inverters enable the use of these circuits as delay-line in analog circuits due to the adjustable gain and a DC operating point. Figure 14 shows the delay of 4 analog CSPFG inverters connected in series for different values for V_{hf} . In this simulation the input signal is a sinus wave with a frequency of 100MHz and a amplitude of 300mV presented as blue circles. The output signals are also sine shaped with the same frequency, but a increasing delay as the V_{hf} decreases. Table 1 lists the time delay

and the phase shift for each V_{hf} value.

V_{hf}	0.4	0.45	0.5	0.55	0.6
Time delay	0.61 nS	0.35 nS	0.22 nS	0.17 nS	0.13nS
Phase shift	219°	126°	79°	61°	46°

Table 1: Delay response in s and in degree for V_{hf} values from 0.4 to 0.6

3.3 Differentiator

Figure 15 shows a CSPFG Differentiator. The differentiator is made of the forwarding inverter A1 and a feedback circuitry consisting analog inverters A2 and A3. This circuit produces an output voltage that is

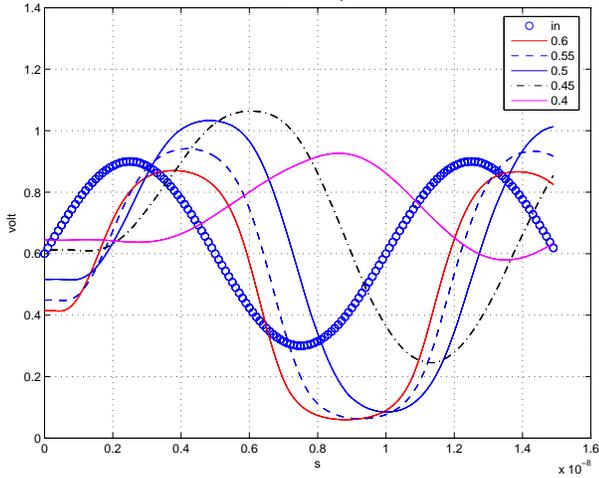


Figure 14: Delay simulation of 4 CSPFG inverters for vhf values from 0.4-0.6 as shown in the legend box

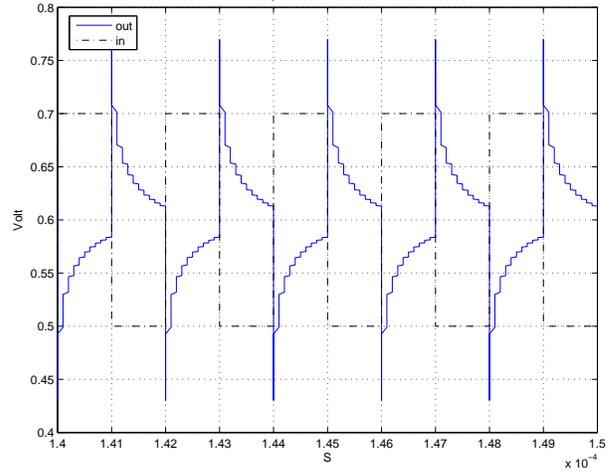


Figure 16: Pulse response of the CSPFG differentiator

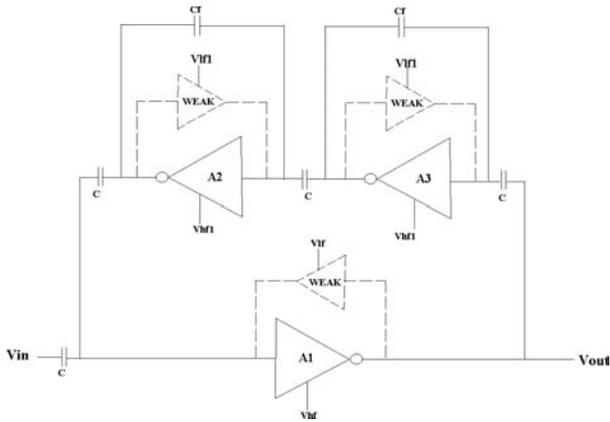


Figure 15: CSPFG differentiator

proportional to the rate change of the input voltage. This behavior has been shown in the figures 16 to 18. Figure 14 shows the circuits response to a square wave. We see that the output instantly jumps and settles fast to the circuits DC level of $VDD/2$.

C	Cf	Vhf	Vlf	Vhf1	Vlf1
10fF	11fF	1.2	0.85	0.55	0.85

Table 2: Bias vales and capacitor sizes used in the differentiator Circuit shown in figure 3

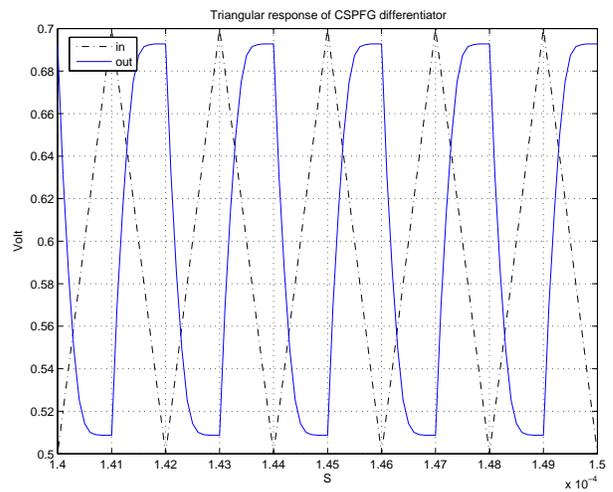


Figure 17: Response of the CSPFG differentiator to a triangular wave

Figure 17 illustrates the differentiator response to a triangular wave. The output is a square wave with opposite sign. From the figure we see that the corners of the square wave are being rounded resulting in a rise and fall time. This distortion is caused by circuits limiting gain and the limitations in very high frequencies. The limitations in high frequencies are not so dominant here because the circuit can operate with very high frequencies. This is shown and discussed in more details later.

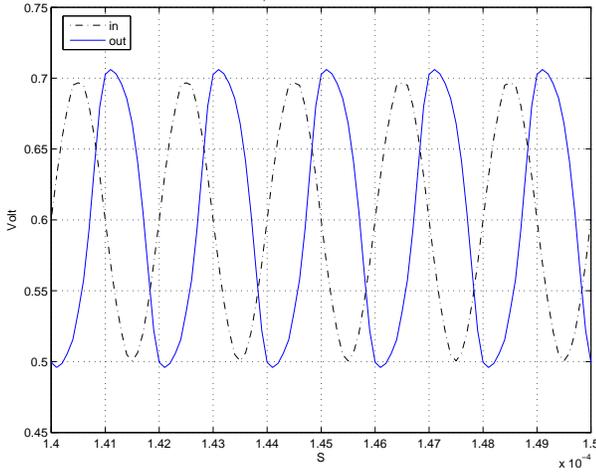


Figure 18: Response of the CSPFG Differentiator to a sine wave

Figure 18 shows the Differentiator’s response to a sine Wave. We can see that the output is a co sine wave with the same frequency. The output is lagging due to the circuits internal delay.

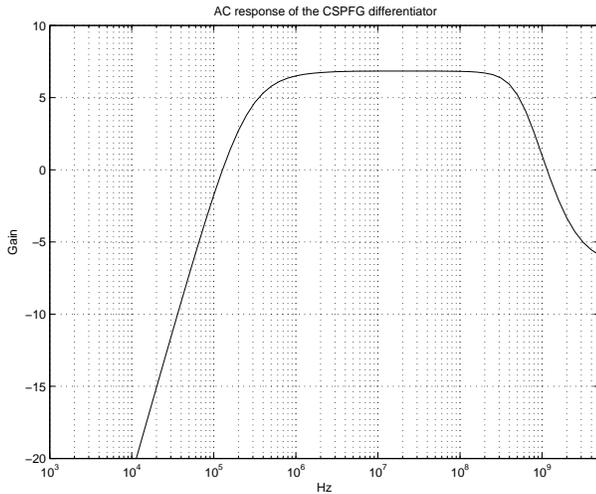


Figure 19: AC response of the CSPFG Differentiator

AC response of the differentiator is illustrated in figure 19. The circuit behaves as a high pass filter as expected, blocking frequencies below 100KHz. The bias voltages V_{hf} and V_{lf} can be used to change the bandwidth of the differentiator as they change the highest and lowest cutoff frequencies of the forwarding amplifier. The amplifier A_2 and A_3 determine the amplification of the circuit for different frequency bands. The bias voltages V_{hf1} and V_{lf1} can be used to change the bandwidth of the feedback circuitry. Ac-

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 cording to [22] the rise time t_r of the output of any linear system is related to the circuits upper cut-off frequency by:

$$t_r \approx \frac{0.35}{f_{max}} \quad (5)$$

assuming $f_{max} \approx 800MHz$ we will have a rise time of $t_r \approx 0.5ns$. This results in a very fast responding circuit.

4 CSPFG filters

In previous section we presented some circuits based on CSPFG inverters, these circuits demonstrated the versatility of the CSPFG inverter as amplifier. In this section we show that CSPFG inverters are also very well suited for designing active filters where the operational amplifier have been the main building block [23, 24, 25, 26, 27]. One draw back in designing filters using Operational amplifiers is that when connected in series their dc level will be very sensitive to environmental variations and can result in skew in offset/DC through the cascade [28]. This can easily be avoided using CSPFG circuit due to the capacitive coupling and local dc level adjustment. Another advantage using CSPFG inverters are that their cut-off frequency can be adjusted by a few bias voltages. In this section we present a CSPFG band pass filter and a CSPFG band stop filter.

4.1 Band pass filter

The differential CSPFG amplifier shown in figure 10 becomes a single input band pass filter simply by connecting the 2 inputs, $V+$ and $V-$ together as shown in figure 20. The input signal goes through 2 branches, the first branch is $C1$, the CSPFG amplifier $A1$ and $C2$, the other branch is $C3$. These branches are once again connected to each other at $V1$.

The amplifier $A1$ determines the lowest cutoff frequency of the filter by inverting all the signals in its pass band. The result is attenuation of the signal at $V1$ and a signal equal to the input signal for frequencies higher than the pass band. The amplifier $A3$ determines the highest cutoff frequency. The bias voltages V_{hf1} and V_{hf3} can be used to change the bandwidth of the filter as they change the highest cutoff frequencies of the $A1$ and $A3$ respectively. The amplifier $A2$ is used to increase the gain of the filter.

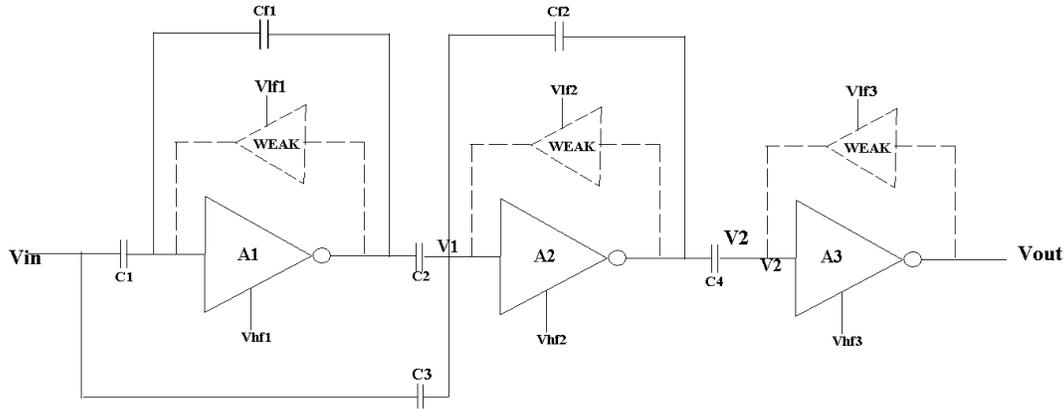


Figure 20: CSPFG Band pass filter

We may express the cutoff frequencies as:

$$f_{max} \approx \frac{\beta_{Wb} V_{hf2_{effective}}}{2C_1 VDD} \quad (6)$$

$$f_{min} \approx \frac{\beta_{Wb} V_{hf1_{effective}}}{2C_1 VDD} \quad (7)$$

The bandwidth of the band pass filter can be calculated as the difference between the lowest cut-off frequency and the highest cut-off frequency of the filter. The bandwidth can be approximated as:

$$f_{width} \approx \frac{\beta_{Wb}(V_{hf3_{effective}} - V_{hf1_{effective}})}{2C_1 VDD} \quad (8)$$

The Center frequency of the band pass filter is

$$f_{center} \approx \frac{\beta_{Wb}(\frac{V_{hf3_{effective}} - V_{hf1_{effective}}}{2})}{2C_1 VDD} \quad (9)$$

Figure 21 shows the AC response of the filter shown in figure 20. In this simulation we have tested the circuits AC response for various voltages on V_{hf1} . V_{hf2} is biased as V_{hf1} and V_{hf3} is biased 20 mV larger than V_{hf1} . The legend box in the figure lists the V_{hf1} values, increasing from 250mV to 600mV with a step of 50mV.

In figure 22 we see the circuits' response to a sinusoidal signal with a frequency of 200 MHz and amplitude of 300 mV. It is easy to see that the filter suppresses the sinus wave for biases other than 450mV.

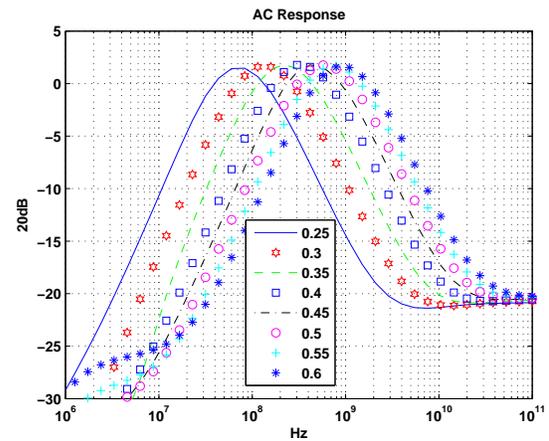


Figure 21: Band pass simulation of the CSPFG amplifier for different values on V_{hf1} , assuming that $V_{hf3} = V_{hf1} + 20mV$

The blue line (boxes) is the output result when the voltage on V_{hf1} is 450mV (in the pass area according to figure 6). A phase shift is also observed for each bias voltage. The phase shift increases as the bias voltage V_{hf} is lowered. Another phenomenon that is observed is that the DC level of the signal is changing due to changes in the bias voltages V_{hf3} . This is more likely caused by the unmatched transistors in the analog CSPFG inverter. The DC level change has no effect on the operation of the circuit due to the capacitive coupling between each CSPFG amplifier and can be neglected.

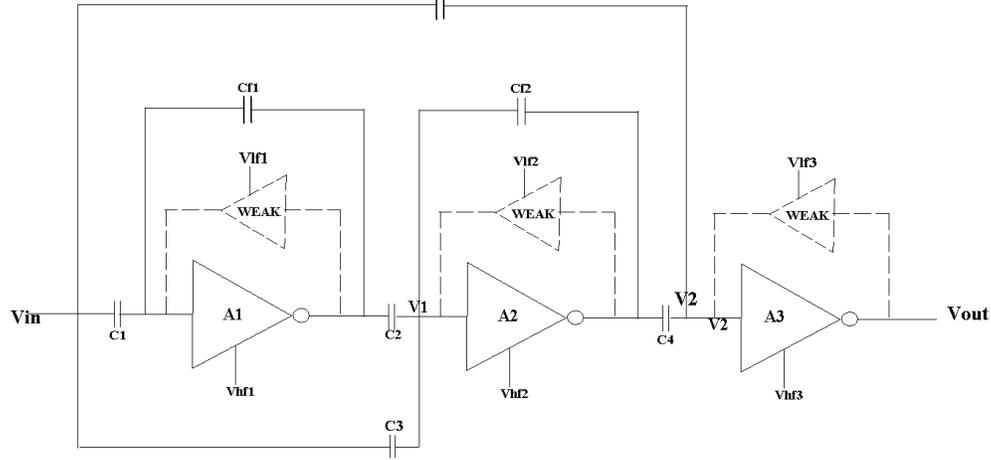


Figure 23: CSPFG band stop filter

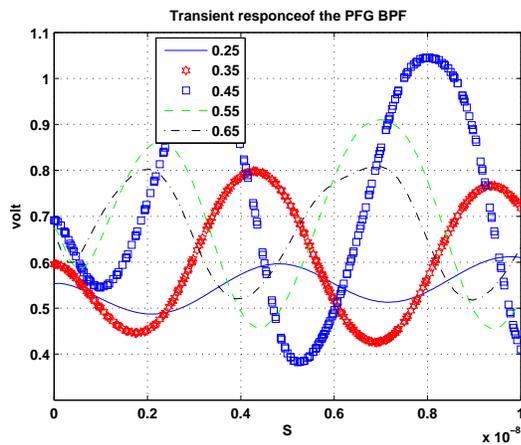


Figure 22: Time delay simulation of the CSPFG amplifier for different values on V_{hf1} , assuming that $V_{hf3} = V_{hf1} + 20mV$

4.2 Band stop filter

Figure 23 shows a band stop filter designed using the CSPFG inverters. The filter works with the same principal as the band pass filter presented in section 4.1 with 1 major change, the capacitor C_{bp} that connects the input to the output of the band pass filter, here called V2. C_{bp} inverts the band pass behavior of the filter to band stop by connecting the input signal to the inverting output, resulting in an attenuation of the signals in V2 in the pass band. The wide band CSPFG inverter A3 connected to the output is used only as an amplifier to increase the gain of the filter without effecting the filter properties. This inverter has no capacitive feedback, resulting in maximum gain. V_{hf} is

biased with VDD, to achieve a wide band amplifier.

Figure 24 shows the AC simulation result of the band stop filter shown in figure 22 for different values for v_{hf} as shown in the legend box.

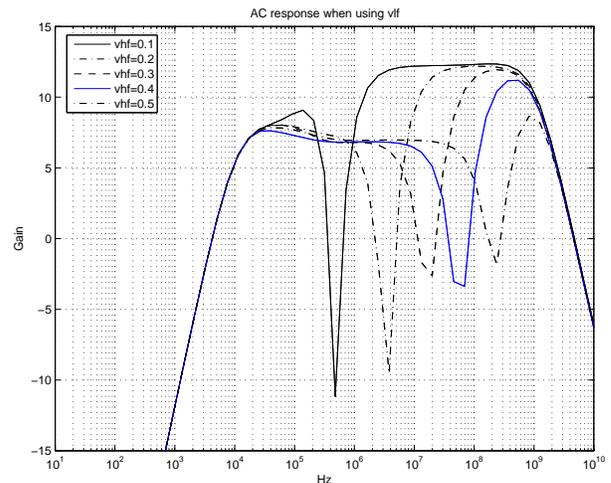


Figure 24: AC response of the band stop filter shown in figure 22 for different values of v_{hf} . assuming v_{hf2} 40mv larger than v_{hf}

$$f_{width} \approx \frac{\beta_{Wb}(V_{hf2_{effective}} - V_{hf1_{effective}})}{2C_i VDD} \quad (10)$$

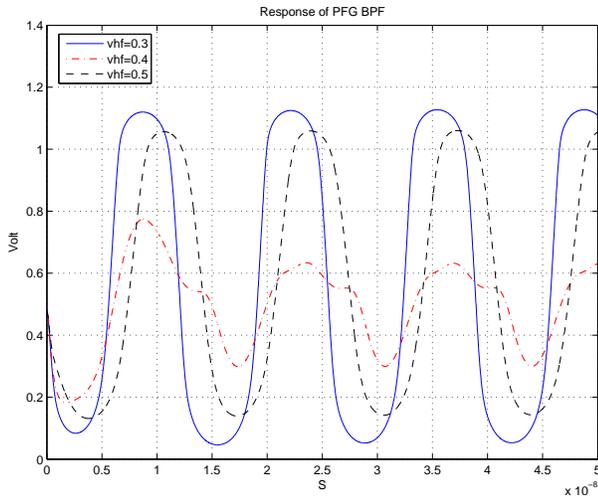


Figure 25: Response of the band stop filter to a sine wave with a frequency of 75 MHz shown in figure 22 for different values of vhf. assuming vhf2 40mv larger than vhf

Figure 25 is the response of the band stop filter for different values of vhf according to the legend box. The stimuli is a sinus wave with a frequency of 75MHz and a amplitude of 300 mV. We can clearly see that the band stop filter attenuates the stimuli for vhf equal to 400mV and it amplifies the signal for values below and above that, namely vhf equal to 300mV and 500 mV. The output signal within the stop band of the filter has a top to top value of approximately 330mv. This behavior is corresponds to the AC response of the circuit as shown in figure 24.

5 Conclusion

The CSPFG inverters presented in this paper can be used in various applications, both in analog and digital systems. In digital design as inverter and delay line and in analog design as amplifier and filter. Analog CSPFG amplifiers are immune to environmental variables such as temperature changes, small changes in VDD, because the operation point of each inverter is set locally and each inverter is capacitive separated from others. In filter design they offer tunability and are useful in application where a narrow band is to be detected. One important area is detecting frequency

in resonating sensors. Filter designed using CSPFG inverters are also suited for VLSI and ULSI circuit design duo to the physical size limitations in these, as no inductors or resistors is necessary. Other good properties of the CSPFG filters are simplicity and versatility. The ability to choose pass area, simply using a few bias voltages, allows tuning even after production and installation. When used as amplifiers, CSPFG inverters offer speed and high linear gain. As presented in this paper CSPFG inverters can replace operational amplifiers in many applications to ease the design, especially in filters and high frequency signal processing.

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