Analog design of a competitive middle layer for a new neural network for optical character recognition

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Abstract
An electronic circuit is presented, for a new type of neural network, which gives a recognition rate of over 100kHz. The network is used to classify handwritten numerals, presented as Fourier and wavelet descriptors, and has been shown to train far quicker than the popular Back Propagation Network whilst maintaining classification accuracy.

Indexing terms: Neural Networks, Fourier Descriptors, Wavelet Descriptors, OCR, Competitive Neurons, Analog Circuits.

Introduction

In neural network pattern recognition studies, the Back Propagation network (BPN) [1] is commonly employed. Although providing high accuracy results, this network can take excessive time to train. To overcome this, a new type of neural network has been developed and its hardware design is presented in this paper. The network, called the "Dynamic Supervised Forward-Propagation Network" (DSFPN) [2], is based upon the forward only Counterpropagation Network (CPN) [1]. Although the CPN will learn in few epochs, its unsupervised learning algorithm does not give a high classification accuracy. Unlike the CPN, the DSFPN is trained using a supervised algorithm which gives a far better classification accuracy but still trains extremely quickly. In addition the middle layer of the DSFPN can grow dynamically during training, allowing it to learn subclasses, in the training data, in an unsupervised manner.

Recognition results for handwritten numeral recognition, processed using Fourier and wavelet descriptors, are presented to demonstrate the superior performance of the DSFPN.

The DSFPN has a simple architecture, employing a hidden competitive middle layer, which makes it an ideal subject for hardware design. An analog circuit for the DSFPN is presented in this paper and results are given for tests run on electronics simulation software. These results show that the hardware version of the network can run accurately at a recognition rate of over 100kHz.

Neural Network

The DSFPN [2] is a feed-forward, competitive middle layer network, similar in operation to the forward only Counterpropagation Network. It differs from the CPN in two main ways: it uses a supervised training algorithm, and the middle layer may grow dynamically during training, both of which improve classification accuracy over the CPN.

Input data vectors, used with the DSFPN, must be normalized to a constant magnitude before being presented to the network; this can be achieved by the input neuron configuration known as the instar [1]. When a normalized input vector is presented to the network, each competitive middle layer neuron will respond in proportion to the scalar product of its input weight vector and the input data vector. The neuron with the highest activation will fire and all other neurons will be suppressed, giving a network output equal to the output of the winning neuron. A design for this competitive middle layer is presented below.

Classification Results

Table 1 shows results of handwritten numeral classification using Fourier descriptors [2]. The table shows that the DSFPN trains with 405 times less presentations than are required for the BPN; this represents a significant reduction in training time. Table 2 shows results for a DSFPN trained to classify handwritten numerals processed using wavelet descriptors [3], results are shown for three different levels of descriptor. The classification

accuracies achieved show a considerable improvement over the Fourier descriptor results in Table 1.

Circuit design of the DSFPN

The DSFPN functions using a middle layer of competitive neurons. In such a layer only the neuron with the highest activation will fire and all other neuron outputs will be suppressed. In a software implementation this task is trivial but in an electronic circuit, it requires a feedback structure know as "on-center off-surround feedback" [1] in which individual neurons receive positive feedback from their own output and negative feedback from all other neurons.

A competitive layer neuron, built from operational amplifiers working as current summing amplifiers, is shown in Fig 1. It receives data input through weight resistors connected to: the ADD input for positive input weights, and the SUB input for negative input weights. Resistor Rfon provides the on-center feedback link; the off-surround feedback link is via OFFin and OFFout. Rf1 and Rf2 are feedback control resistors. D1 limits the negative saturation level to 0 volts and R1 allows the diode junction capacitor to quickly charge/discharge when op-amp outputs switch between positive and negative voltages. OP1 and OP2 are very high speed op-amps of type LF351/NS, which is the National Semiconductors version of the 741 op-amp constructed using a J-FET input stage. Cf1 and Cf2 are low value capacitors, 33fF. Their purpose is to limit the instantaneous rate of change of the op-amp output voltages by making the op-amps operate in an integration mode. Without these capacitors, the SPICE implementation used was unable to resolve the op-amp output voltages. With these capacitors in place, the rate of change of output voltage can be seen from Fig. 3 to be approximately 3.75MV/S. This leads to a lag between the rise of the input voltages and the rise of the output voltage of 0.6µS. With an input voltage pulse applied every 10µS this corresponds to lag of considerably less than ½ a cycle and so will not cause the system to oscillation.

Competitive neurons are integrated together, to form a competitive layer, as shown in Fig. 2. Resistors $Rw_{m,n}$ are inversely proportional to the network weights. With this op-amp summing configuration, the contribution of each weight to the neuron activation is proportional to input voltage multiplied by Rf/Rw. This fact is important as the absolute values of resistors created by an analogue VLSI process can not be controlled accurately but the ratio of resistances created by the same process is accurate to a high order. Op-amp OPoff sums all neuron outputs to produce the off-surround feedback link. With this configuration, the rate of change of the output of neuron n is given by,

$$\frac{\partial v_{out,n}}{\partial t} \propto \mathbf{w}_{in,n} . \mathbf{v}_{in} + G_{off} \sum_{k=1}^{N} v_{out,k} + G_{on} v_{out,n} \quad (1)$$

where $w_{in,n}.v_{in}$ is the pattern data input, G_{off} is the negative off-surround feedback factor and $G_{on}v_{out,n}$ is the positive on-center feedback.

A reset line is included in this circuit to force all outputs back to zero when the inputs are removed.

To operate correctly, the feedback weights must be carefully chosen. When making this choice, we must bare in mind the effect of OPoff reaching saturation. This situation will arise when two or more neuron-outputs reach half saturation level, and so a list of conditions, for correct operation, can be produced:

(i) Two or more neurons may not rise to half saturation output, regardless of the input data-vector.

(ii) If all neurons have a low output then the neuron with the highest activation will rise, assuming that its data input voltage is positive.

(iii) If one neuron has a high output and positive data input, and all others have a low output, then the output of that neuron will rise to saturation and all other outputs will be suppressed.

The feedback weights and circuit parameters used to satisfy the above conditions and equation. 1 are as follows: G_{on} = 1.8, G_{off} = -1, saturation = 5v and maximum data input ($w_{in,n}.v_{in}$) = 0.5v.

Middle layer size

As the middle layer of the DSFPN may grow dynamically during training, the necessary number of middle layer neurons units required for a particular problem can not always be predicted in advance. To enable any number of middle layer neurons to be used, the structure shown in Fig 2 is designed to be built in a modular way. A number of modules may be connected together, to form a middle layer of any length by connecting the respective OFFin, OFFout and input lines. The off-surround feedback summation would be carried out by a separate op-amp.

Circuit simulation results

A simple circuit was tested using SPICE simulation. Weight resistors were calculated from a software simulation of a 10 hidden-neuron network, which had been trained on Fourier descriptor data. Input

voltages, calculated from the Fourier descriptors, were switched on to the analog input lines with a rate of 100kHz and a duty cycle of 0.5. The neuron outputs are shown in Fig. 3, which shows two pattern presentations representing the numerals '2' and '0' respectively. For clarity the neuron outputs have been spread vertically from the 0V level so the neurons, which are numbered 1 to 10, are centered around 1V to 10V respectively . The neurons 1 to 10 represent the numerals {'2', '0', '3', '4', '7', '6', '5', '9', '8', '1'} respectively. The figure shows the circuit operating correctly, initially more than one neuron responds to a particular input, the off-surround feedback will drive down all but the neuron with the greatest response. Checks on the network outputs for a full set of input vectors have shown that the correct neuron response to each input is achieved.

Conclusions

Results showing the effectiveness of the new neural network have been presented and hence the justification for a hardware implementation of this network to enable fast data classification. The DSFPN, can train 405 times faster than the commonly used Back Propagation Network, whilst still retaining a high recognition performance.

Wavelet descriptor have been shown to give considerably more accurate recognition results as compared to data presented as Fourier descriptors. The error rate reduction was from 2.22% for Fourier descriptors, to only 2.08% for wavelets.

A circuit implementation, for the DSFPN competitive middle layer, has been presented. Simulation results for this circuit show that it can perform reliable pattern recognition at a rate of 100kHz.

Acknowledgments

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Table 1 Fourier descriptor test results

Network	Number of presentations	Training time (S)	Accuracy on test data (%)
DSFPN	16264±466	5.35±0.15	97.78±0.02
CPN	4100±100	2.03±0.06	91.33±1.12
BPN	$(6.58\pm2.65)\times10^6$	4838±1946	94.25±2.50

Table 2 Wavelet descriptor results

Res. level	Number of presentations	Training time (S)	Accuracy on test data (%)
3	21270±1975	52.6±5.0	99.6±0
4	23820±1844	28.8±2.3	99.6±0
5	50874±5730	33.2±4.0	99.792±0.008

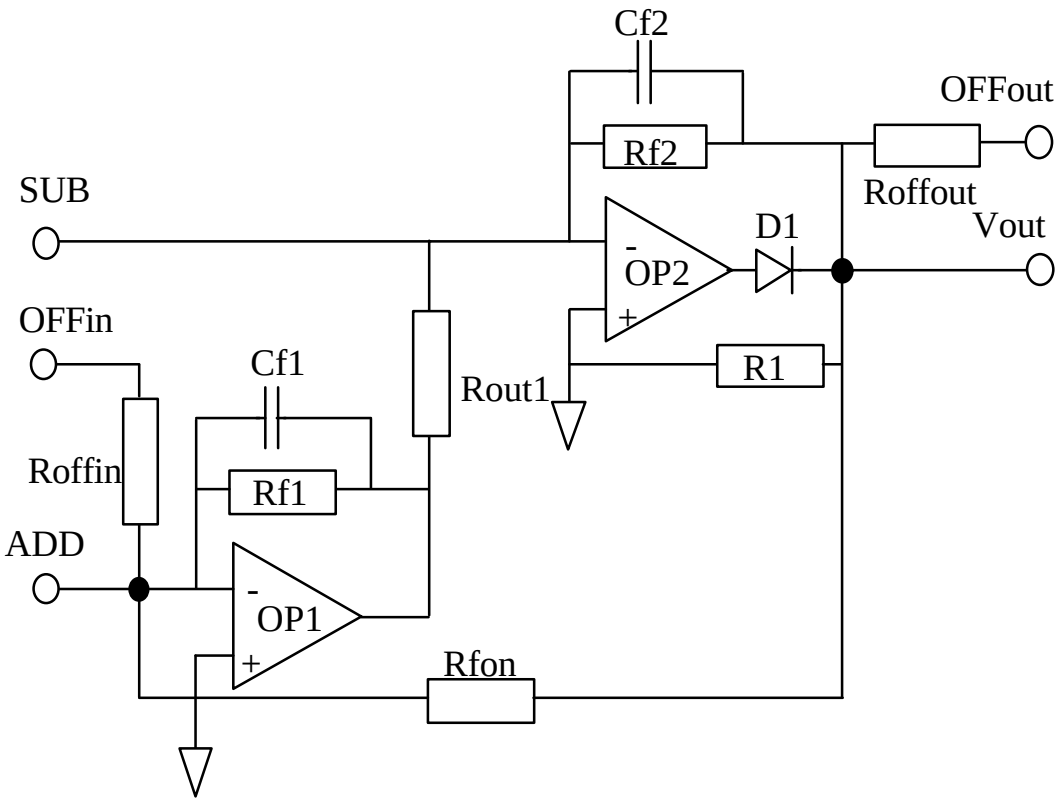
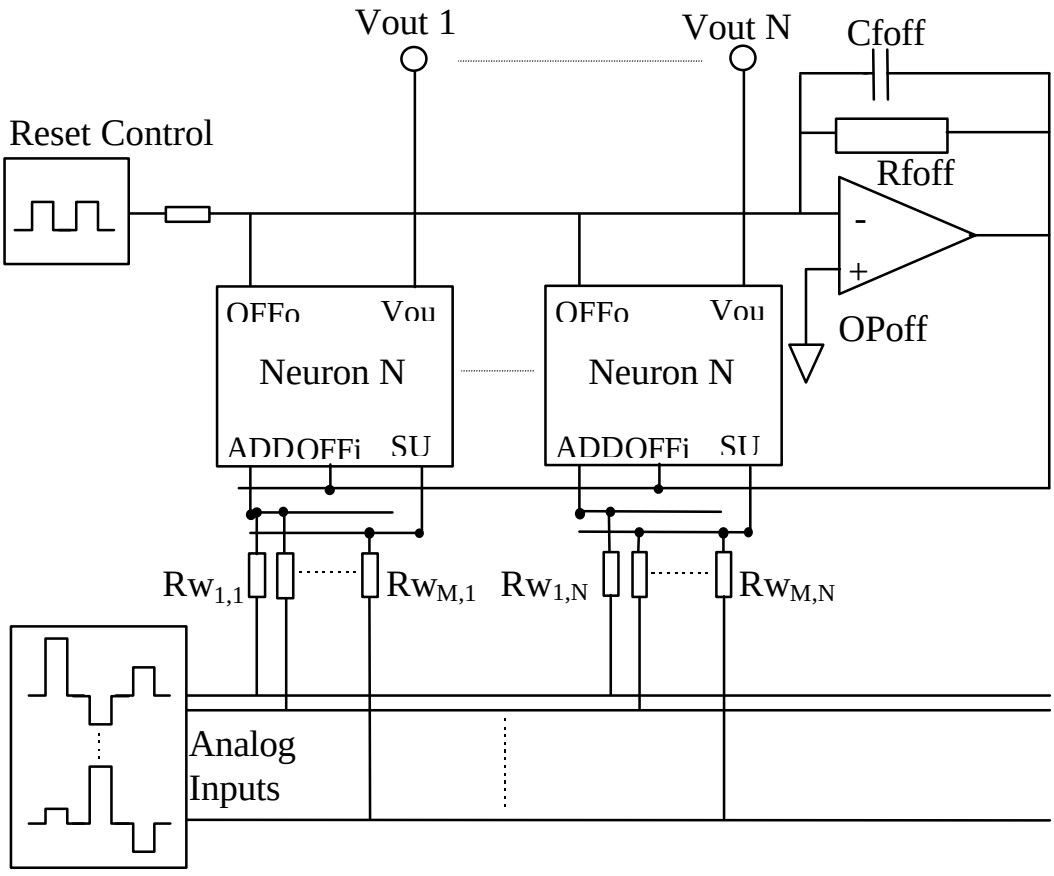


Figure 1 Competitive layer neuron



Key to neuron connections: 1-ADD, 2-SUB, 3-OFFin, 4-OFFout, 5-Vout

Figure 2 Competitive middle layer

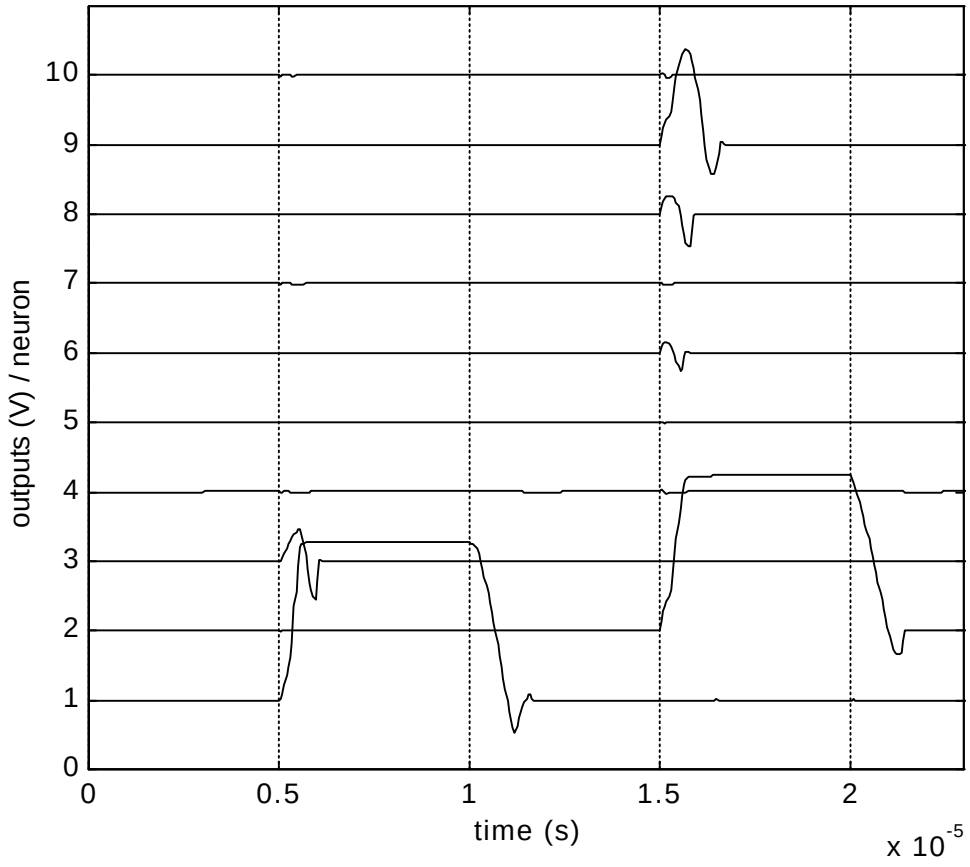


Figure 3 Output of DSFPN for 2 operations