Quantum Mechanical Simulation of High-k Gate Dielectrics Metal-Oxide-Semiconductor Structures

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Abstract: - High-k dielectric materials are being considered as replacement for SiO_2 as the gate dielectric since the high physical thickness can reduce the tunneling current while retaining the low equivalent oxide thickness (EOT) required next generation Metal-Oxide-Semiconductor field effect transistors (MOSFET's). In this paper, we simulate the capacitance – voltage (C-V) of n-type MOS devices with different high-k dielectric insulator numerically. According to the results, high-k dielectric materials maintain the capacitance and provide a robust physical thickness preventing tunneling current. Capacitance of high-k dielectrics couldn't be estimated by capacitance of insulator with EOT directly because an 8 % difference of capacitance among materials is observed in an extreme case. To obtain a accurate result, a self-consistent Schrödinger – Poisson equation should be considered.

Key-Words: - Quantum confinement effects, Schrödinger equation, High-k dielectric, MOS devices, Capacitance, Equivalent oxide thickness, Modeling and simulation.

1 Introduction

To span both 100 nm and 70 nm technology nodes, the oxide thickness of gate dielectric needs to be scaled below 1.5 nm [1-3]. Due to large gate leakage currents and reliability problems, which are caused by tunneling phenomena and appear even at low voltages these values cannot be obtained in a classical MOS structure with SiO_2 as gate oxide [4-5,18]. Clearly, if one looks at the capacitor equation, the only factor left to adjust is the dielectric constant. Therefore, while the actual scaling limit of SiO_2 is still debate, research on the high-k gate dielectrics has been expanded significantly to enable the capacitor dielectric to maintain a robust thickness while still providing a continuously shrinking area and storage voltage. As mentioned above, gate dielectric materials must have high dielectric constant, low leakage current and good thermal stability, interface characteristics comparable to Si-SiO_2. According to previous studies, high-k dielectric material such as SiO_2, Si_3N_4, HfO_2, TiO_2, Ta_2O_5, ZrO_2, La_2O_3 and their silicates are possible candidates [6-15,17].

However, it has been shown recently that higher physical gate oxide thickness can result in degradation of the electrical performance due to increased fringing fields from gate to source/drain. Therefore, gauging the impact of the gate stack on the device by accurate simulations of the MOS and MOSFET capacitance should be addressed for high-k dielectric application. In this study, capacitance - voltage (C-V) characteristics of MOS devices with four gate dielectric, which are SiO_2, Si_3N_4, HfO_2 and TiO_2, are examined quantitatively. An important result is presented. That is, equivalent oxide thickness (EOT) not only depends on dielectric constant but also depends on other characteristics of materials, such as band gap, conduction band electrode offset and so on. Estimating EOT of high-k materials by dielectric constant directly results in incorrect C-V characteristic, field and potential distribution in the substrate.

The remaining content of this study is given as follows. Sec. 2 briefly explains the simulation models and the computational method. Sec. 3 shows the simulation results and discussion. Sec. 4 draws the conclusion.

2 Modeling and Simulation

Capacitance of a MOS capacitor equals the oxide capacitance and the silicon capacitance connected in series. Since the silicon capacitance depends on total charge per unit area in siliocn, the distribution of charge should be estimated. The Schrödinger – Poisson equation are solved to obtain electron concentration, field and potential distribution in the substrate of the simulated MOS capacitor. Firstly, the Poisson equation is described as follows:

$$\nabla \varepsilon \cdot \nabla \psi = -q\left(p - n + N_D - N_A\right), \quad (1)$$

where ε is the electrical permittivity, q is the elementary electronic charge, n and p are the electron and hole densities, and N_D and N_A are the number of ionized donors and acceptors, respectively. The Schrödinger equation along the semiconductor substrate (z - direction) [17,18]

$$\left(-\frac{\partial}{\partial z}\frac{\hbar^2}{2m_{z,v}(z)}\frac{\partial}{\partial z}+E_C(z)\right)\Psi_{j,v}(z)=E_{j,v}\Psi_{j,v}(z). \quad (2)$$

$\hbar$ is the reduced Planck constant, E_C is the conduction band energy, v is the band valley, $m_{z,v}$, is the effective mass for valley in quantization direction, $\Psi_{j,v}$ is the j-th normalized eigenfunction in valley v; and , $E_{j,v}$ is the j-th eigenenergy. The computing procedure is given as follows. Firstly, the stop criteria, mesh, output variables and simulation models are chosen. Then, Poisson equation is solved iteratively until the result converges. Next, Schrödinger equation is solved until it converges. After the two equations converge, we'll check the whole system converges or not. If the whole system converges, then stop computing. Otherwise, the outer loop should be iterated again until the whole system converges. This scheme makes sure the solution will be self-consistent. Thus, the capacitance could be estimated accuratly.

3 Results and Discussion

In the numerical studies, a NMOS with 30 nm gate length is simulated. Figure 1 illustrates the simulated NMOS. The thickness of poly-Si gate (H_g) is 100 nm and the thickness of p+ substrate (H_s) is 250 nm. The doping concentration of substrate is 5×10^{19} cm^{-3}. Two equivalent oxide thicknesses, 2 nm and 4 nm, are simulated by a 10 Hz frequency ac signal. Applied gate voltage varies from –1.5 ~ 1.5 V. High-k dielectric materials considered in this work are Si_3N_4, HfO_2 and TiO_2. Table 1 gives the dielectric constant of them and the EOTs of each material are given in Table 2. Numerical results of the NMOS are obtained by using a commercial TCAD tool, ISE-DESSIS ver. 8.0.3 [19].

Table 1. Dielectric constants of high-k Insulators.

Materials	SiO_2	Si_3N_4	HfO_2	TiO_2
k	3.9	7.5	21	60
Band gap (eV)	9	5	6	3.1

Table 2. Equivalent oxide thickness for high-k Insulators.

Materials	SiO_2	Si_3N_4	HfO_2	TiO_2
EOT 1 (nm)	2	3.85	10.77	30.77
EOT 2 (nm)	4	7.69	21.54	61.54

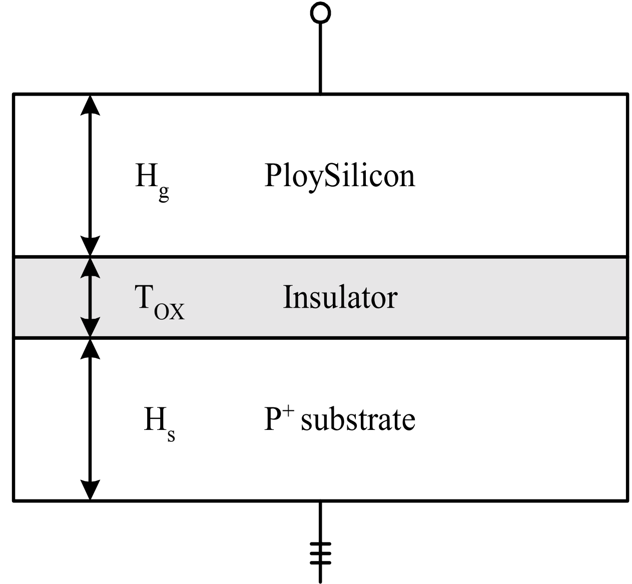

Fig. 1. The simulated NMOS with 30 nm gate length.

In this study, we assume that there is no interfacial trap charge. Figures 2 and 3 shows simulated C-V curves of MOS with SiO_2 and TiO_2 for EOT = 2 and 4 nm. EOT is given by

$$EOT = \left(k_{SiO_2}/k_x\right) \quad t_x \quad (3)$$

where k_x is the k value for the film of interest, t_x is the physical thickness of the film of interest and k_{SiO2} is the k value of silicon dioxide. EOTs in Table 2 are calculated by Eq. (3).

According to the results, a thinner oxide thickness actually induces a larger capacitance than a thicker one. Approximately, the difference of capacitance is proportional to $1/t_x$. Since capacitance of a MOS capacitor equals the oxide capacitance and the silicon capacitance connected in series, total capacitance can be expressed as

$$C = C_{OX}C_{Si}/\left(C_{OX}+C_{Si}\right), \quad (4)$$

where C_{OX} and C_{Si} are capacitance of gate dielectric and silicon, respectively. Once strong inversion layer forms, total capacitance is dominated by the silicon capacitance. C is approximated by C_{OX}, which is k_x/t_x. Therefore, C is proportional to $1/t_x$.

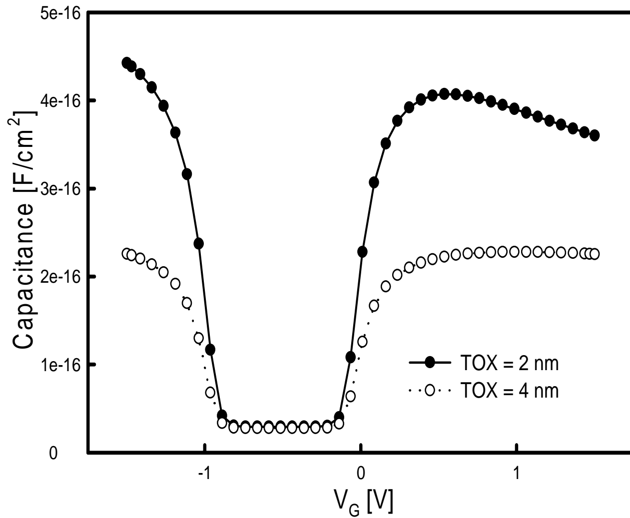

Fig. 2. The simulated capacitance of the NMOS with 2 and 4 nm SiO_2 gate dielectric thickness.

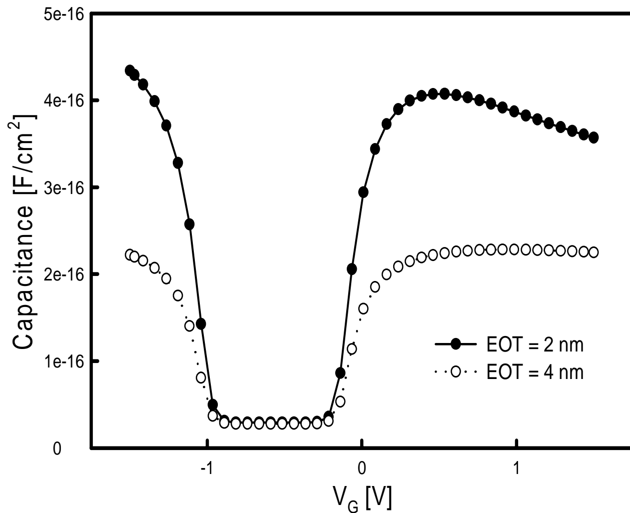

Fig. 3. The simulated capacitance of the NMOS with 2 and 4 nm TiO_2 gate dielectric thickness.

Figures 4 and 5 illustrates C-V curves with different high-k materials for EOT = 2 and 4 nm. From the figures, differences of capacitance with different materials are shown. In an extreme case, an 8 % difference is observed. It is because electric field would penetrate through insulator into silicon. The penetrating mechanism depends on the physical thickness of insulator, band gap, band structure, conduction band electrode offset and quantum mechanism. Therefore, we cannot estimate C by C_{ox} and Eq. (3) directly. A Schrödinger – Poisson equation should be considered.

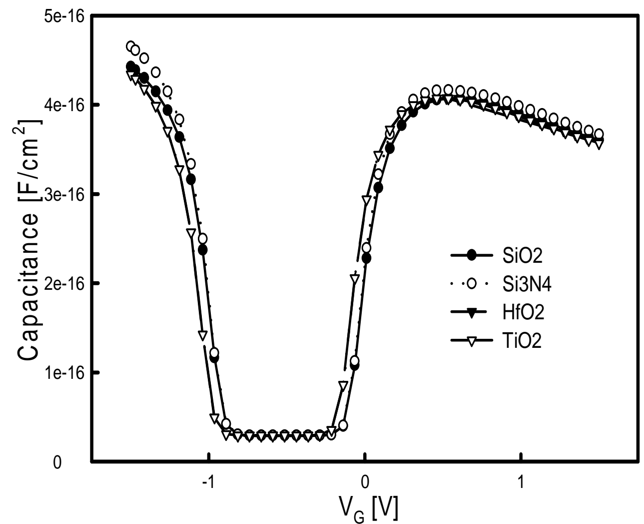

Fig. 4. The simulated capacitance for the NMOS of different gate dielectric materials with EOT = 2 nm.

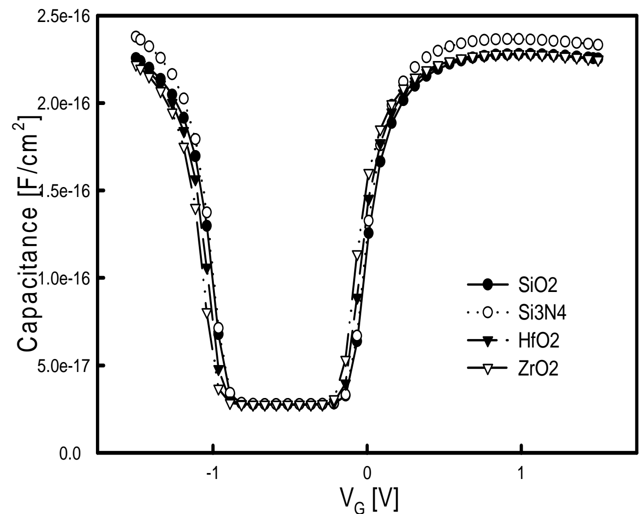

Fig. 5. NMOS capacitance with different gate dielectric materials, where EOT = 4 nm.

According to the numerical results mentioned above, we can make summary of the results. High-k dielectrics actually provide a robust thickness without losing any capacitance. Capacitance of high-k dielectrics couldn't be estimated by capacitance of insulator with EOT directly because an 8 % difference of capacitance among materials is observed in an extreme case. The difference is caused by the penetrating mechanism of different materials. Therefore, the penetrating mechanism has to be

analyzed and model carefully to obtain an accurate device capacitance.

4 Conclusions

To increase the gate capacitance while reducing the tunneling current, alternative high dielectric constant materials are currently under intense investigation. In this paper, a 30 nm NMOS is simulated with SiO_2, Si_3N_4, HfO_2 and TiO_2. A self-consistent Schrödinger – Poisson equation are considered to obtain the capacitance of the simulated device. The results are more accurate than estimating capacitance by oxide capacitance with EOT. According to our numerical studies, high-k dielectrics ensure a continuously shrinking of MOS/MOSFET possible without gate leakage concern. Although high-k gate dielectrics seem to be an attractive solution of continuous scaling of MOS device, a number of difficulties are investigated: (1) crystallization upon heating; (2) dopant penetration; (3) fixed charge; (4) in some cases instability in contact with poly Si; (5) low channel mobility; and (6) uncontrolled oxide formation at the Si/high-k interface. The selection of suitable materials and their process are left for further studies.

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