Gate Tunneling Current Calculation of Nanoscale MOSFETs with a Unified Quantum Correction SPICE Model

SHAO-MING YU[1], JAM-WEM LEE[2], and YIMING LI[2,3,*]
[1]Department of Computer Science, National Chiao Tung University
[2]Departmenet of Nano Device Technology, National Nano Device Laboratories
[3]Microelectronics and Information Systems Research Center, National Chiao Tung University
[*]P.O. Box 25-178, Hsinchu city, Hsinchu 300
TAIWAN

Abstract: - In this paper, an analytical quantum correction model for ultrathin oxide MOSFET devices is proposed. With this novel SPICE-compatible model, the gate tunneling current is precisely calculated without any complicated quantum mechanical models. The proposed model is optimized with respect to (i) the position of the charge concentration peak, (ii) the maximum of the charge concentration, (iii) the total inversion charge sheet density, and (iv) the average inversion charge depth, respectively. Comparing with the conventional approach to direct tunneling current calculation, the proposed model demonstrates good agreement with the quantum mechanical simulation. Make it more clearly that the quantum correction technique can be unified used in modeling the quantum confinement effects in gate tunneling current, gate to channel capacitance, and channel current. Our quantum correction model can accurately account quantum effects of nanoscale MOSFET and can directly be implemented into vary large scaled integration (VLSI) circuit simulation.

Key-Words: Nanoscale MOSFET, Thin Oxide, Direct Tunneling, SPICE-compatible, Quantum Mechanical Effects, Quantum Correction, Schrödinger-Poisson, Modeling and Simulation, Circuit Simulation

1 Introduction

To maintain good controllability of the short-channel effect of the sustaining scaled down CMOS devices, the gate oxide thickness should be simultaneously reduced accordingly to the channel length [1-28]. For the sub-100 nm CMOS devices, thickness of gate oxides, which smaller than 2 nm is strongly wanted. In those ultra thin gate oxides, a substantial direct tunneling current flowing from the gate to the channel will result in a gate leakage current even under low voltage operating condition; furthermore, the gate tunneling current increases exponentially with the decrement of oxide thickness [1, 4, 6-7, 14-28]. Consequently, the increasing leakage current will become a serious problem, especially in terms of the standby power consumption. Accordingly, a precisely calculation of the gate leakage current is very important in ensuring the performance of any designed VLSI circuits [1,14-28].

Owing to the confinement of carriers in the narrow potential well close to an inverted or accumulated silicon surface, their motion in the direction normal to the surface must be treated quantum-mechanically [1-13]. That is, the electronic properties of inversion and accumulation layers exhibit two - dimensional (2D) transport behavior. For thin gate oxides, the quantum effect can cause a significant discrepancy and greatly degrades the gate to channel capacitance. For the task of the gate tunneling current modeling, the electrons exhibiting 2D transport character, the transmission probability applicable to an incident Fermi gas of free electrons is no longer a meaningful concept and the well known WKB approximation [1,27] or the numerical integration of Airy functions [1] is not valid. For exactly simulating the effects, quantum mechanical model of electron / hole tunneling from the quantized was proposed recently [1]. The previously motioned method could predict gate-tunneling current; however, it is a very time-consuming task in the numerical solution of the Schrödinger-Poisson (SP) equations [1-13]. In order to perform the correction in whole circuit simulations, the incorporation of the quantization effects in SPICE models is necessary, especially designing the nanoscale MOSFETs' VLSI circuits. Because leaking of quantum corrections, the gate leakage current is always underestimated and the circuit performance becomes greatly overestimated. As a result, the quantum corrected gate tunneling current model is strongly wanted for an exact simulation of nanoscale MOSFETs' VLSI circuits.

Based on our recent work, we in this paper have successfully developed a unified SPICE model for

nanoscale MOSFET simulation [4-12]. The model introduces a SPICE-compatible quantum correction for gate tunneling current, gate to channel capacitance, and channel current. The quantum correction method represents quantum effects by a modification function that constructed by T_{ox} and V_G for the purpose of simulating nanoscale MOSFETs.

2 Quantum Correction Model

As shown in Fig. 1, we perform the quantum correction of the carrier density. The calculated inversion-layer charge densities could be then cast into the form [4-12]

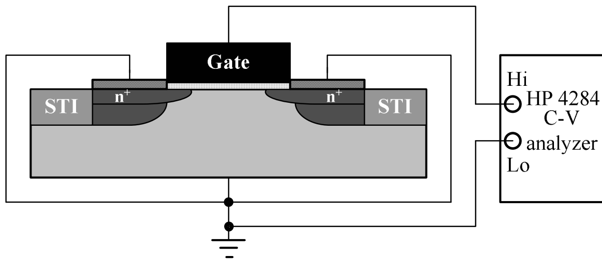

Fig. 1. A cross section view of the nanoscale MOSFET and C-V curves measurement configuration.

$$n_{QM} = n_{CL} a_0 \times [1 - \exp(-a_1 (\frac{x}{\lambda_{th}})^2 + a_2 (\frac{x}{\lambda_{th}})^4 - a_3 (\frac{x}{\lambda_{th}})^6)], \quad (1)$$

where n_{CL} is the classical electron density solved from the Poisson equation and

$$\lambda_{th} = (\frac{\hbar}{2m^* k_B T})^{1/2} \quad (2)$$

is the thermal wavelength. We can also write n_{CL} into the following analytical expression:

$$n_{CL} = n_i b_0 \exp(-b_1 \frac{x}{\lambda_{th}}). \quad (3)$$

The optimal parameters a_0, a_1, $a_2 = 0$, a_3, b_0, and b_1 are calculated and calibrated from the solution of SP equations for the proposed model. They are modeled as a function of V_G and T_{ox}, shown below:

$$a_0 = 2.82 - 0.555 \exp(-V_G), \quad (4)$$

$$a_1 = 2.22 - 1.79 \exp(-V_G) - 0.21 T_{ox}, \quad (5)$$

$$a_3 = -0.00467 + 1.048 V_G^2 / T_{ox}^{1.23}, \quad (6)$$

$$b_0 = (-88 + 23888 V_G) - (1838 + 9075 V_G) T_{ox} + (403 + 1189 V_G) T_{ox}^{\ 2}, \quad (7)$$

$$b_1 = (1.9 + 0.5 V_G) - (0.26 - 0.05 V_G) T_{ox}, \quad (8)$$

where V_G is in volts and T_{ox} is in nm. The model parameters given in (4)-(8) are based on a p-type substrate with $N_A = 10^{17}$ cm^{-3}. For other substrate doping, V_G should be adjusted by an amount equal to a shift in the threshold voltage due to the change in N_A. Thus, we can write C_{total} into expressions of V_G and T_{OX}; finally, we can obtain a C_{QM} in function of V_G and T_{OX}.

3 Modeling of Direct Tunneling Current

The direct tunneling current is easily modeled by the following correction formula

$$J_g = J_0 D(E_T) F_s(E_T), \quad (8)$$

$$J_0 = q m^* k_B^{\ 2} T^2 / (2\pi^2 \hbar^3), \quad (9)$$

$$F_s = \ln(\frac{1 + \Delta si}{1 + \Delta poly}), \quad (10)$$

$$\Delta si = \exp(\frac{E_f^{\ si} - E_T}{k_B T}), \quad (11)$$

$$\Delta poly = \exp(\frac{E_f^{\ poly} - E_T}{k_B T}), \quad (12)$$

$$D(E_T) = \exp(B[G_1 + G_2 \frac{|V_{ox}|}{X_B}(1 + G_3 \frac{|V_{ox}|}{X_B})]), \quad (13)$$

$$X_{Bt} = X_B - E_T, \quad (14)$$

$$E_T = E_{Cs}^{\ si} + \frac{1}{2}(\sqrt{(V_{ox} - G_0)^2 + 10^{-3}} - (V_{ox} - G_0 \phi_t)), \quad (15)$$

where $E_f^{\ si}$ is the Fermi level of silicon substrate and

the E_f^{poly} is the Fermi level of the polysilicon gate. V_{ox} is voltage drop across the gate oxide, and B is a constant given by

$$B = \frac{2T_{ox}}{\hbar}\sqrt{2qm^* X_{Bt}} \quad (16)$$

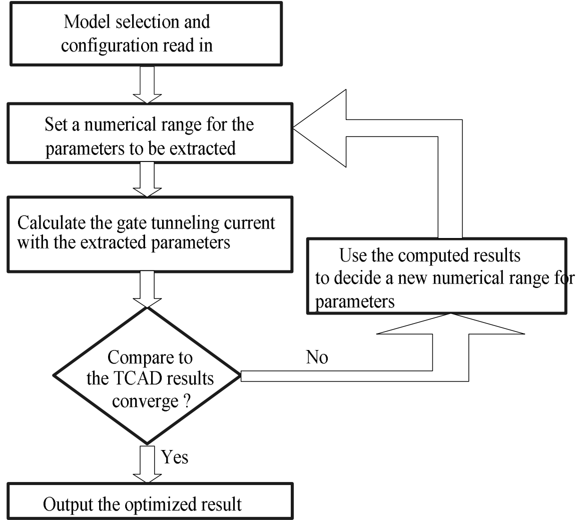

Fig. 2. An optimization procedure used in our simulation.

$G_0 \sim G_3$ are the fitting parameters that have to be optimized by comparing the result of SP device solver. Fig. 2 shows the optimization procedure in our simulation for extracting the parameters $G_0 \sim G_3$. The parameters also have some characteristics which can help us to obtain the optimized value for each parameter. The parameter G_1 controls the overall tunneling current level. The parameters G_2 and G_3 can control the slope and curvature of the log I_g vs. V_{gs} characteristics.

4 Application to C-V Characteristics

We have applied our quantum correction model for the inversion charge to the calculation of C-V curves. A 20×20 μm^2 N-MOSFET with T_{ox} = 1.6 nm is fabricated and measured for the C-V curve. The exact oxide thickness is calculated form high resolution transmission electron scope (HRTEM) image shown in Fig 3 which indicates that oxide thickness is 1.6 nm. The experimentally measured data is shown together with the traditional method and the SP result in Fig. 3. The agreement is excellent except for $V_g \geq 1.0$ V. This is expected as we have assumed zero penetration of the wavefunction into the oxide in our SP equation solver. The deviation of the calculated result from the measured data indicates that there is a substantial tunneling through the oxide taking place at $V_g \geq 1.0$ V [8].

With introducing the quantum capacitor, the SPICE simulator could predict C-V characteristics of MOS capacitor accurately. Moreover, incorporation of the capacitor into MOSFET structure can also help us to obtain a more precise I-V and C-V behaviors.

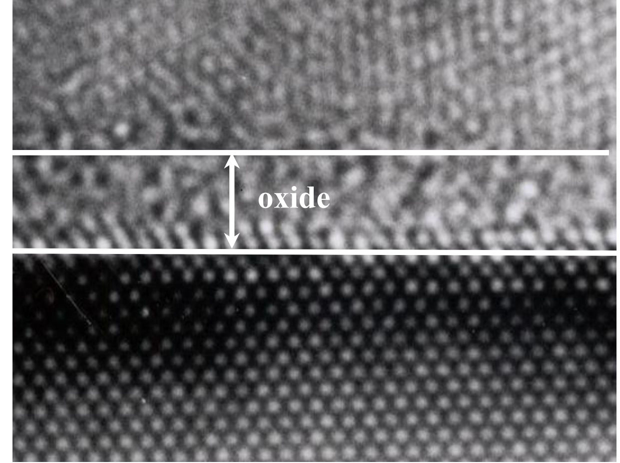

Fig. 3. HRTEM image of the experiment sample, which shows T_{ox} = 1.6 nm.

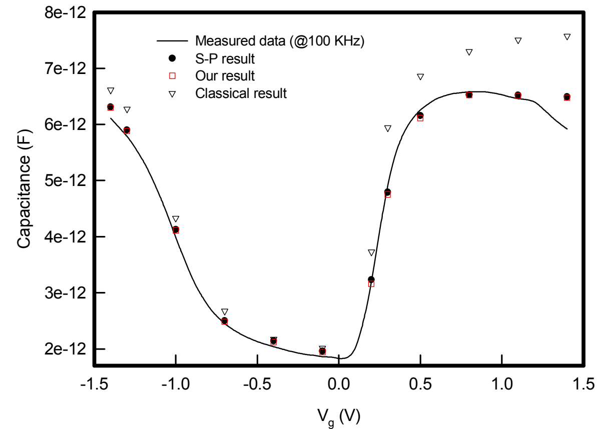

Fig. 3. A comparison of the simulated and measured C-V curves for the proposed SPICE-compatible model and the SP model.

5 Gate Tunneling Current Simulation

Gate tunneling current is firstly fitted by using the tunneling current expressions showing in the section 3. In the calculation, Fermi level at silicon substrate is mainly obtained from the classical calculations. That is, the Fermi level is simply get from the solving of Poisson equation. Owing to a leaking of quantum correction, the calculated Fermi level will be wrong, moreover, the voltage across the thin gate oxide will be greatly underestimated. For the underrating of Vox, the gate tunneling current would be largely miscalculated.

The tunneling current calculated from the classical surface potential is shown in the Fig. 4 that the compact model presents good agreement with the simulated result by a commercial TCAD tool – ISE [28]. This good result is not only useful for the 3 nm thicken oxide shown in Fig. 4 but also for the thinner oxide result exhibited in Figs. 5 ~7.

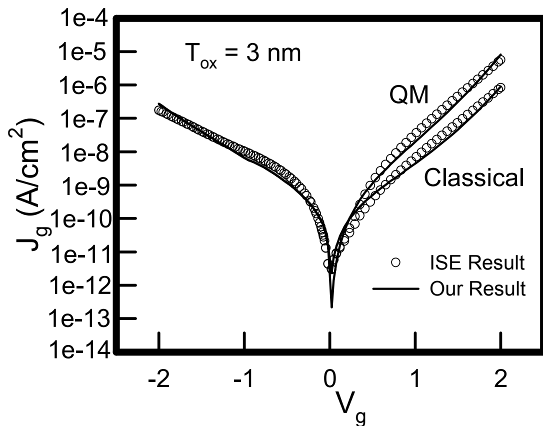

Fig. 4. A comparison of the simulated gate tunneling current among the classical, our model and the TCAD result. The thickness of the gate oxide is 3 nm thick.

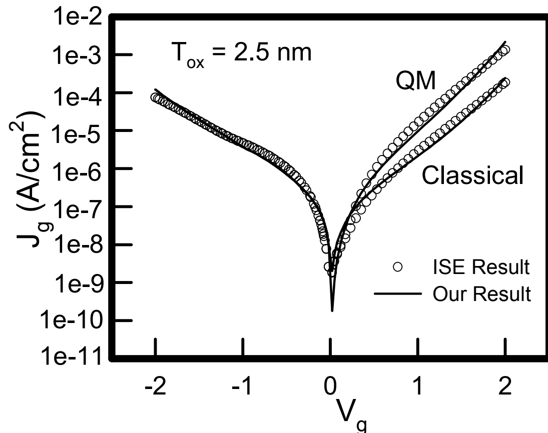

Fig. 5. A comparison of the simulated gate tunneling current among the classical, our model and the TCAD result. The thickness of the gate oxide is 2.5 nm thick.

Figures 4-7 also show the gate tunneling currents obtained from the quantum potential based calculations. It could be addressed that, with introducing the quantum potential into the model shown in the section 3, we can have a quantum corrected gate tunneling without changing expression, constant ,and parameters. Make it more clearly that, with using the quantum potential, one can have a accurate result wihtout changing the parameters extracted from the classical result.

The results explore a very attractive fact that with incorporating the quantum potential correction, one can easily simulate direct tunneling current precisely. Traditionally, the exact direct tunneling current has to be computed from the self-consistently solving of two partial differential equations; those are Poisson equation, and Schrödinger equation. Couple computing of the Schrödinger and Poisson equations is very time consuming; which is very difficult to apply them to the advanced design of modern VLSI circuits. Our quantum correction model; on the contrary, is very simple in calculations, moreover, sustains a very good agreement between the model and TCAD result. This is very useful in circuit design that the gate leakage current could be taken into consideration in performing the circuit simulations.

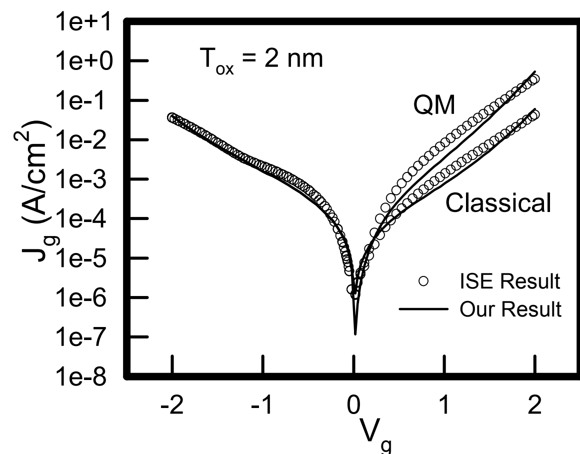

Fig. 6. A comparison of the simulated gate tunneling current among the classical, our model and the TCAD result. The thickness of the gate oxide is 2 nm thick.

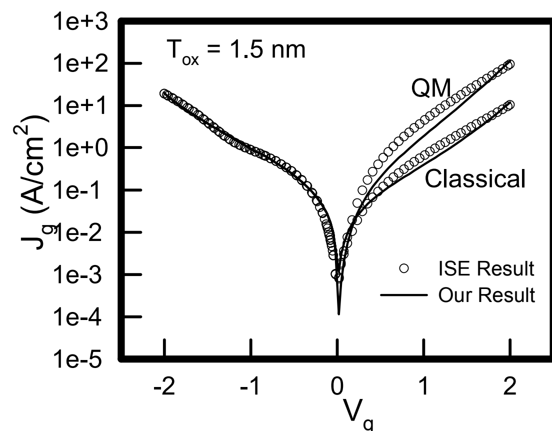

Fig. 7. A comparison of the simulated gate tunneling current among the classical, our model and the TCAD result. The thickness of the gate oxide is 1.5 nm thick.

Our quantum correction method contents a good agreement over a wide range of the oxide thickness. That is, by using the same set of fitting parameters, gate leakage current in various thicken oxides could be predicted that one can estinmate the thickness variance induced gate current instability. This is especially important for the circuit design by the nanoscaled MOSFET that 10% variance of the gate oxide is acceptable; therefore, the manufacturing variation can be efficiently estimated from our proposed SPICE model. With using the quantum corrected model for SPICE simualtion, the effects of the gate leakage could be precisely calculated that design margin can be reduced to obtain a better circuit performance.

The quantum correction is not only achieved on the modeling of gate tunneling current, but also on the modification of channel carrier concentration. In one word, with introducing the adjustment, all of the quantum effect could be solved at once. Moreover, only a littile computational complexity is added.

6 Conclusions

A SPICE-based gate tunneling correction model has been proposed and demonstrated in this paper. The proposed model was mainly optimized with respect to (i) the position of the charge concentration peak, (ii) the maximum of the charge concentration, (iii) the total inversion charge sheet density, and (iv) the average inversion charge depth, respectively. Any exact calculations of direct tunneling current were computed from the self-consistently solving of two partial differential equations; those are Poisson equation, and Schrödinger equation. Couple computing of the Schrödinger and Poisson equations is very time consuming in realistic device simulation. It becomes a bottleneck of applying them to the advanced design of modern VLSI circuits. Our quantum correction model proposed here; on the contrary, is very simple in practical applications. Furthermore, it sustains a very good agreement between the model and TCAD result. This is very useful in circuit design that the gate leakage current could be taken into consideration in performing the circuit simulations. With introducing the quantum correction compact model, one can easily calibrate all quantum effects at the same time. The most attractive characteristic is few additional computational complexity added. Those properties are very attractive and useful for both the designs of novel VLSI circuits and system-on-a-chip; especially for the circuits and systems which constructed by the nanoscale devices.

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